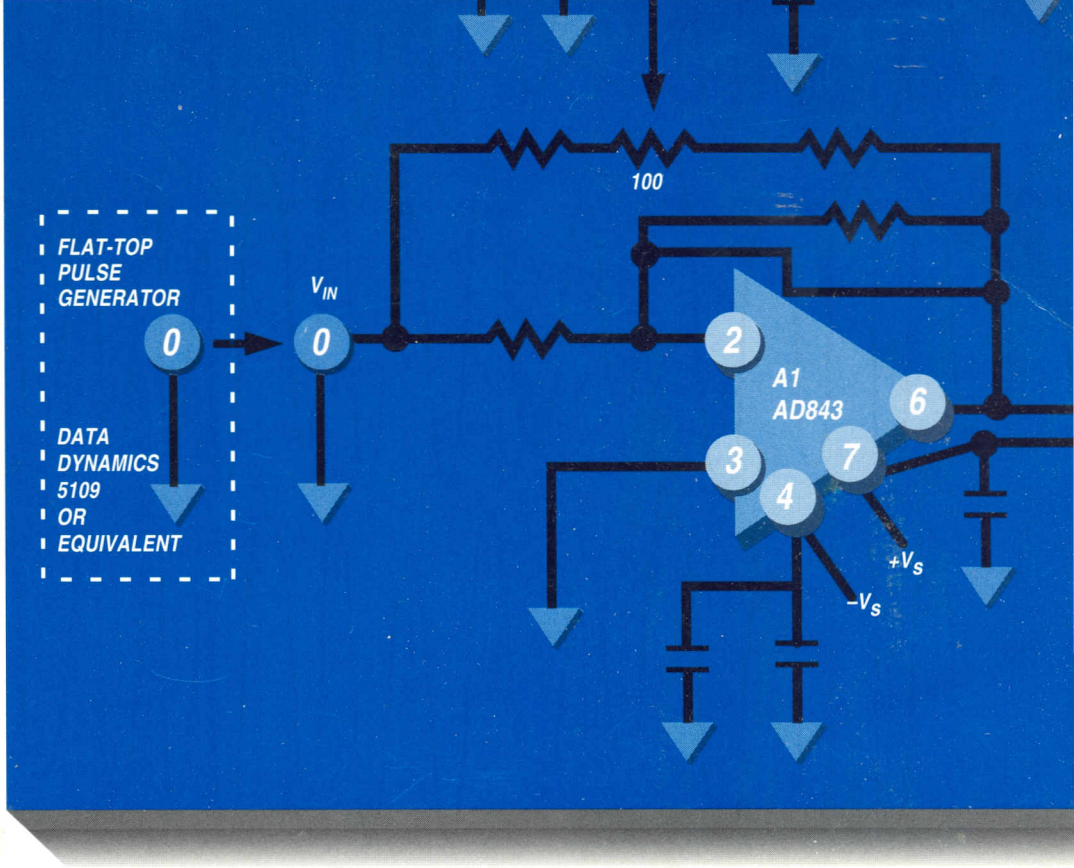
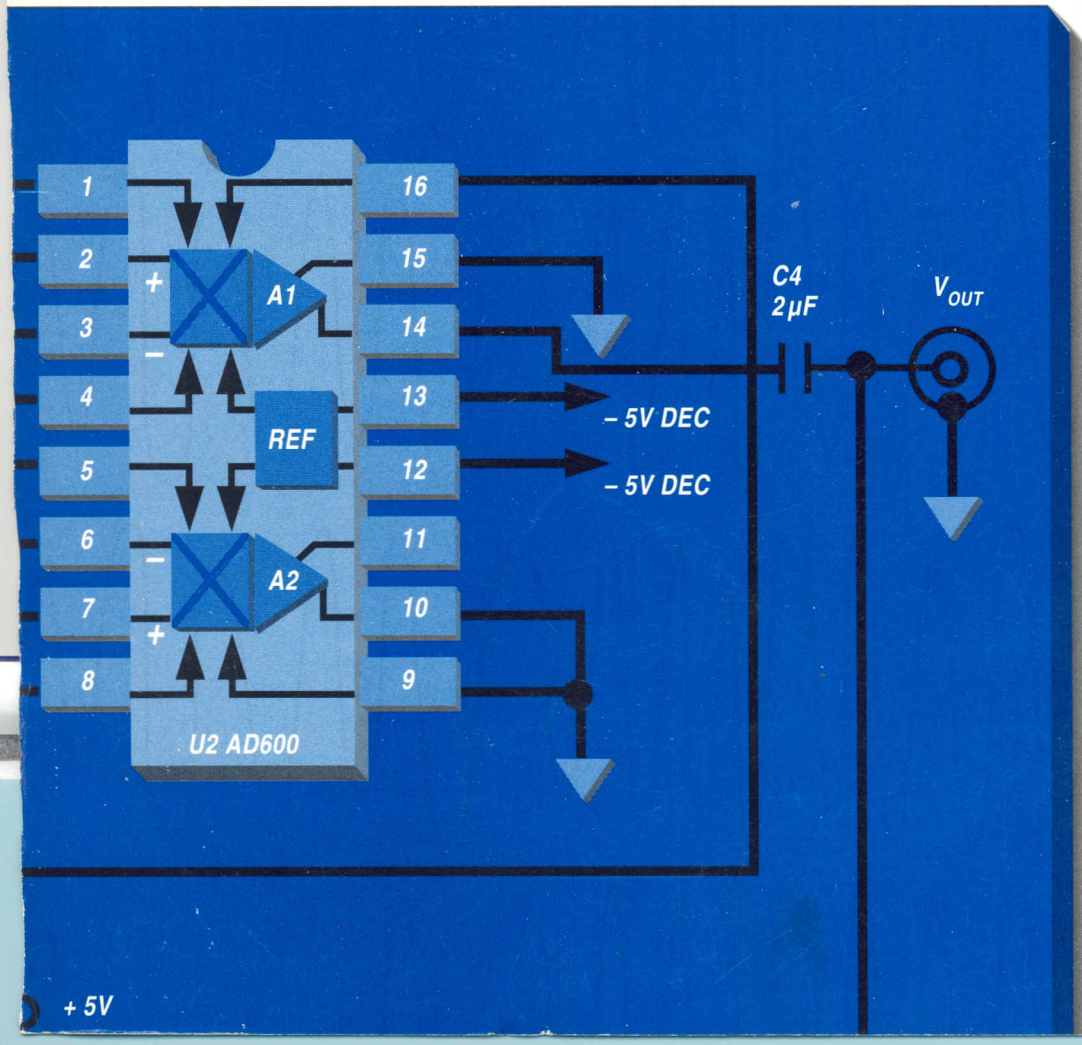
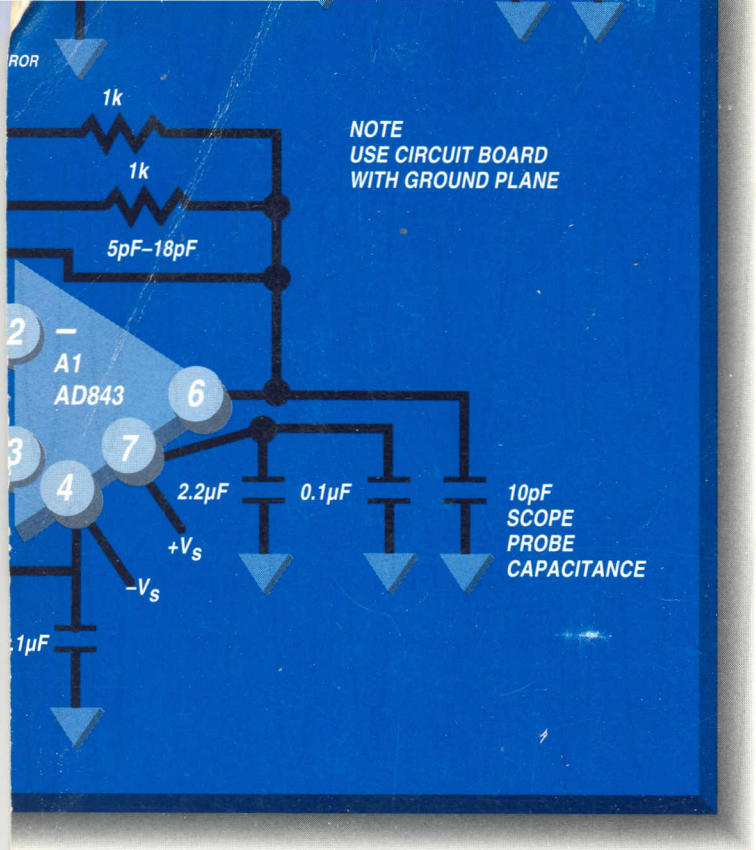


1992 AMPLIFIER APPLICATIONS GUIDE



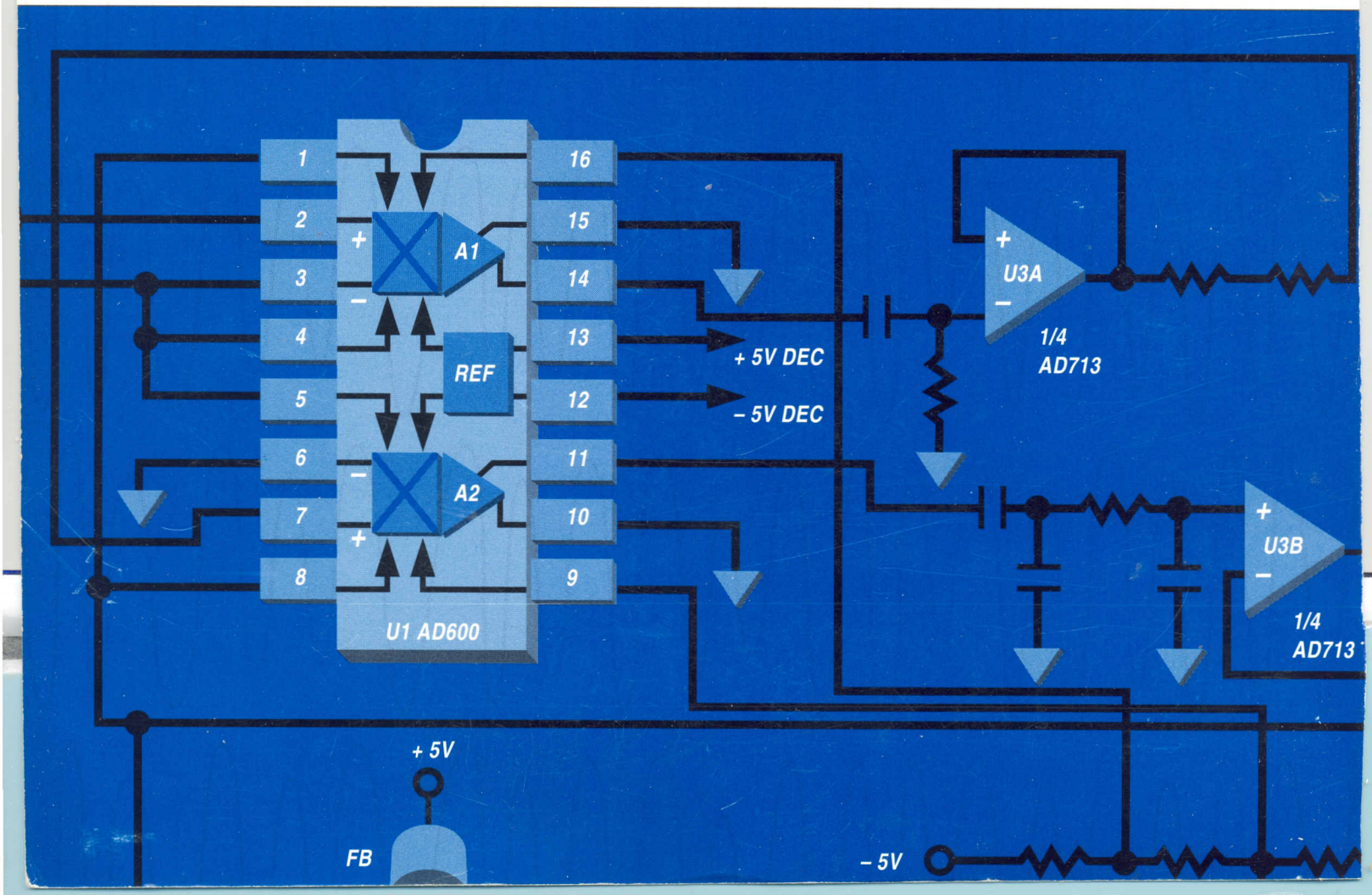
ANALOG DEVICES



ANALOG DEVICES

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1992 AMPLIFIER APPLICATIONS GUIDE

First Printing Errata Sheet



1992 Amplifier Applications Guide
First Printing Errata Sheet-August, 1992

Front Cover, Top diagram: Remove short between pin 6 and pin 2 of AD843 and replace with a capacitor.

Front Cover, Bottom diagram: Pin 13 of U2 should be labeled: +5V.

Back Cover, Top diagram: Remove short between pin 6 and pin 2. Replace with a capacitor. Reverse positions of 2.2μF and 0.1μF capacitors.

Back Cover, Bottom diagram: Reverse the polarity of the inputs to U3A.

Copyright Page: "Herin" should be spelled "Herein"

Outline section: Under SECTION II outline, under the third bullet point, add "Monolithic Thermocouple Amplifiers" after "Thermistors".

Outline section: Under SECTION XI outline, change "Effect" to "Affect".

Figure 1.1: Add OP-295 to list of Low Power, Single Supply Amplifiers

Figure 1.2: Change OP27 to OP275, Add OP27 between AD624 and AD829

Figure 1.4: Add label "VIDEO" to section below "PROFESSIONAL VIDEO"

Figure 1.6: Add AD844 between OP-160 and AD811 in middle of diagram.

Figure 1.7: Add OP-275 dot above AD811 dot between AD9630 and AD9620

Outline Page, Section II: add "Monolithic Thermocouple Amplifiers" after Thermistors in outline.

Figure 2.10: Pin 3 of second OP-177 should go to ground.

Figure 2.21: Make "-" sign on first op amp horizontal.

Figure 2.22: Remove "1%" label from 499Ω resistor and 27.4kΩ resistor.

Figure 2.23: Remove the erroneous "10" below Vout. Remove "1%" label from 475Ω resistor.

Figure 2.26: Second column total error should be 116, third column should be 112, and fourth column should be 280.

Figure 2.29: Re-label S1, S2, S3, S4 as SW1, SW2, SW3, SW4 to be consistent with the text.

Figure 2.31: Add comment ..."and low peak-to-peak voltage noise in 0.1 to 10Hz bandwidth" to first bullet point.

Figure 2.34: Change 1000 to 100 on horizontal scale of left-hand graph of voltage noise.

Figure 2.35: Remove "Ultra" from title and first bullet point. Change Hz in first and third bullet points to $\sqrt{\text{Hz}}$.

Figure 2.38: Change title to "Choosing Instrumentation Amplifiers".

Page 2.28: In second paragraph, change "Bifet" to "Super-Beta".

Figure 2.42: Title of first column should be "Gain Accuracy". Title of fourth column should be: CMRR dB @ 60Hz. In title of fifth column change hZ to Hz.

Figure 2.43: For Single Supply chart, change CMRR dB to CMRR dB @60Hz. In "Input-Overvoltage Protected" chart, add AD626 with +54V Max Input Voltage.

Figure 2.44: Change Gain Accuracy of AD626 to 0.5. Change title of last column to CMRR, dB @ 60Hz.

Figure 2.45: Remove AD526 from selection table! It is not an instrumentation amplifier!!!

Figure 2.47: Change fifth bullet point to show +5 to $\pm$15V specified supply range.

Figure 2.51: Add G=1000, and "Scope Synchronized to Chopper Frequency" to diagram.

Figure 2.52: Add "Scope Unsynchronized" to diagram.

Figure 2.53: Add "Scope Unsynchronized" to diagram.

Page 2.40: First column, line 12 should read: "When compared to other temperature sensors, thermocouples are quite linear. However, their low....."

Figure 2.60: AD592 should be shown as a current source.

Figure 2.61: AD592 should be shown as a current source. Label amplifiers from left to right: A1, A2, A3 since this is mentioned in text.

Page 2.59: In first paragraph, 0.5°C/mW should be 0.5°C/W.

Figure 2.67: "Guage" in title should be spelled "Gauge".

Figure 2.68: Drawn to show Kelvin connection better.

Page 2.68 2.69: Add section titled: "Monolithic Thermocouple Amplifiers with Cold Junction Compensation: The AD594/AD595/AD596/AD597. This is an extraction of the introductory remarks on the respective data sheets. **Complete text is attached to this Errata sheet.**

Figure 3.2: Ideal diode should be in parallel with photo current generator not in series.

Figure 3.9: Label the IC pin connect to the standoff as "Bent Lead".

Figure 3.16: Add pin numbers corresponding to AD645 pinouts. Show main amplifier connected to collector of current mirror. Output of amplifier goes to pin 6. **(Diagram attached to this errata sheet).**

Figure 3.18: Delete resistor network connected to bottom of 1000MΩ summing resistor. Connect bottom of 1000MΩ resistor to a 100Ω resistor connected to ground. Connect a 1MΩ resistor to the junction of the 100Ω and 1000MΩ resistor. The other end of the 1MΩ resistor should go to the wiper of a 100kΩ pot which is connected between + and - 15V. **(Diagram attached to this errata sheet)**.

Figure 3.19: Delete Rp. Change 1000MΩ resistor to Rp = 15.4MΩ. Connect bottom of 15.4MΩ resistor to a 100Ω resistor which goes to ground. Connect a 1MΩ resistor to the junction of the 100MΩ and 15.4MΩ resistor. The other end of the 1MΩ resistor should go to the wiper of a 100kΩ pot which is connected between + and - 15V. **(Diagram attached to this errata sheet.)**

Figure 3.21: Same correction as Figure 3.19.
(Diagram attached to this errata sheet).

Figure 3.24: Same correction as Figure 3.19.
(Diagram attached to this errata sheet).

Figure 3.28: In diagram, C2 should be 50pF, not 10pF.

Figure 3.30: "In^{+}" in second term of long equation for Von should be squared.

Figure 3.37: Same correction as Figure 3.19.
(Diagram attached to this errata sheet.)

Page 3.31: Second column, lines 5 and 6: "6" should be "5.6".
Second column, line 13, $\sqrt{2}$ should be $\sqrt{10}$.
Figure 3.41: R4 should be 900kΩ. Equation on left-hand side should read:

WITH "T" NETWORK: $\frac{1}{\beta_T} = (1 + \frac{100}{1000})(1 + \frac{900}{100})$

$$= (1.1)(10) = 11.1$$

$$\frac{1/\beta_T}{1/\beta_1} = 5.6$$

Figure 3.48: Change third bullet point to read: "Minimize op amp input capacitance: Cin $\leq$ Cd."

Page 4.1: Add John Wynne, Faisal Ansari, Joe Buxton, Adolfo Garcia, and Steve Sockolov to the list of authors.

Figure 4.4: Reverse the polarity of the inputs of A2.

Page 4.5: Column 2, line 23: Change "goes" to "go".

Page 4.9: Last sentence: Change "control" to "compression".

Page 4.10: Last paragraph: "N-Channel" should be "P-Channel".

Figure 4.10: Add (A) to left-hand drawing and (B) to right-hand drawing.

Page 4.13: First column, line 11: Change "4.8(b)" to "4.10(b)".

Page 4.13: Second paragraph: "Figure 4.8(b)" should be "Figure 4.10(b)".

Figure 4.11: Delete "-5V". Connect bottom of this 10kΩ resistor to V- of the op amp.

Figure 4.15: Change 121kΩ resistor to 12.1kΩ.

Figure 4.16: Change offset voltage to 300μV max, Change supply current to 300μA max, change gain-bandwidth product to 85kHz.

Figure 4.17: Reverse the polarity of the inputs to the OP-295.

Figure 4.18: Reverse the polarity of the inputs to the OP-295.

Page 4.21: Upper right-hand paragraph should read "The amplifier is frequency compensated so that it can drive a 1μF to 10μF output capacitance without oscillation."

Page 4.21: Middle right-hand paragraph should read; "The OP-90/OP-290/OP-490 comes close to ....."

Figure 4.19: Change specs on OP-295 as follows: Max Vos = 300μV, Max Is/Amplifier = 150μA.

Add data for dual OP-213 into table as follows

Dual OP-213 150μV 0.2μV/C 2mA

Figure 4.24: Reverse polarity of the inputs of the OP-27.

Page 4.31: Second column , line 1 should read: "...a few inches of conductor can have...."

Page 4.34: Add Reference: Fair-Rite Products, P.O. Box J, Wallkill, NY, 12589

Figure 4.31: Top trace is 100mV/div., Bottom trace is 5mV/div.

Figure 5.4: Invert the polarity of the inputs to U1.

Page 5.10: Second column, line 5: Change R4 to R2.

Figure 5.9: In diagram, change R3 to R1, R4 to R2, R1 to R3, and R2 to R4.
In table, change R1,R2 to R1,R3 and R3,R4 to R2,R4. Change 12kΩ under R2,R4 for SSM-2143 to 6kΩ.

Figure 5.16: Change arrows to grounds.

Figure 5.18: Change equation for Gain to GAIN = 1 + R1/R2

Page 5.22: Add Reference 3: Aavid Engineering Co., P.O. Box 400, Laconia, NH, 03247.

Page 6.19: Line 15 should read: ..." Furthermore, its success will still be limited by the number of parts that.....".

Page 6.21: Second column, line 15 should read: ..."They exist between....."

Figure 7.8: Change SFDR to 110 dBc.

Page 7.7: "Figure 710" in right-hand column should be "Figure 7.10".

Page 7.12: Last paragraph, third sentence should read: "The percentage change in closed loop gain, ΔA_{cl}, for a percentage change in open loop gain, ΔA, is approximately $\Delta A/|A_o\beta|$, where A_o is the nominal dc open loop gain at room temperature."

Figure 7.16: Change second bullet point to read: "Percentage Change in Open Loop Gain", and fifth bullet point to read: "Percentage Change in Closed Loop Gain".

Figure 7.27: Substitute curves from Figure 8.20. Table for Gain, BW, and Product remains the same.

Figure 7.85: Change 5.1kΩ resistors to 5.62kΩ. Change top 16kΩ resistor to 5.76kΩ. Parallel it with a 100pF capacitor. Change bottom 16kΩ resistor to 5.49kΩ. Parallel it with a 100pF capacitor. Change 270Ω resistors to 51Ω. Change differentially connected 0.01μF capacitor to 0.0047μF. Eliminate 120Ω resistors to ground. Label top input to AD1879 "-IN" and bottom input "+IN". **(Diagram attached to errata sheet).**

Page 7.61: First column: Change last sentence to read: "The differentially connected 0.0047μF capacitor supplies most of the differential-mode transient currents, while the 0.01μF capacitors connected to ground absorb spike currents which are common mode. The 51Ω series....."

Figure 8.20: First graph should be INVERTING FREQUENCY RESPONSE. Settling time photo should be the same as Figure 7.32.

Page 8.29: First column, line 19: "bully" should be "bulky".

Figure 8.36: R2 in the denominator of the equation for I_L should be changed to R4.

Figure 8.37: Reverse the input polarities for both AD9617s.

Figure 8.42: Show termination resistor between pins 1 and 2 of AD830. Do not connect to ground at AD830.

Page 9.19: Right-hand side of Equation 9.2.5 should be positive.

Figure 9.2.6: Change title to VCA WITH SQUARE LAW GAIN CONTROL USING THE AD539 MULTIPLIER. Input range should be 50dB, not 55dB.

Figure 9.2.11: Change "R_F" to "R8 = R9"

Page 9.38: Line 5 in first paragraph under 9.2.5: C1 should be C4.

Figure 9.2.25: First label on horizontal axis should be 0.1.

Figure 9.2.26: Extend horizontal axis back one decade to 100μV. The graph is basically flat back to this point.

Figure 9.2.28: Change label on vertical axis to mV RMS

Figure 9.2.29: Change vertical axis scale to Volts.

Page 9.51: Line 5 under 9.2.9: "increases" should be "decreases".

Page 9.71: Second paragraph, line 5: +100mV should be -100mV.

Page 9.72: The right-hand term of Eq. 9.3.24 should be negative. The phrase:"that is, a small *forward*-bias on the collector." should immediately follow the equation.

Page 9.82: In Eq. 9.4.13 the term"A^{N-1}" in the last fraction should be moved to the left under $E\sqrt{A}$.

Page 9.86: In first equation, N-2 should be N-1. In Eq. 9.4.20, N-2 should be N-1. In Eq. 9.4.22, N-3 should be N-2. In the sentence between Eq. 9.4.22 and Eq. 9.4.23, 6.6438 should be 6.6435.

Figure 9.4.9: Delete "(NOT USED)" from output of last stage.

Figure 9.4.11: Add load resistor R_Y to ground.

Page 9.91: In Eq. 9.4.39, and 9.4.40 change + to - after the number "1".

Page 9.100: Change title to "Some Aspects of Log-Amps Based on Bipolar Differential Stages".

Page 10.3: Second column, line 7: "cascade" should be "cascode".

Page 10.15: Second column, line 9: Change generation to degeneration.

Page 10.27: First column, line 5: change "transistor" to "resistor".

Figure 10.34: Change "BIFET" to "BIFET and PNP Input" for both bullet points.

Section 11 Title Sheet: Change "Effect" to "Affect"

Figure 11.7: For AD712, Change series resistor to 14kΩ and noise to $22nV/\sqrt{Hz}$

Page 11.11: In title, change "Effect" to "Affect".

Page 11.23: Last line of second column should read: "$1nV/\sqrt{Hz}$ in the best low noise op amps."

Page 11.26: First line should read: "If the impedance is resistive there is a..."

Figure 11.34: In equation F, change non-inverting to inverting.

Figure 11.35: RTI NOISE should be $nV/\sqrt{Hz}$.

Figure 11.36: Right-hand top graph should be for Rs = 10kΩ.

Figure 11.56: Allow space between "Conduction" and "Electrostatic", and space between "Induction" and "Electromagnetic".

Figure 11.58: Add low and high frequency decoupling capacitors to left-hand node. Remove connecting line between A and B in right-hand diagram.

Page 11.56: First column, line 15: insert the word "formula" after the word "reactance".

Page 11.58: Second column: Change last sentence to read: "If sensitive circuitry is located close to a switching supply, its performance may be devastated - if it is further away problems will be minimized. "

Figure 12.28: Insert space between "Mount" and "adhesive" on next to last line.

Page 12.26: Change Wainwright address to: Wainwright Instruments Inc., 7770 Regents Rd., #113, Suite 371, San Diego, CA 92122, Tel: 619-558-1057. Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-2245, Fax: +49-8152-5174.

Page 13.6: Second column, line 16: change gm5 and C5 to gm2 and C4.

Figure 13.7: C4 in the "Noiseless" column should be $159x10^{-9}F$.

Page 13.10: Second column, line 17: Change "By" to "because".

Page 13.28: Change last sentence to read: "The complete list of all 300 models on the "Release F, 4/92 version of the diskette is shown in Figure 13.30.

Figure 13.30: Replace with Release F listing which contains 300 macromodels. **(Figure attached to errata sheet).**

Index, Page 19: Add "monolithic thermocouple amplifiers, II.68-69"

Analog Devices Parts Index, Page 22: Add: AD594, AD595, AD596, AD597, pp. II.68-69.

(Put at end of Section II)

MONOLITHIC THERMOCOUPLE AMPLIFIERS WITH COLD JUNCTION COMPENSATION: THE AD594/AD595/AD596/AD597

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby converting it into a stand-alone Celsius transducer with a low-impedance output voltage.

The AD594/AD595 includes a thermocouple failure alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.

The AD594/AD595 can be powered from a single ended supply (including +5V) and by including a negative supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will typically operate with a total supply current of 160μA, but is also capable of delivering in excess of ±5mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristic of type J (iron-constantan) thermocouples, and the AD595 is laser trimmed for type K (chromel-alumel) inputs. The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of two or three resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications. The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used from 0 to +50°C, and are available in 14-pin, hermetically sealed, sidebrazed ceramic DIPs as well as low cost cerdip packages.

The AD596/AD597 is a monolithic temperature set-point controller which has been optimized for use at elevated temperatures such as those found in oven control applications. The device cold junction compensates and amplifies a type J or K thermocouple input to derive an internal signal proportional to temperature. The AD596/AD597 can be configured to provide a voltage output (10mV/°C) directly from a type J or K thermocouple signal. The device is packaged in a reliability qualified, cost effective 10-pin metal can and is trimmed to operate over an ambient temperature range from +25°C to +100°C.

Operation over an extended ambient temperature range is possible with slightly reduced accuracy. The AD596 will amplify thermocouple signals covering the entire -200°C to +760°C temperature range recommended for type J thermocouples while the AD597 can accommodate -200°C to +1250°C type K inputs. The AD596/AD597 has a calibration accuracy of ±4°C at an ambient temperature of 60°C and an ambient temperature stability specification of 0.05°C/°C from +25°C to +100°C.

BiFET OP AMP SIMPLIFIED INPUT CIRCUIT

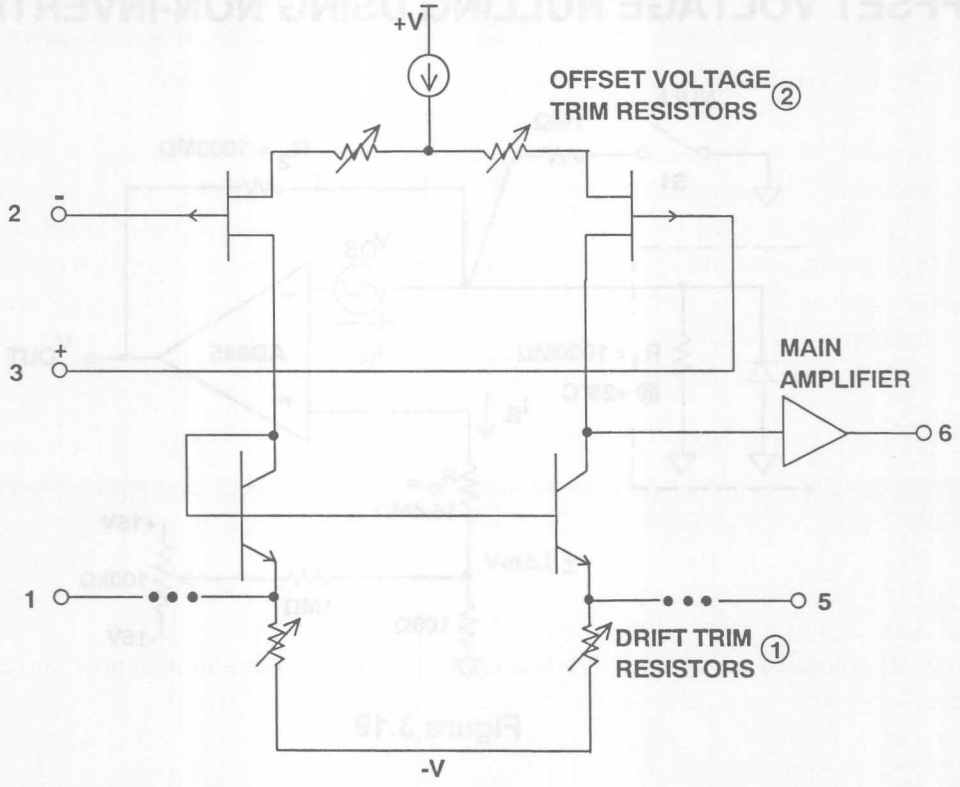


Figure 3.16

OFFSET VOLTAGE NULLING USING INVERTING INPUT

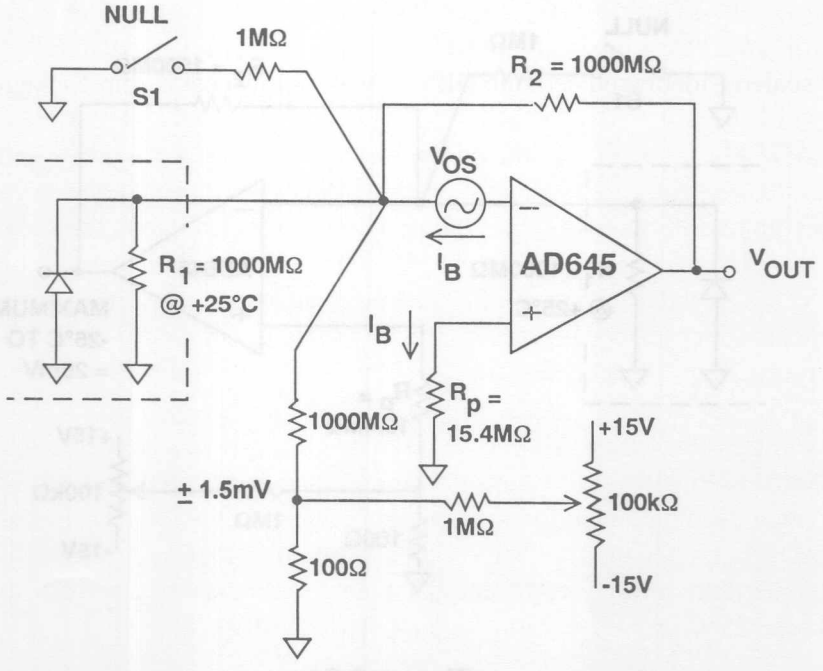


Figure 3.18

OFFSET VOLTAGE NULLING USING NON-INVERTING INPUT

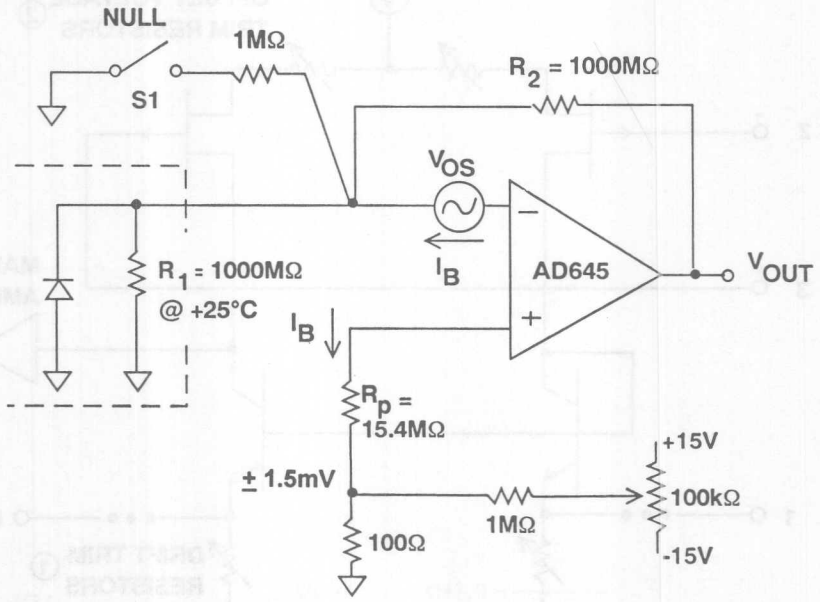


Figure 3.19

FINAL DC DESIGN FOR PHOTODIODE PREAMP

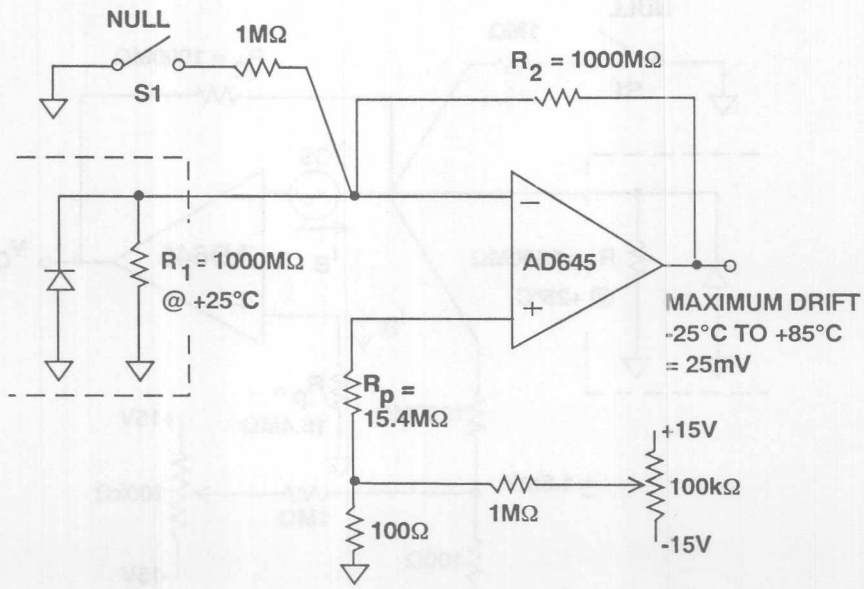


Figure 3.21

REACTIVE PORTION OF PHOTODIODE CIRCUIT

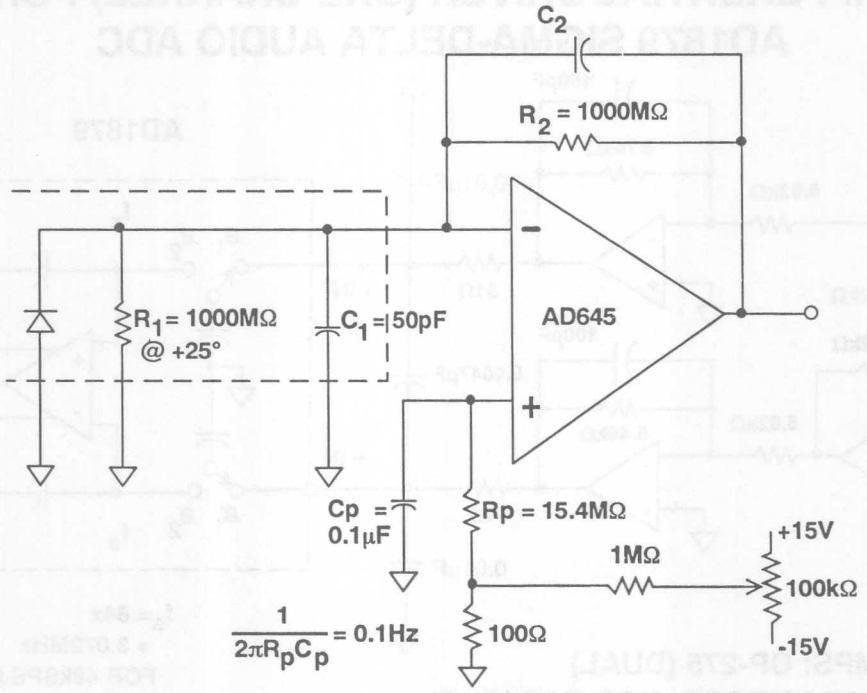


Figure 3.24

OPTIMIZED PHOTODIODE PREAMP

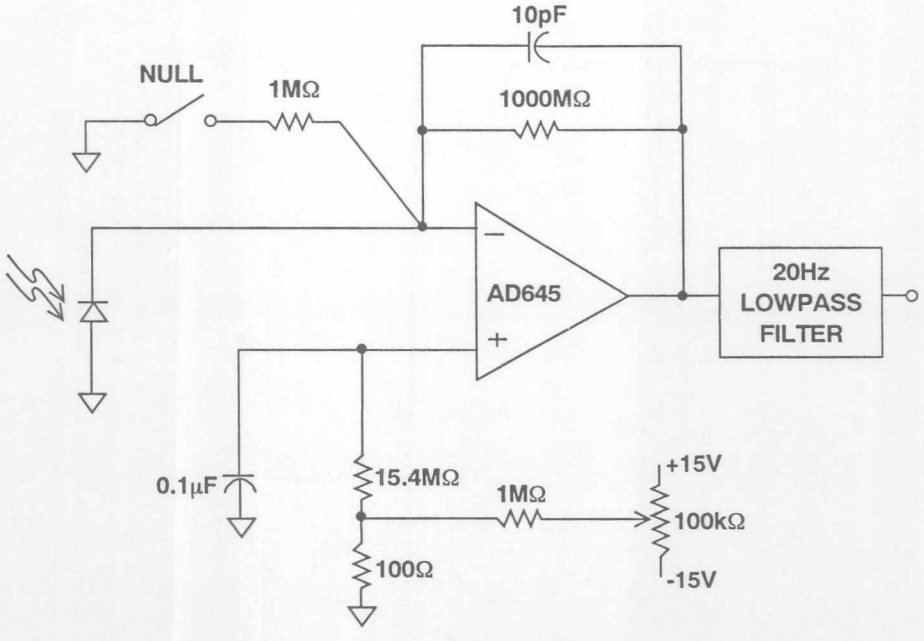
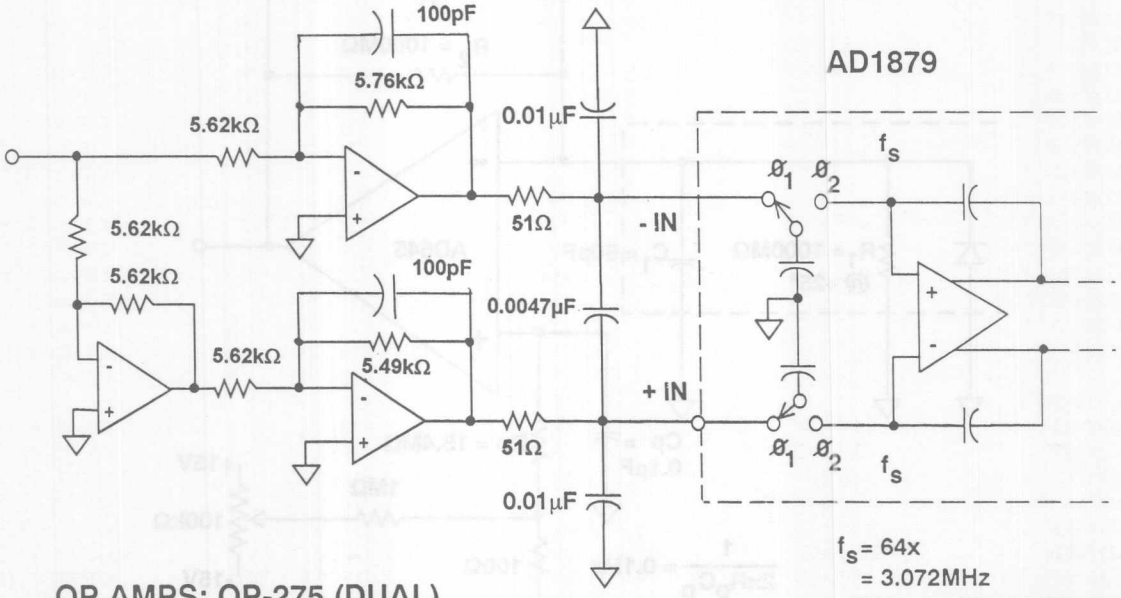


Figure 3.37

DIFFERENTIAL DRIVER (ONE CHANNEL) FOR AD1879 SIGMA-DELTA AUDIO ADC



OP AMPS: OP-275 (DUAL)
ALL CAPACITORS: NPO-CERAMIC

Figure 7.85

AD624A
AD624B
AD624C
AD624S
AD630 *
AD630A *
AD630B *
AD630J *
AD630K *
AD630S *
AD645 *(N)
AD645A *(N)
AD645B *(N)
AD645J *(N)
AD645K *(N)
AD645S *(N)
AD704
AD704A
AD704B
AD704J
AD704K
AD704T
AD705
AD705A
AD705B
AD705J
AD705K
AD705T
AD706
AD706A
AD706B
AD706J
AD706K
AD706T
AD711
AD711A
AD711B
AD711C
AD711J
AD711K
AD711S
AD711T
AD712 *(N)
AD712A *(N)
AD712B *(N)
AD712C *(N)
AD712J *(N)
AD712K *(N)
AD712S *(N)
AD712T *(N)
AD713
AD713A
AD713B
AD713J
AD713K
AD713S
AD713T
AD734
AD734A *
AD743 *(N)
AD743A *(N)
AD743B *(N)
AD743J *(N)
AD743K *(N)
AD743S *(N)
AD744
AD744A
AD744B
AD744C
AD744J
AD744K
AD744S
AD744T
AD745 *(N)
AD745A *(N)
AD745B *(N)
AD745J *(N)
AD745K *(N)
AD745S *(N)
AD746
AD746A
AD746B
AD746J
AD746S
AD811
AD829
AD829A
AD829J
AD829S
AD840
AD840J
AD840K
AD840S
AD843 *
AD843A *
AD843B *
AD843J *
AD843K *
AD843S *
AD844
AD844A
AD844B
AD844S
AD845
AD845A
AD845B
AD845J
AD845K
AD845S
AD846
AD846A
AD846B
AD846S
AD847
AD847A
AD847J
AD847S
AD848J
AD848S
AD9617
AD9618
AD9630
AMP01
AMP02
MAT02
MAT03
MAT04
OP160
OP160A
OP160F
OP160G
OP177 (N)
OP177A (N)
OP177B (N)
OP177E (N)
OP177F (N)
OP177G (N)
OP200
OP200A
OP200E
OP200F
OP200G
OP20
OP20B
OP20C
OP20F
OP20G
OP20H
OP215
OP215A
OP215B
OP215C
OP215E
OP215F
OP215G
OP21
OP21A
OP21E
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OP220
OP220A
OP220C
OP220E
OP220F
OP220G
OP221
OP221A
OP221B
OP221C
OP221E
OP221G
OP249
OP249A
OP249G
OP260
OP27 (N)
OP27A (N)
OP27B (N)
OP27C (N)
OP27E (N)
OP27F (N)
OP27G (N)
OP275 *(N)
OP275G *(N)
OP282 *
OP282G *
OP290
OP290A
OP290E
OP290F
OP290G
OP297
OP297A
OP297E
OP297F
OP297G
OP37 (N)
OP37A (N)
OP37B (N)
OP37C (N)
OP37E (N)
OP37F (N)
OP37G (N)
OP400
OP400A
OP400E
OP400F
OP400G
OP400H
OP41
OP41A
OP41B
OP41E
OP41F
OP41G
OP420
OP420B
OP420C
OP420F
OP420G
OP420H
OP421
OP421B
OP421C
OP421F
OP421G
OP421H
OP42
OP42A
OP42E
OP42F
OP43B
OP43E
OP43F
OP43G
OP44
OP470
OP482 *
OP482G *
OP490
OP490A
OP490E
OP490F
OP490G
OP497
OP497A
OP497B
OP497C
OP497F
OP497G
OP61
OP64
OP77 (N)
OP77A (N)
OP77B (N)
OP77E (N)
OP77F (N)
OP77G (N)
OP90
OP90A
OP90E
OP90F
OP90G
OP97
OP97A *
OP97E *
OP97F *
PM1012
REF01 (N)
REF01A (N)
REF01C (N)
REF01E (N)
REF01H (N)
REF02 (N)
REF02A (N)
REF02C (N)
REF02D (N)
REF02E (N)
REF02H (N)
REF05 (N)
REF05A (N)
REF05B (N)
REF10 (N)
REF10A (N)
REF10B (N)
SSM2131
SSM2210
SSM2220

* Indicates new model since release E, 10/91
(N) Indicates noise model

Figure 13.30

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ANALOG DEVICES TECHNICAL REFERENCE BOOKS

PUBLISHED BY PRENTICE HALL

Analog-Digital Conversion Handbook
Digital Signal Processing Applications Using the ADSP-2100 Family
Digital SIgnal Processing in VLSI
DSP Laboratory Experiments Using the ADSP-2101
ADSP-2100 Family User's Manual

PUBLISHED BY ANALOG DEVICES

Amplifier Applications Guide
Mixed Signal Design Seminar Notes
High-Speed Design Seminar Notes
Nonlinear Circuits Handbook
Transducer Interfacing Handbook
Synchro & Resolver Conversion
THE BEST OF *Analog Dialogue,* 1967-1991

AMPLIFIER APPLICATIONS GUIDE



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1992

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INTRODUCTION

SECTION I

INTRODUCTION

SCOTT WURCER

Over the last 25 years, the IC op amp has evolved into a large array of both general purpose and application-specific devices. Although Analog Devices has an amplifier to fit almost any application, the task of selecting the correct amplifier is frequently difficult. The material in this seminar is arranged to highlight a number of specific and different op amp applications in a manner which combines theory with practice. By examining these actual real world state-of-the-art applications, the user will gain insight which will be invaluable in designing systems requiring amplifiers.

The concept of using an op amp as a universal analog computing element predates the integrated circuit by a number of years. Philbrick and others realized the usefulness of the op amp building block approach to analog computing. The three fundamental analog computing functions of integration, differentiation, and multiplication (gain) are easily realized using op amps with passive feedback. Op amps made with vacuum tubes were used with some popularity in large analog computing mainframes. The advent of the planar IC process brought with it the same move to integration for analog functions as for digital functions.

The first truly successful IC op amp was the μA709 introduced more than 25 years ago. It was followed by the internally compensated μA741 and the LM101. These early products marked the beginning of the IC op amp era. Analog Devices and many others have manufactured all of these early devices. The μA741 and the LM101 are still commonly used today. It was also during these early days that the first IC instrumentation amplifier was introduced, the AD520. Analog Devices has continued to maintain a leadership position in instrumentation amplifiers with the industry standard AD524 family and more recently with the AD620 and AD621.

IC designers soon realized that the inherent matching of devices on the same die could be exploited to produce precision amplifiers. This led to the earliest high precision op amps, the OP-07 and the OP-27. These products, however, achieved only modest ac performance. The basic μA741 circuit in BiFET (Bipolar/FET) technology added an improvement in speed at the expense of dc performance.

Analog Devices has been successful in narrowing the performance gap between FET and Bipolar technology by pioneering laser trim technology to provide less than 1μV/°C drift in general purpose BiFET and electrometer amplifiers. The AD549 and AD645 have under one picoampere input bias current and are fabricated on a junction isolated process.

Around 1971, dielectrically-isolated complementary-bipolar processes became available to serve the high speed market. The inherent expense and manufacturing difficulty associated with this process prevented it from becoming universally accepted by IC manufactures of high speed products. Junction isolated complementary-bipolar processes, including Analog Devices' proprietary CB process, have brought both low cost and high performance to high speed amplifiers. A large number of products designed using this technology will be discussed in this seminar, including some recent additions such as the low-power high speed quad OP-467 and the first attempt to combine high speed with true dc precision, the AD797.

THE EVOLUTION OF IC OP AMPS

- Vacuum Tubes
- Analog Computers (Philbrick)
- Planar IC Process
- μA709, μA741, LM101 Op Amps
- Instrumentation Amplifiers: AD520 → AD524 Family → AD620, AD621
- Precision Op Amps: OP-07, OP-27
- Low Bias Current Bipolar/FET Processes (BiFET): AD549 → AD645
- Low Power, Single Supply: OP-90, OP-290, OP-490
- High Speed Complementatry Bipolar Processes → AD840-Series, OP-467 (Quad), AD797

Figure 1.1

The trends toward higher speeds and greater levels of integration have significantly reduced the role of discrete logic gates in large digital system designs. In this age of Large Scale Integration (LSI) and Very Large Scale Integration (VLSI), one might indeed question the reason for the continued existence and proliferation of more and more varieties of discrete IC amplifiers. The answer lies in the variety of signals which comprise the world of analog signal processing and the increased accuracy requirements placed on both precision and high speed measurements.

For example, accurate measurements in weigh-scale bridges require amplifier accuracies of less than 1mV at impedance levels of hundreds of ohms. Detecting picoamperes of photodiode current or measuring the output of high impedance charge amplifiers requires extremely low bias current and low noise amplifiers. Accurate reproduction of wide bandwidth High Definition Television (HDTV) signals requires that differential gain and phase errors are minimal and that the bandwidth remains flat within 0.1dB up to 30MHz.

Because the amplifier is a fundamental front-end signal conditioning element in most real world signal processing applications, its performance should exceed that of the overall system. It is the exploitation of opportunities for increased system performance in a wide variety of real world signal processing applications that explains the continued popularity of the IC amplifier as a fundamental analog building block.

Offset voltage, bias current, and noise are the basic performance limitations in precision dc applications. Figure 1.2 groups a variety of amplifiers as a function of input bias current and input voltage noise. Figure 1.3 is a technology grouping as a function of input bias current and input offset voltage. Both of these figures show Analog Devices' position at the forefront of amplifier technology. Super-Beta technology fits into the technology profile well in terms of dc precision and low noise, and has allowed an expansion of instrumentation amplifier

offerings. The AD620 and AD621 are products which bring new levels of performance and functionality to this exacting market.

AMPLIFIER GROUPING: INPUT BIAS CURRENT, INPUT VOLTAGE NOISE

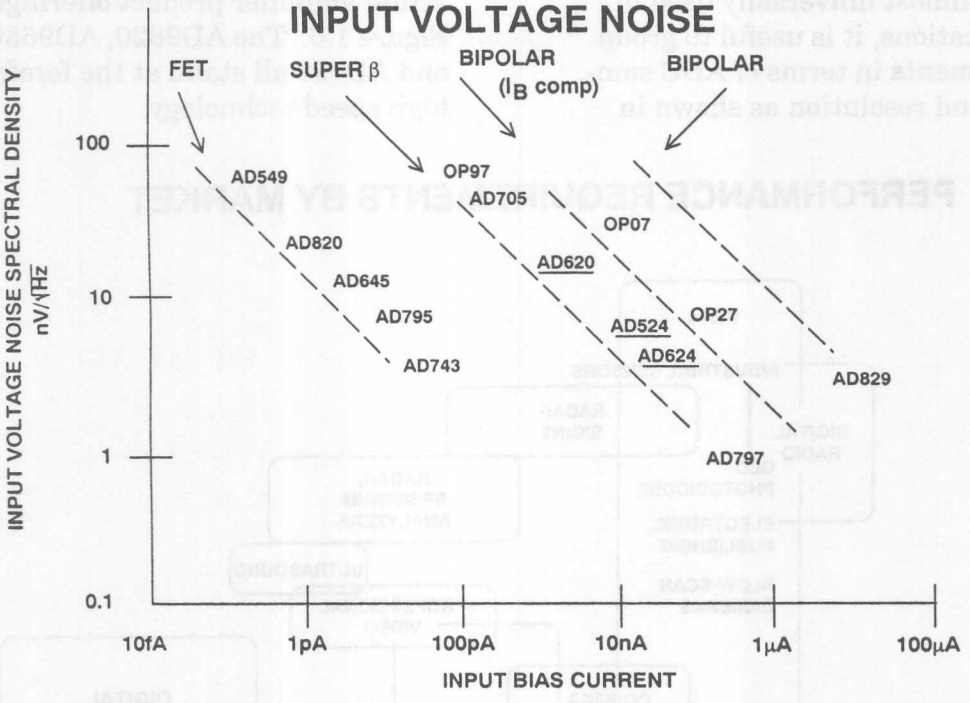


Figure 1.2

AMPLIFIER GROUPING: INPUT BIAS CURRENT, INPUT OFFSET VOLTAGE

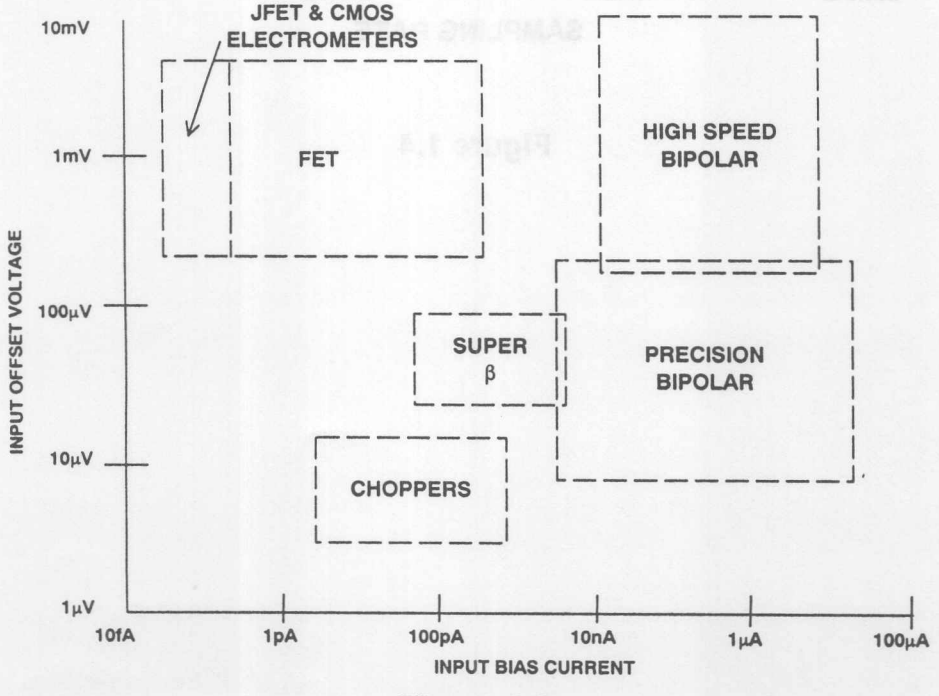


Figure 1.3

The high speed market has recently been the largest driver of amplifier process technology. Because digital techniques are almost universally used in these applications, it is useful to group the requirements in terms of ADC sampling rate and resolution as shown in Figure 1.4. The corresponding implementation of these requirements as a function of process is shown in Figure 1.5, and actual amplifier product offerings in Figure 1.6. The AD9620, AD9630, AD811, and AD797 all stand at the forefront of high speed technology.

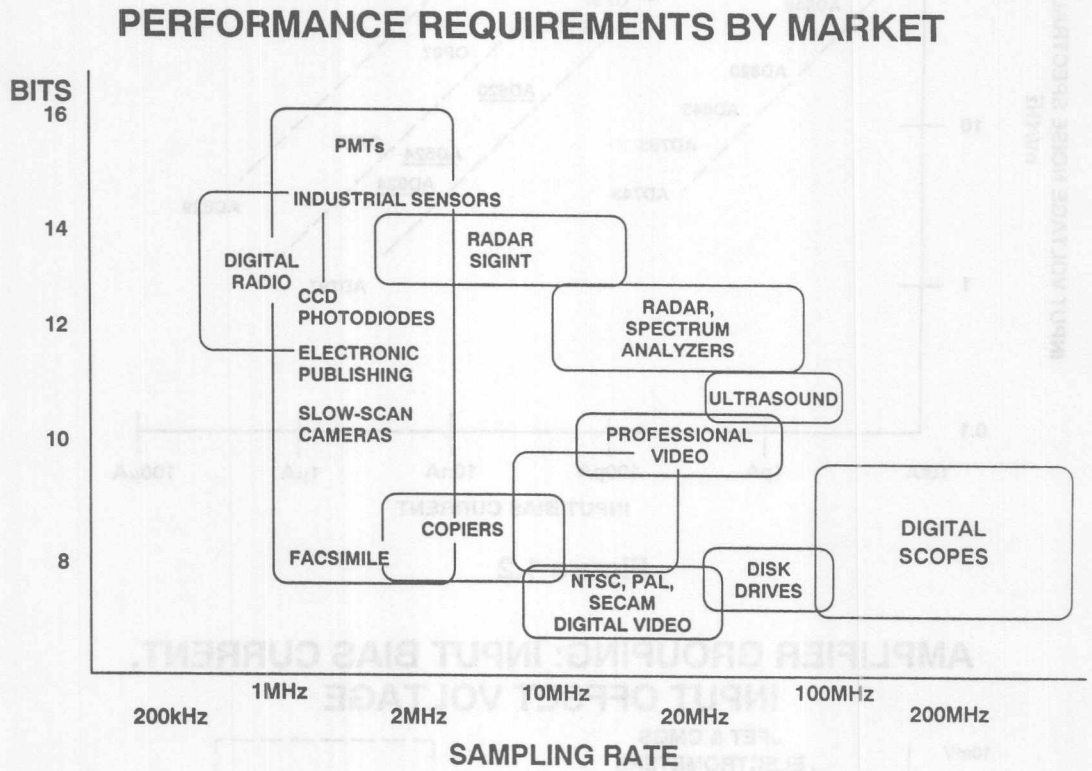


Figure 1.4

PROCESS CAPABILITIES AND DIRECTION BY MARKET

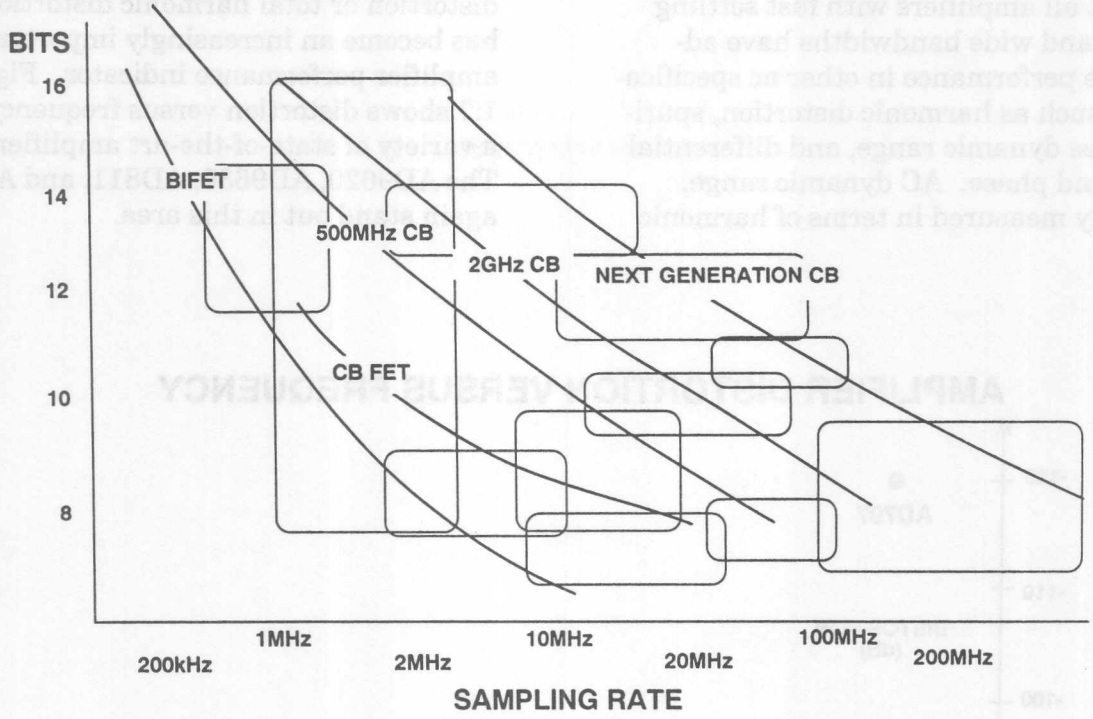


Figure 1.5

AMPLIFIERS BY MARKET

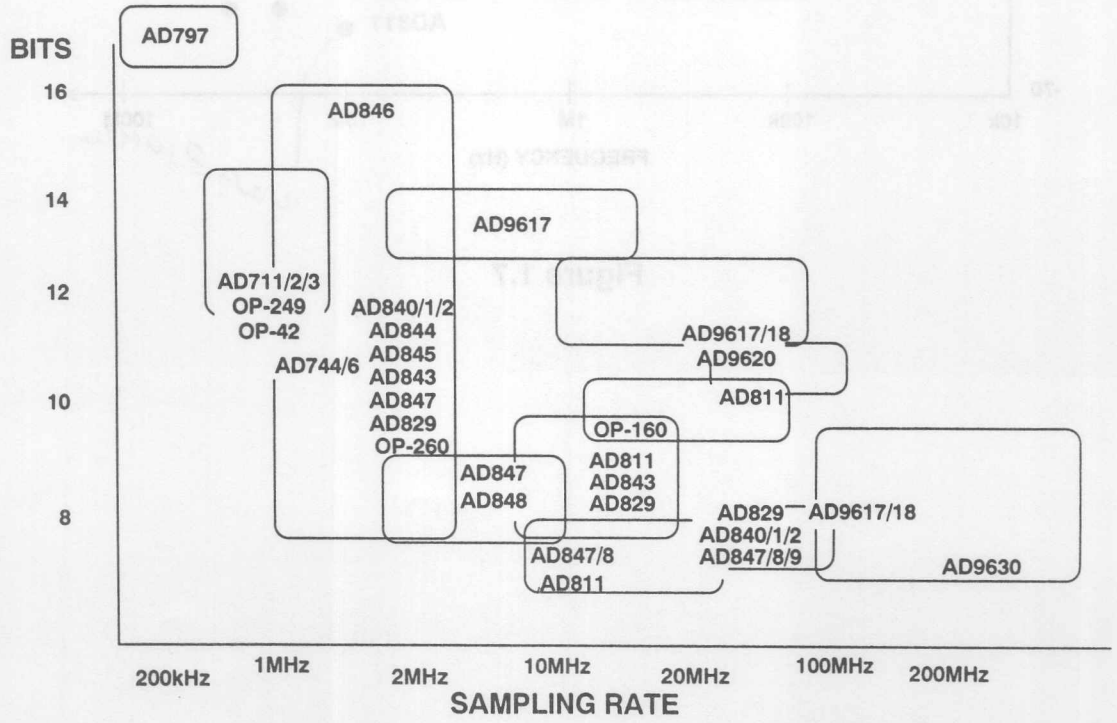


Figure 1.6

Not all amplifiers with fast settling times and wide bandwidths have adequate performance in other ac specifications such as harmonic distortion, spurious free dynamic range, and differential gain and phase. AC dynamic range, usually measured in terms of harmonic distortion or total harmonic distortion, has become an increasingly important amplifier performance indicator. Figure 1.7 shows distortion versus frequency for a variety of state-of-the-art amplifiers. The AD9620, AD9630, AD811, and AD797 again stand out in this area.

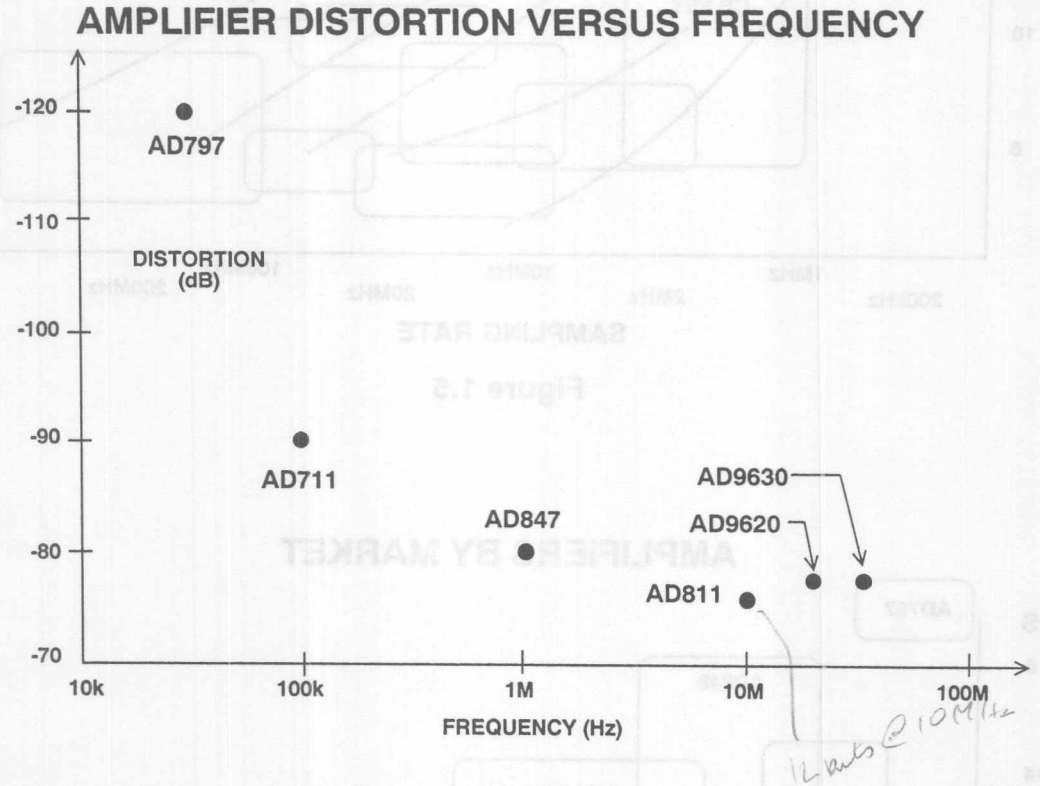


Figure 1.7

SECTION II
PRECISION TRANSDUCER INTERFACES

- Bridge Circuit Applications
- Bridge Amplifiers
- Signal Conditioning for Temperature Measurement: Thermocouples, Resistance Temperature Devices (RTDs), Thermistors

SECTION II

PRECISION TRANSDUCER INTERFACES

JAMES WONG, ADOLFO GARCIA

PRECISION BRIDGE INTERFACES

JAMES WONG

Because of the many physical variables involved, real world signal processing requires a wide variety of sensing elements. Most are based on resistance, capacitance, or voltage output (thermocouple) elements, thereby simplifying the interface to electronic measuring and processing equipment.

Resistive elements are the most common transducers. They are cost effective to manufacture and easy to interface with amplifier circuits. Furthermore, it is possible to integrate sensing elements directly on ICs. Resistive elements can be made sensitive to temperature, strain (by pressure or by flex), light signals. Using these basic elements, many complex physical phenomena can be measured; such as fluid or mass flow (by sensing the temperature difference between two calibrated resistances) and dew-point humidity (by measuring two different temperature points), etc.

These transducer elements' resistances can range from less than 100 Ω to several kΩ, depending on the transducer design and the physical environment to be measured. For example, RTDs (Resistance Temperature Devices) are typically 100 Ω. Thermistors are typically in the 3500 Ω range or higher. There are also high impedance piezoelectric or capacitance-modulating transducers whose impedances range from 10's to 100's of MΩ.

TYPICAL SENSING ELEMENTS FOR MEASURING REAL WORLD VARIABLES

- **Resistance Output (RTDs, Strain Gauges)**
- **Capacitance or Charge Output (Piezoelectric)**
- **Voltage Output (Thermocouples)**
- **Current Output (Photodiode Detectors)**
- **ALL ARE LOW LEVEL SIGNALS REQUIRING PRECISION LOW-NOISE AMPLIFICATION**

Figure 2.1

Most of these transducers produce very low level signals, and therefore high gain is necessary in order to get usable signal levels. Amplifying these signals with precision while maintaining low noise performance presents a significant design challenge. The following sections examine some of the important design tradeoffs involved.

BRIDGE AMPLIFIERS

A balanced bridge is one of the most useful circuits for sensing low level signals from a transducer. When applied properly, bridge amplifiers reproduce transducer signals accurately and reliably. Most bridges employ resistive elements, either for temperature sensing or for measuring the amount of strain from pressure or flex.

Figure 2.2 shows three commonly used bridge types. The single-element varying type is most suited for temperature sensing, such as an RTD (Resistance Temperature Device).

However, it produces the least amount of signal. The 2-element varying type produces twice the signal, which is significant for signals in the microvolt to millivolt range. It is the least popular of the three because the implementation of it in a transducer is more difficult. The all-element varying type produces the most signal for a given resistance change. Whatever the form, choosing the right bridge and amplifier configuration can minimize nonlinear behavior and simplify the design.

Bridge circuits are simple to use but can be difficult to optimize because the output signal is usually very small. The inherent high common-mode voltage of a balanced bridge also makes designing difficult. Designers must usually make tradeoffs between performance and cost. In circuits where microvolts of error are significant, the fewer components and the simpler the circuit, the better the design.

Bridge resistance varies over a wide range from as low as 100 Ω to 100's of kΩs or more. The resistance depends on the transducer design. Figure 2.3 shows some popular transducer sensors and their typical resistance ranges.

BASIC BRIDGE CONFIGURATIONS

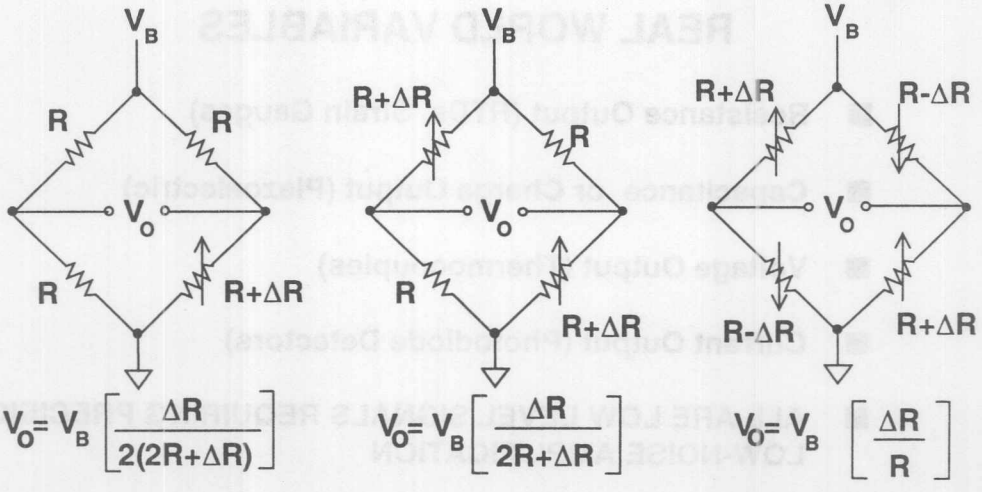


Figure 2.2

RESISTANCE OF POPULAR TRANSDUCERS

■ RTD (Resistance Temperature Device)	100Ω
■ Pressure transducers	350 - 3500Ω
■ Strain Gauge	120, 350, 3500Ω
■ Weigh-Scale load cells	350 - 3500Ω
■ Thermistor	100 Ω - 10MΩ
■ Relative humidity	100kΩ - 10MΩ

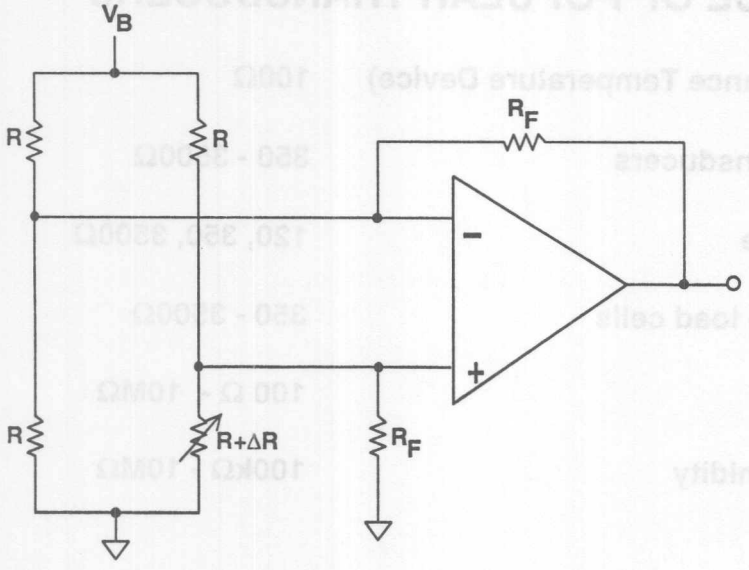
Figure 2.3

This section discusses the various bridge amplifier configurations, their relative linearity, and their advantages and disadvantages. The choice of the amplifier is also critical to the performance of the bridge.

SINGLE-ELEMENT VARYING SENSOR BRIDGES

Single-element sensors do not necessarily require a full bridge to produce usable signals. A variable resistance inside the feedback loop of an op amp produces usable signal. However, a bridge offers a convenient means to make more precise measurements of resistance change and provides a convenient means to level-shift. Figures 2.4 through 2.9 show different single-element varying bridge configurations, each having unique advantages and disadvantages.

SINGLE-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 1



Advantages:

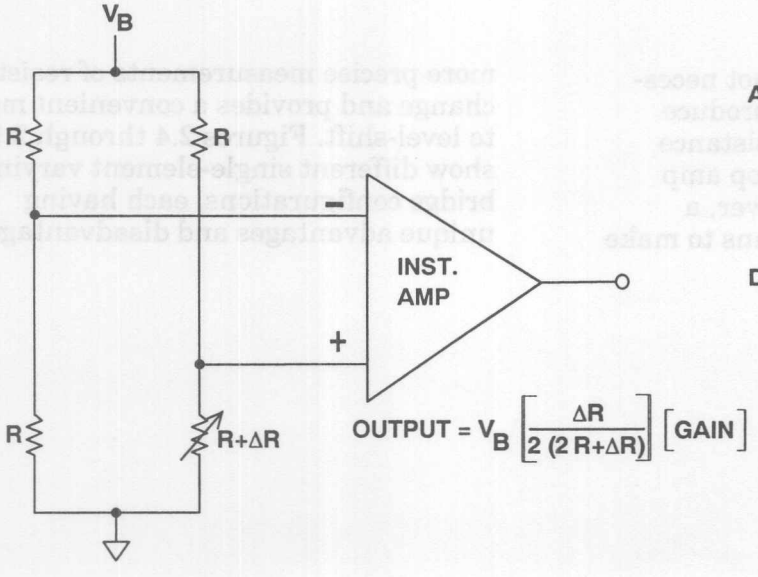
- No signal in = zero volts out
- Single supply operation
- Single op amp stage

Disadvantages:

- Nonlinear operation:
- 0.125% nonlinearity for 1% fullscale ΔR change
- Poor gain accuracy
- Unbalanced output R due to varying element

Figure 2.4

SINGLE-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 2



Advantages:

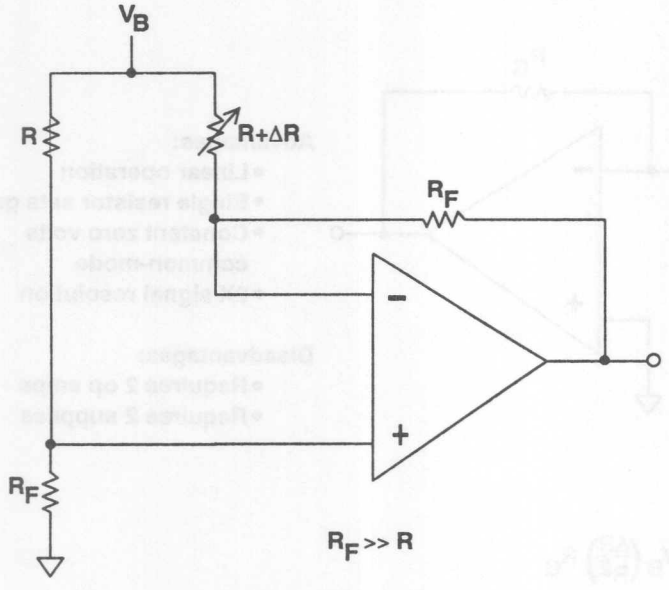
- Efficient design
- Only bridge R matching required
- Better gain accuracy

Disadvantages:

- Nonlinear operation
- 0.125% nonlinearity for 1% fullscale ΔR change

Figure 2.5

SINGLE-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 3

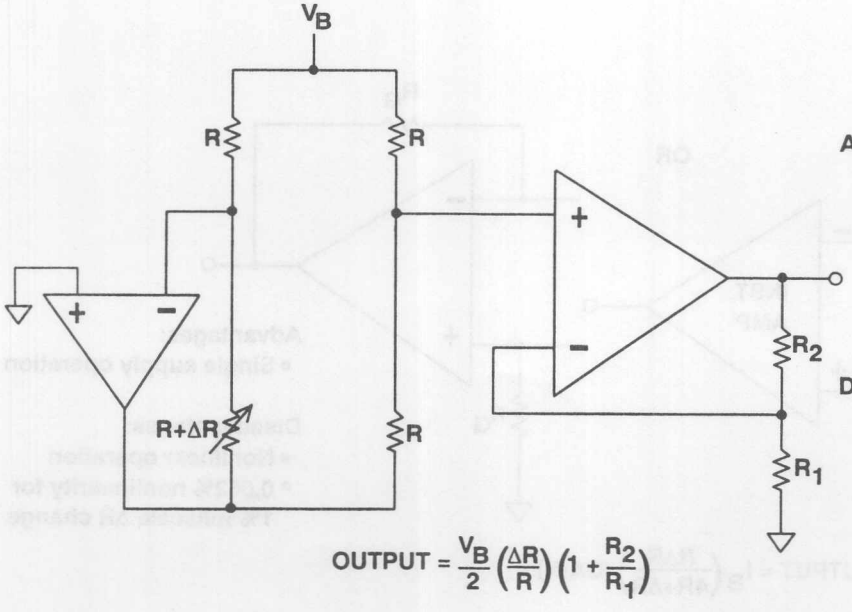


Advantages:
- Linear operation
- Low cost op amp
- No signal in = zero volts out
- Single supply

Disadvantages:
- Requires matching resistors
- Operates at high common-mode bridge voltage

Figure 2.6

SINGLE-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 4

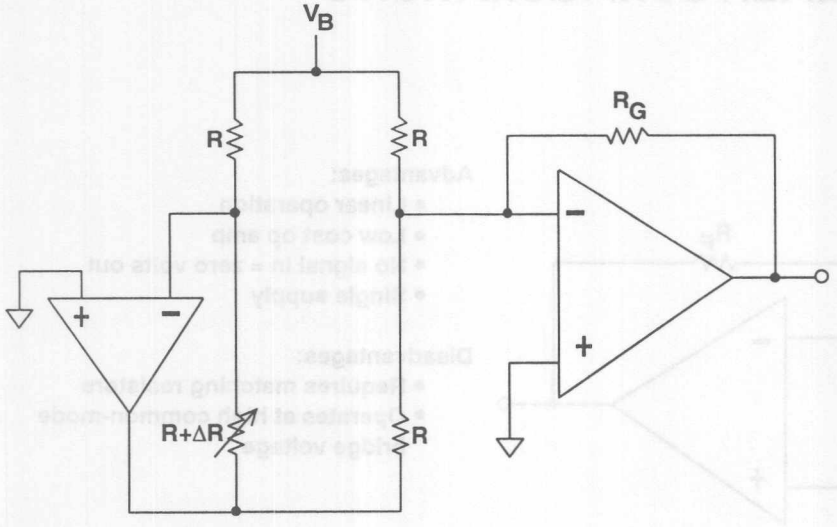


Advantages:
- Linear operation
- Uses low cost op amp
- No signal in = zero volts out
- Zero volts common-mode operation
- 2X signal resolution

Disadvantages:
- Requires 2 op amps
- Requires 2 supplies
- Requires R matching for bridge and gain

Figure 2.7

SINGLE-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 5



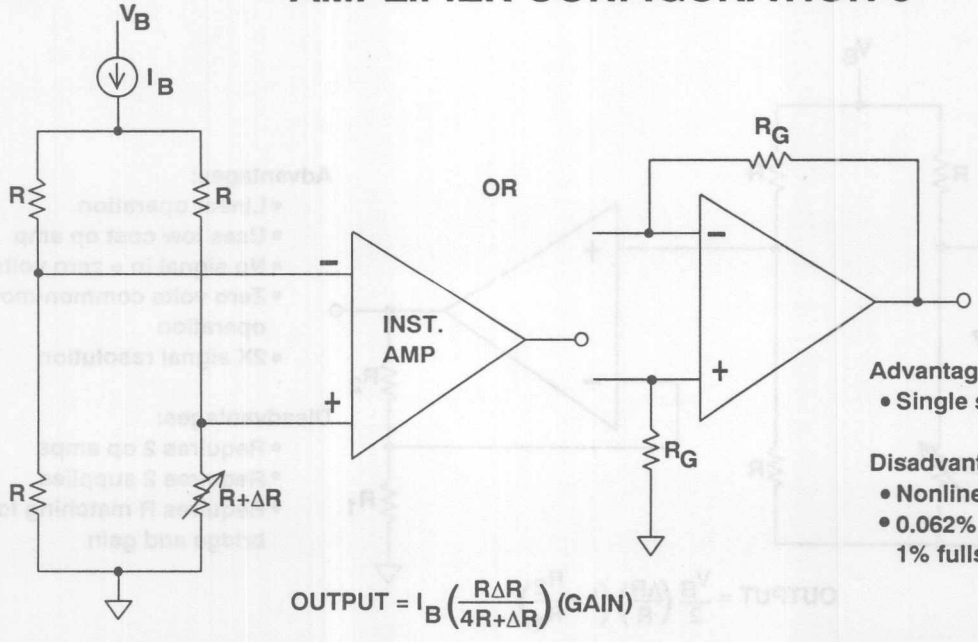
Advantages:
- Linear operation
- Single resistor sets gain
- Constant zero volts common-mode
- 2X signal resolution

Disadvantages:
- Requires 2 op amps
- Requires 2 supplies

$$\text{OUTPUT} = V_B \left(\frac{\Delta R}{R^2}\right) R_G$$

Figure 2.8

SINGLE-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 6



Advantages:
- Single supply operation

Disadvantages:
- Nonlinear operation
- 0.062% nonlinearity for 1% fullscale ΔR change

$$\text{OUTPUT} = I_B \left(\frac{R\Delta R}{4R+\Delta R}\right) (\text{GAIN})$$

Figure 2.9

A typical implementation of a single-element varying bridge is an RTD thermometer amplifier as shown in Figure 2.10. The bridge power is derived from a stable 2.500V reference. Each leg of the bridge normally carries only 600μA so as to minimize self-heating. The bridge is servoed to suppress the common-mode voltage to zero , thus simplifying the gain stage design as well as assuring linear performance.

At 600μA current, the RTD dissipates less than 0.1mW of power even at the maximum resistance . This is important because some RTDs have thermal resistance as high as 0.5 to 0.8 °C per mW. Consequently, even 1mW of dissipation can result in an appreciable error if the element is allowed to self heat. The design ensures self-heating contributes much less than 0.1 °C error over the full temperature range of the RTD.

If the RTD is remotely located some distance away from the measurement circuitry, the long line resistance will contribute measurement error. The optional zero adjustment circuit provides a method to balance the bridge. Calibration can be made at low temperatures or at the 0°C point. At 0°C the output should be adjusted to zero volts. The virtual ground summing node of the RTD is a convenient point to linearize the sensor by providing a small amount of positive feedback from the output. To calibrate, set the fullscale and linearity adjust pots to midpoint. Either apply a 500°C temperature to the sensor or substitute the equivalent 500°C RTD resistance. Then adjust the fullscale pot to 5.000V output. Apply half-scale temperature or the equivalent RTD resistance, then adjust the linearity pot to 2.500V output. Recheck the two settings and adjust as needed. Over the temperature range of -150° to +500°C, the circuit achieves better than ±0.5°C accuracy.

LOW POWER LINEARIZED RTD THERMOMETER BRIDGE AMPLIFIER

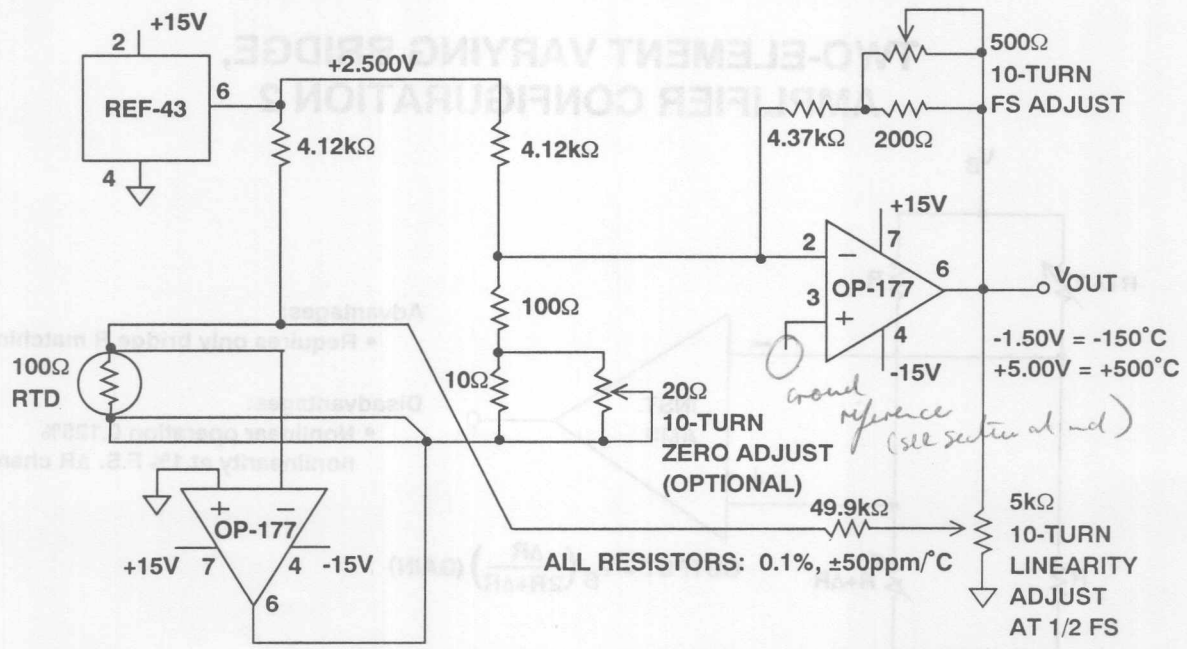
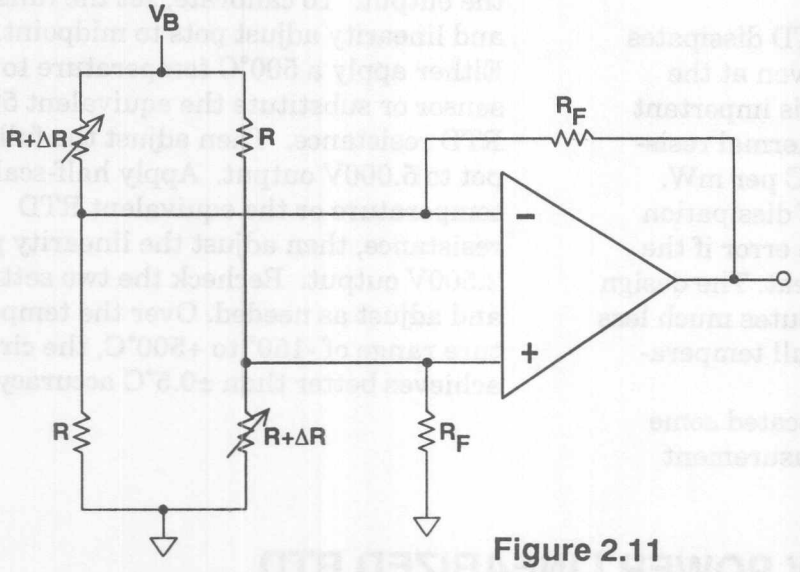


Figure 2.10

TWO-ELEMENT VARYING SENSOR BRIDGES

Two-element varying sensor bridges are commonly found in pressure transducers and flow meter systems. They have the benefit of producing twice the signal for a given input than the single-element bridges. Figures 2.11through 2.15 show several two-element bridge configurations and the relative merits of each.

TWO-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 1



Advantages:

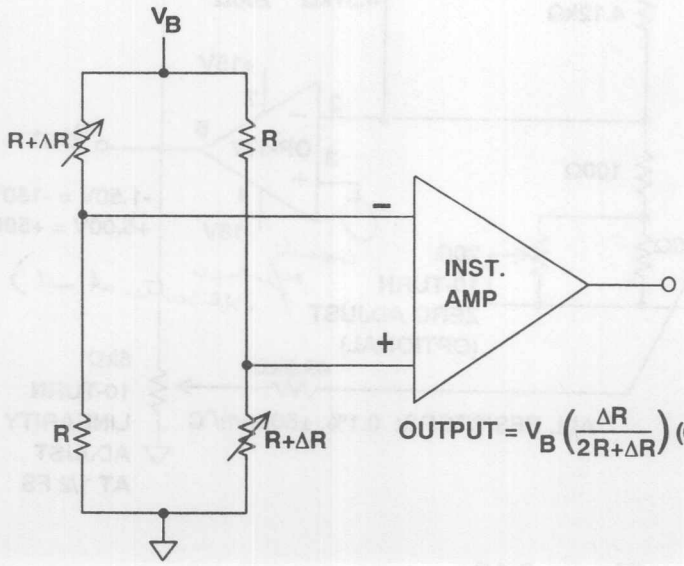
- Uses low cost op-amp
- Excellent gain-setting range
- No signal in = OV out
- Single supply operation

Disadvantages:

- Nonlinear operation 0.25% nonlinearity at 1% fullscale ΔR change
- Requires R matching

Figure 2.11

TWO-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 2



Advantages:

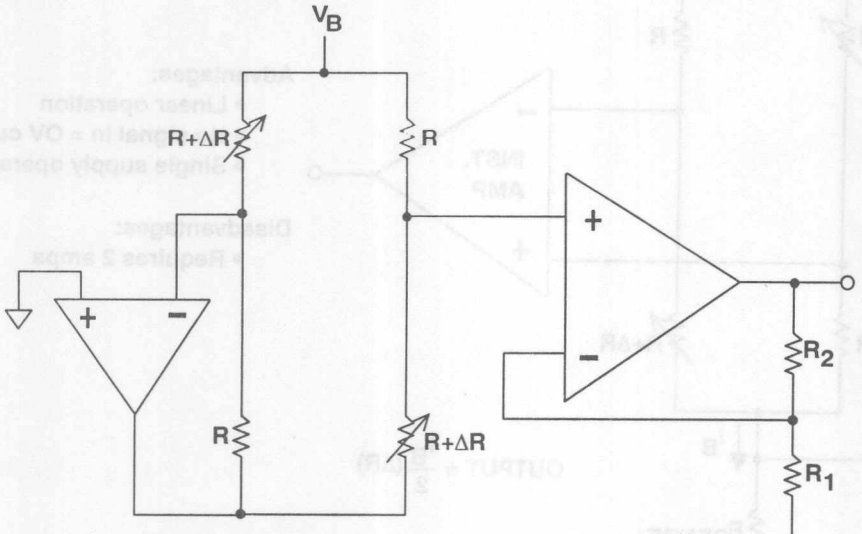
- Requires only bridge R matching

Disadvantages:

- Nonlinear operation 0.125% nonlinearity at 1% F.S. ΔR change

Figure 2.12

TWO-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 3



Advantage:

- 2X signal output

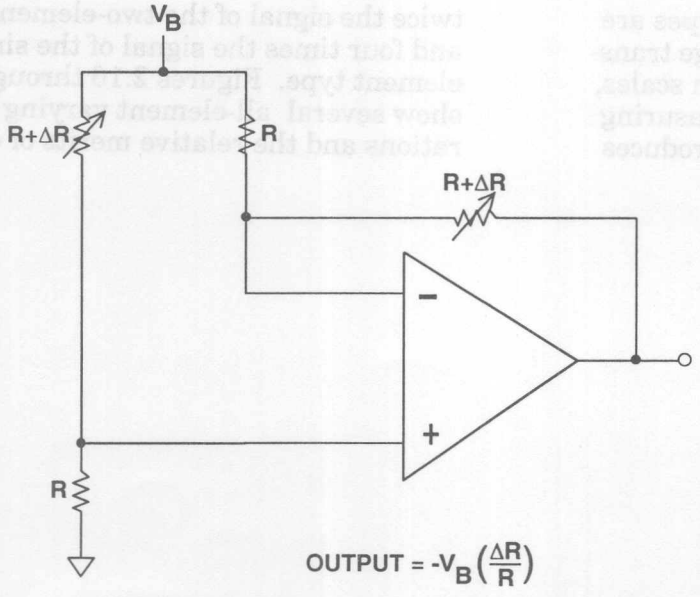
Disadvantages:

- Nonlinear operation 0.25% nonlinearity at 1% fullscale ΔR change
- Requires 2 op amps
- Requires 2 supplies
- R matching critical

$$\text{OUTPUT} = V_B\left(1 - \frac{R}{R+\Delta R}\right)\left(1 + \frac{R_2}{R_1}\right)$$

Figure 2.13

TWO-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 4



Advantage:

- Linear operation

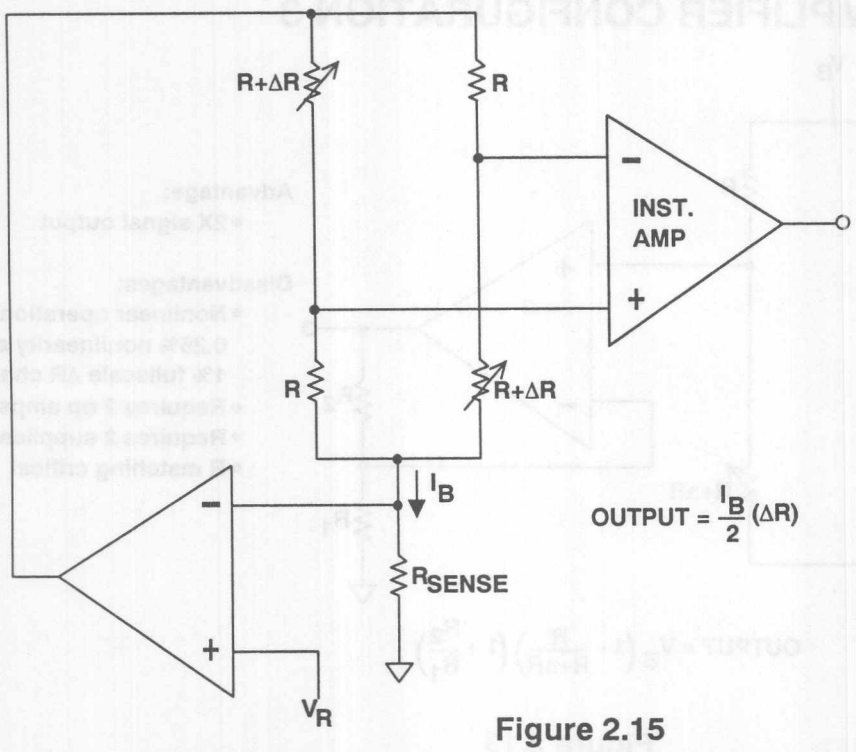
Disadvantages:

- Low signal output implies larger errors
- Requires second amp for gain

$$\text{OUTPUT} = -V_B\left(\frac{\Delta R}{R}\right)$$

Figure 2.14

TWO-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 5



Advantages:
- Linear operation
- No signal in = OV out
- Single supply operation

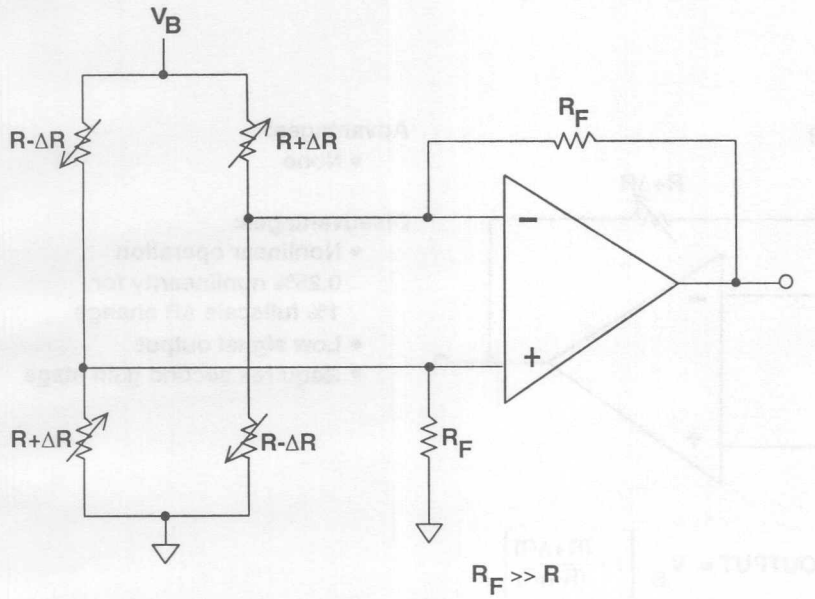
Disadvantages:
- Requires 2 amps

Figure 2.15

ALL-ELEMENT VARYING SENSOR BRIDGES

All-element varying bridge types are most popular among strain-gauge transducer applications such as weigh scales, pressure sensors, and strain measuring instruments. This bridge type produces twice the signal of the two-element bridge, and four times the signal of the single-element type. Figures 2.16 through 2.21 show several all-element varying configurations and the relative merits of each.

ALL-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 1

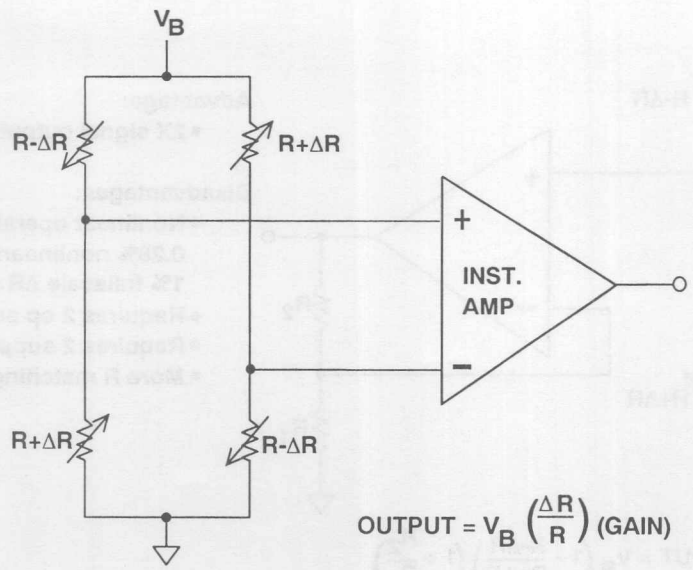


Advantages:
- Single supply operation
- No signal in = OV out
- Simple to set gain
- Uses low-cost op amp

Disadvantages:
- Slightly nonlinear 0.0037% nonlinearity at 1% F.S. ΔR change, at Gain = 100
- R matching critical

Figure 2.16

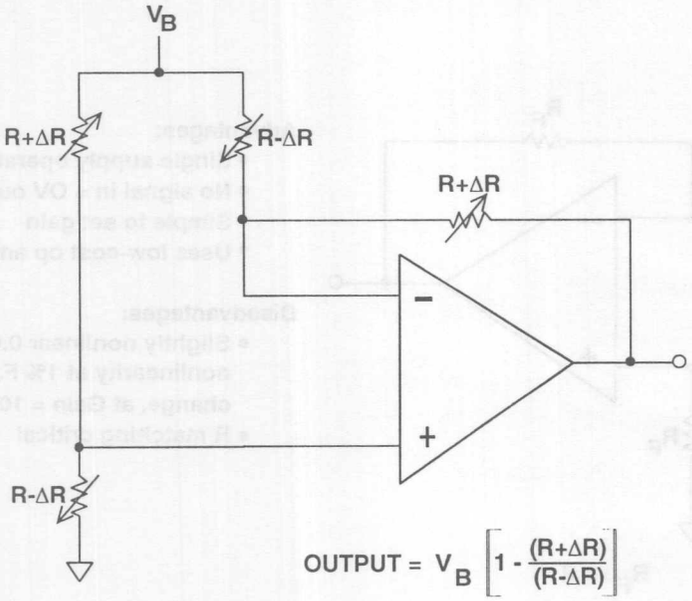
ALL-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 2



Advantages:
- Linear operation
- Single supply operation
- No signal in = OV out
- No R matching required

Figure 2.17

ALL-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 3



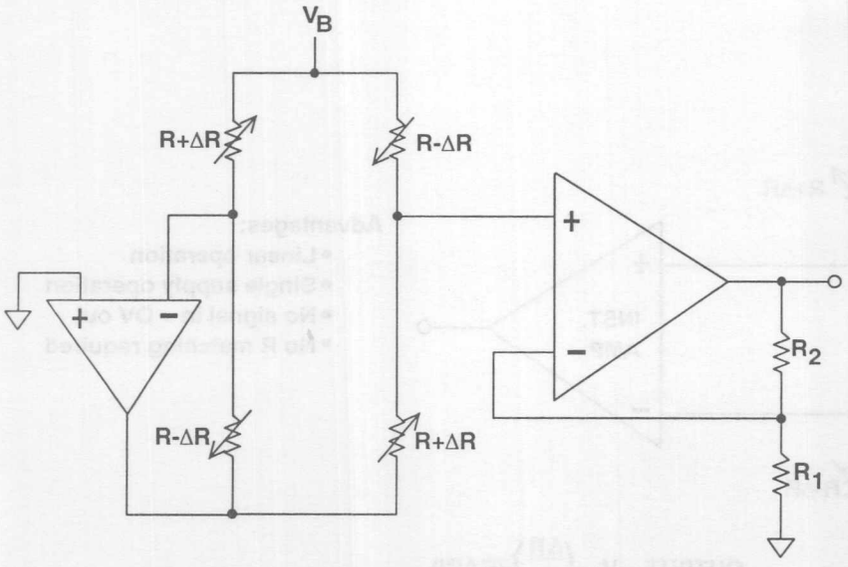
Advantages:
- None

Disadvantages:
- Nonlinear operation
  0.25% nonlinearity for
  1% fullscale ΔR change
- Low signal output
- Requires second gain stage

$$\text{OUTPUT} = V_B \left[1 - \frac{(R+\Delta R)}{(R-\Delta R)}\right]$$

Figure 2.18

ALL-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 4



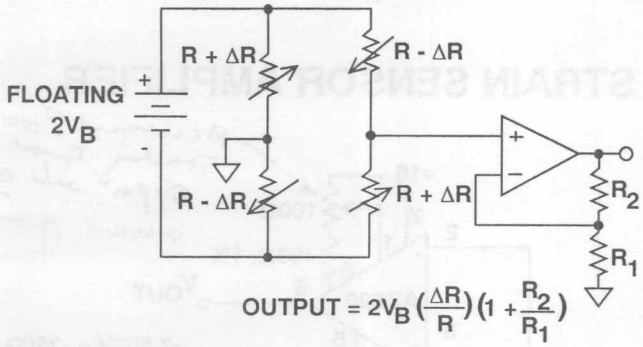
Advantage:
- 2X signal output

Disadvantages:
- Nonlinear operation
  0.25% nonlinearity at
  1% fullscale ΔR change
- Requires 2 op amps
- Requires 2 supplies
- More R matching

$$\text{OUTPUT} = V_B \left(1 - \frac{R-\Delta R}{R+\Delta R}\right)\left(1 + \frac{R_2}{R_1}\right)$$

Figure 2.19

ALL-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 5



ADVANTAGES:

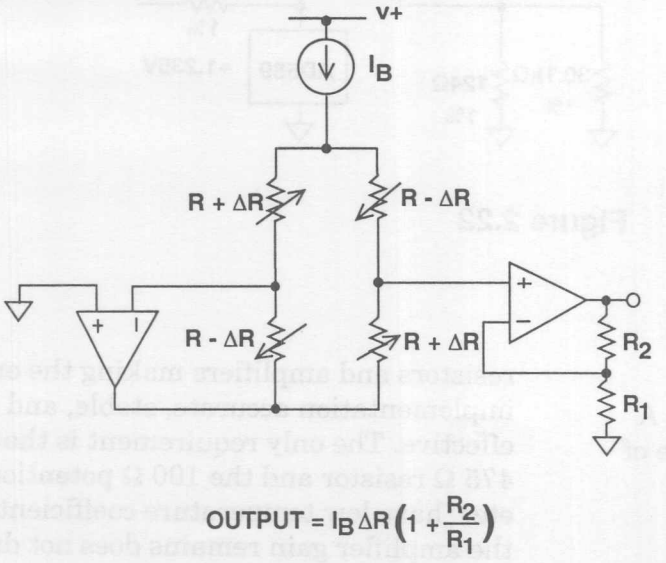
- Linear operation
- 2X signal output
- Uses low-cost op amp

DISADVANTAGES:

- Requires elaborate floating supply

Figure 2.20

ALL-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 6



ADVANTAGES:

- Linear operation
- 2X signal output
- Gain set resistors affect gain accuracy

DISADVANTAGES:

- Requires 2 op amps
- Requires a current source
- Requires 2 supplies

Figure 2.21

An example of an all-element varying bridge circuit is a fatigue monitoring strain sensing circuit as shown in Figure 2.22. The full bridge is an integrated unit that can be attached to the surface on which the strain or flex is to be measured. In order to facilitate remote sensing, current excitation is used. The OP-177 servos the bridge current to 10mA around a reference voltage of 1.235V. The strain gauge produces an output of 10.25mV/1000με. The signal is differentially amplified by the AD620 instrumentation amplifier. Full-scale strain voltage may be set by adjusting the 100 Ω gain potentiometer such that for a strain of -3500με, the output reads -3.500V; and for a strain of +5000με, the output registers a +5.000V. The measurement may then be displayed with a digital voltmeter.

FATIGUE LOAD STRAIN SENSOR AMPLIFIER

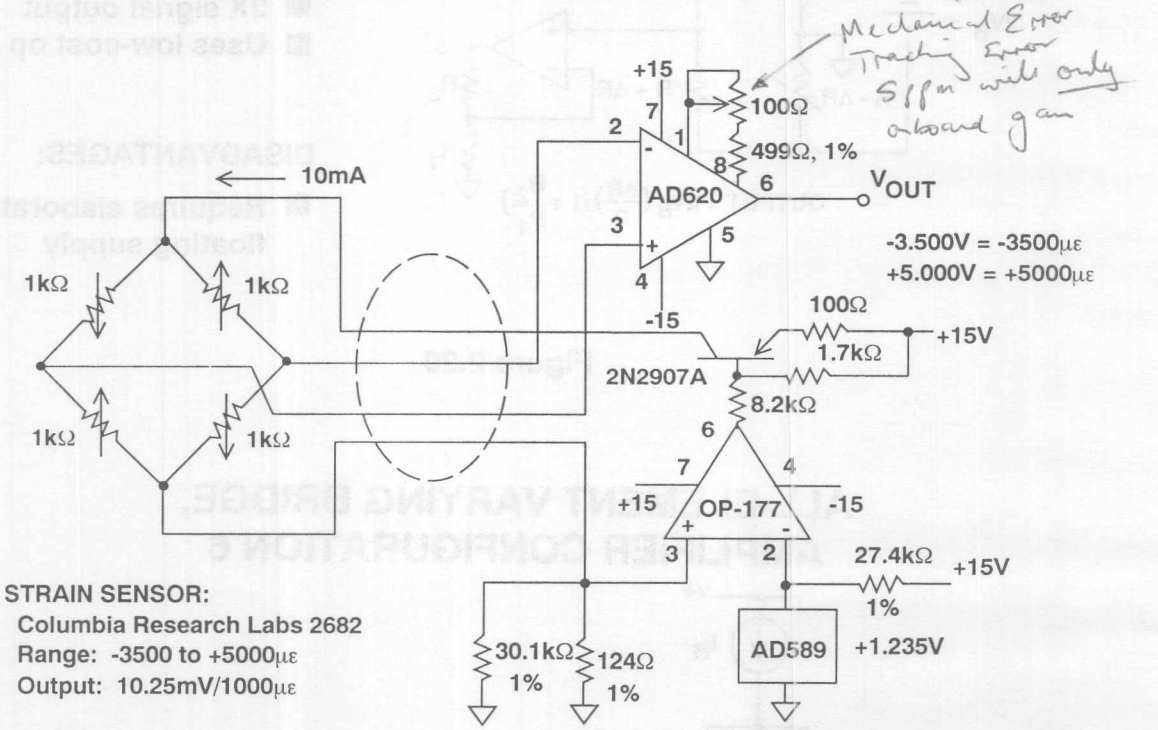


Figure 2.22

Another example is a weigh-scale amplifier circuit shown in Figure 2.23. A typical load cell has a bridge resistance of 350 Ω. A 10.000V bridge excitation produces linear bridge behavior. To ensure this linearity is preserved, an instrumentation amplifier is used. This design has a minimum number of critical resistors and amplifiers making the entire implementation accurate, stable, and cost effective. The only requirement is that the 475 Ω resistor and the 100 Ω potentiometer have low temperature coefficients so the amplifier gain remains does not drift over temperature.

WEIGH-SCALE LOAD CELL AMPLIFIER

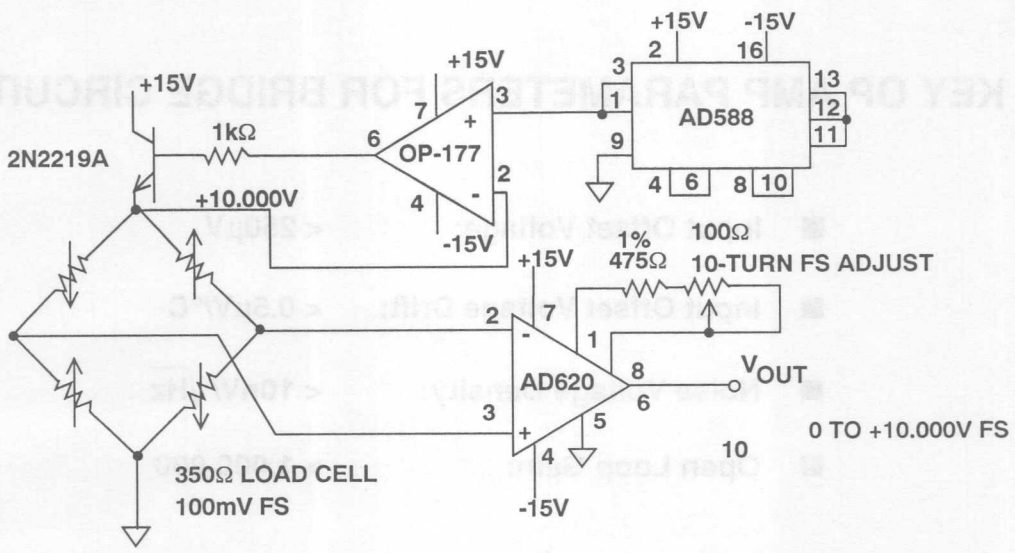


Figure 2.23

CHOOSING THE RIGHT AMPLIFIER FOR OPTIMUM PERFORMANCE

Once a bridge circuit configuration is chosen, it is of critical importance to choose the right amplifier for that circuit. There are several types of amplifiers from which to choose: precision op amps, instrumentation amplifiers, and chopper stabilized amplifiers. Each has unique attributes and capabilities that optimize a particular design feature. Other considerations that relate to system requirements are power consumption, bandwidth, supply voltages, and cost. The following sections discuss some of these tradeoffs.

Although many op amp parameters effect the accuracy of the circuit, it is important to identify the most important ones in the particular circuit application. For example, an op amp input offset current of 10 nA contributes only 1.75μV of error in a 350-ohm bridge. Clearly this is less critical than a 10μV input offset voltage error of a typical precision op amp. It is therefore important to focus on the parameters that have significant error impact on the circuit accuracy. Figure 2.24 lists some of the op amp critical parameters for high precision, high gain applications.

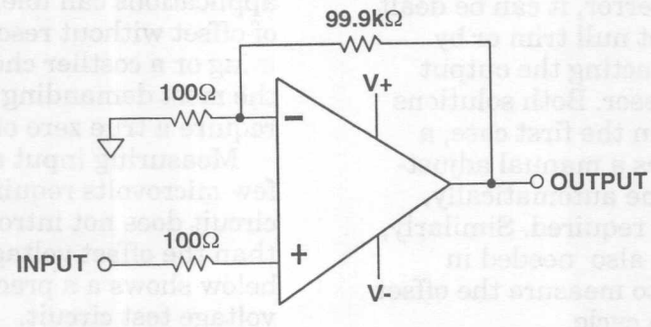
KEY OP AMP PARAMETERS FOR BRIDGE CIRCUITS

- **Input Offset Voltage:** < 250μV
- **Input Offset Voltage Drift:** < 0.5μV/°C
- **Noise Voltage Density:** < 10nV/$\sqrt{Hz}$
- **Open Loop Gain:** > 1,000,000

Figure 2.24

Let us compare some of the latest generation precision op amps and see how they perform under a complete DC error analysis. The circuit used is a simple gain of 1000 amplifier as shown in Figure 2.25. For the purpose of the analysis, only the error contribution due to the amplifier is considered. The external resistor tolerance is assumed to be zero. Since the bridge output has very little common-mode voltage change, no common-mode error is assumed. Total error in microvolts referred to the input for various op amps is shown in Figure 2.26.

AMPLIFIER ERROR BUDGET ANALYSIS



Assumptions:

- Zero Tolerance Resistors
- ±5% Power Supply Tolerance
- Negligible Common-Mode Voltage Change

Figure 2.25

TOTAL ERRORS IN MICROVOLTS REFERRED TO INPUT (RTI) FOR GAIN OF 1000 AMPLIFIER

	INDUSTRY STANDARD	ULTRA PRECISION	ULTRA PRECISION	LO POWER, LO I_B	LO POWER, LO I_B
PARAMETER	OP-07D	OP-177G	AD707J	OP-97F	AD705J
Max V_{OS}	150	60	90	75	90
Max V_{OS}/T	100	40	10	125	60
Max PSRR (3V)	153	9.5	9.5	12	12
Min A_{VOL} (FS)	100	5	1.2	66	66
Input Noise p-p	2	1.4	1.0	2.1	1.9
Max I_{OS}	0.8	0.5	0.15	0	0
Total Error RTI	506	112	126	299	230

Figure 2.26

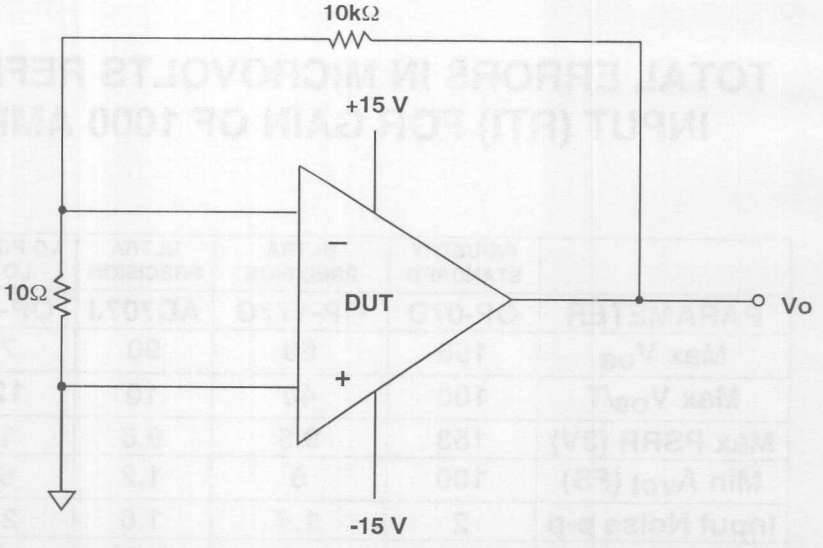
INPUT OFFSET VOLTAGE ERROR

Input offset voltage is usually one of the largest error sources for precision amplifier circuit designs. However, because it is a systemic error, it can be dealt with by using an offset null trim or by mathematically subtracting the output signal in a post-processor. Both solutions carry a cost penalty. In the first case, a potentiometer requires a manual adjustment step. Even if done automatically, additional circuitry is required. Similarly, additional circuitry is also needed in order for a processor to measure the offset during the calibration cycle.

Today's generation of precision op amps offers initial offset voltages as low as 10μV for bipolar devices, and far less for chopper stabilized amplifiers (more on chopper amps in the next sections). Most applications can tolerate a small amount of offset without resorting to null trimming or a costlier chopper amplifier. Only the most demanding applications will require a true zero offset error.

Measuring input offset voltages of a few microvolts requires that the test circuit does not introduce more error than the offset voltage itself. Figure 2.27 below shows a a precision input offset voltage test circuit.

INPUT OFFSET VOLTAGE TEST CIRCUIT



$$V_{IOS} = \frac{Vo}{1000}, \text{ Referred to Input}$$

Figure 2.27

As simple as it may look, this circuit may give inaccurate results unless the proper precautions are taken. The largest error comes from thermoelectric voltages caused by the temperature differential between the circuit component leads that form a pair of mismatched thermocouple junctions. Depending on the component or the IC package lead material, the thermoelectric voltage temperature coefficient may range anywhere from 2μV/ °C to more than 40μV/ °C when connected to a copper printed circuit board trace. Even a fraction of a degree difference at a single junction can be caused by air current and may induce large a enough error to render the offset voltage measurement invalid. Careful attention must also be given to proper layout, bypassing, and grounding techniques to avoid further error sources.

Measuring microvolts of offset reliably and repeatably may therefore depend more on the mechanical layout of the components and how they are placed on the PC board than on the circuit itself. Keep in mind that the two connections of a component such as a resistor create two equal, but opposite polarity, thermoelectric voltages (assuming they are connected to the same metal such as the copper trace on a PC board) which cancel each other — as long as they are at the exact same temperature. Clean connections and short lead lengths help to minimize temperature gradients and increase the accuracy of the measurement.

INPUT OFFSET VOLTAGE DRIFT

This temperature induced error is perhaps the most troublesome to deal with. One reason is that the drift characteristic of each op amp, even of the same type, is random and not necessarily linear. Predicting it accurately is impossible.

Today's precision op amps have reduced this error to satisfactory levels except for the most demanding applications. For example, ultra-precision op amps such as the OP-177 and the AD707 guarantee their input offset drifts to be less than 0.1μV/°C (for the top temperature grade devices).

These precision op amps achieve low drift by extremely careful chip layout. The photomicrograph of the OP-177 die as in Figure 2.28 illustrates a thermally symmetrical layout that minimizes drift. All offset and drift critical components lie symmetrically along a center line. Heat generated from the output stage and quiescent self-heating travels along this axis, thereby effecting all matched pairs equally.

There are other methods of minimizing offset voltage and offset voltage drift. One is a periodic auto-zero calibration under microprocessor control. Another is continuous zeroing as in a chopper stabilized amplifier. Chopper amplifiers do an excellent job of zeroing the offset and drift, however they tend to be much noisier. A way to achieve zero offset and drift and still have the low noise characteristics of a precision amplifier is shown in Figure 2.29 below. In addition to continuously nulling offset and drift, this circuit minimizes common-mode rejection error as well.

PHOTOMICROGRAPH OF OP-177 CHIP

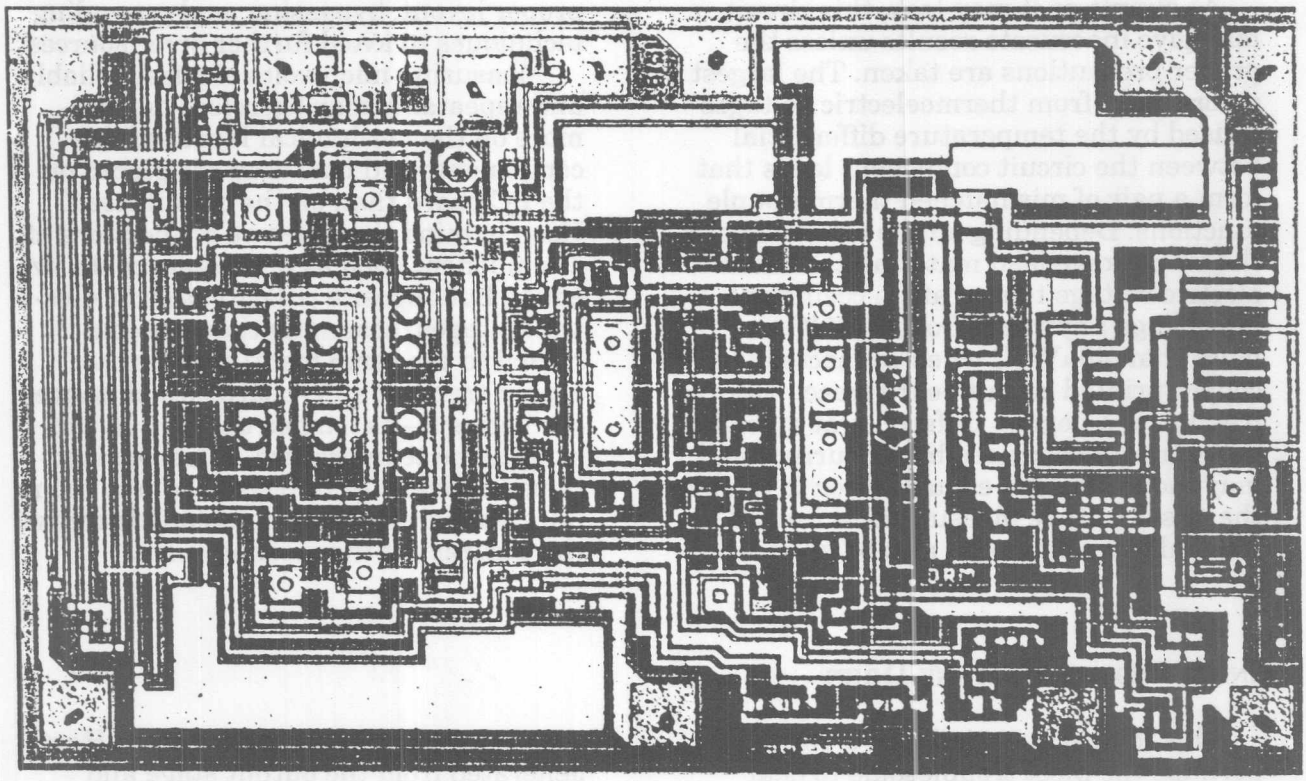
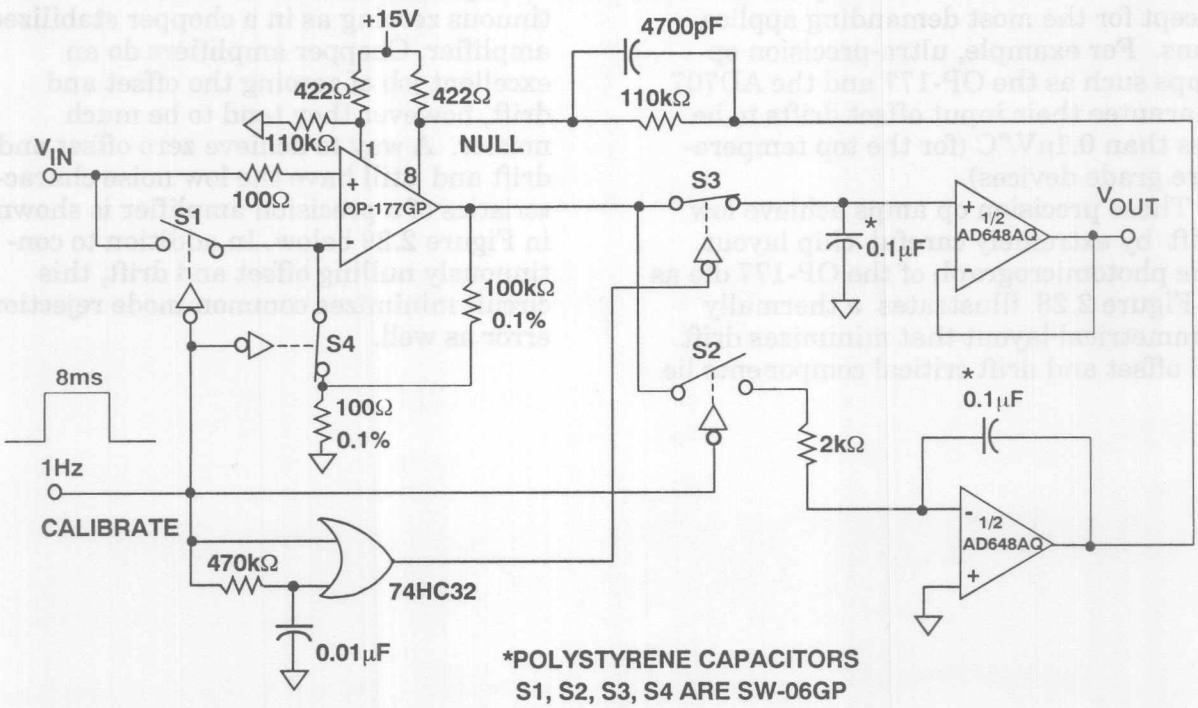


Figure 2.28

LOW-NOISE AUTO-ZERO CIRCUIT CORRECTS COMMON-MODE ERROR

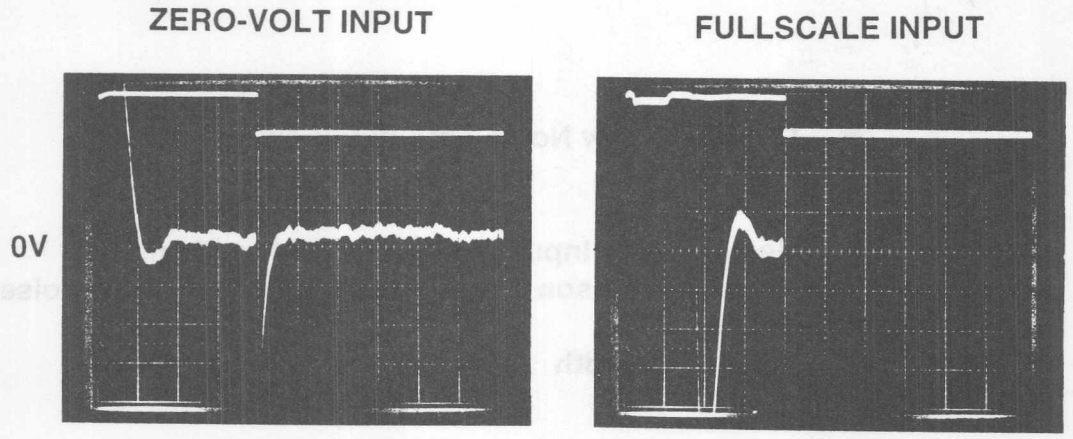


*POLYSTYRENE CAPACITORS
S1, S2, S3, S4 ARE SW-06GP

Figure 2.29

The amplifier operates at a gain of 1001 (although it can be set at any gain by adjusting the feedback resistors ratio). In normal operation, switches SW3 and SW4 closed, while SW1 and SW2 are open. The auto-zero cycle begins when a logic high is asserted at the CALIBRATE input for 8ms, toggling all 4 switches simultaneously. The opening of SW3 holds the most recent voltage at the output. At the same time the closing of SW1 shorts the two inputs of the OP-177 together, while SW4 opens the OP-177 loop. Nulling occurs as SW2 closes the OP-177's null circuit around the AD648 error amplifier. It servos the null pin (pin 8) until the OP-177 output goes to zero (plus or minus the input offset voltage of the AD648). The 4700pF shunting capacitor across the 110kΩ null bias resistor provides feedforward to speed up the OP-177 response. Otherwise the frequency response of the OP-177 will approach the cutoff frequency of the AD648 and cause a low frequency oscillation. 8ms is allowed for the servo loop to settle. The photos in Figure 2.30 depict this servo action at the OP-177 output.

AUTO-ZERO ACTION



TOP TRACES: CALIBRATE INPUT
BOTTOM TRACES: OP-177 OUTPUT

VERTICAL SCALE: 5mV / div. OR 5μV / div. (RTI)
HORIZONTAL SCALE: 2ms / div.

Figure 2.30

At the end of the 8ms auto-zero cycle, the CALIBRATE input logic goes low. All switches toggle except for SW3, thereby holding the nulling voltage at the AD648 error amplifier until the next auto-zero cycle. The closing of SW3 is delayed 5ms by the 470kΩ resistor and the 0.01μF capacitor to allow the OP-177 to settle after its loop is closed. This delayed switch closure minimizes disturbances at the sample and hold output.

The calibration cycle can be controlled by a microprocessor during its idle time and when the amplifier is not making a measurement. Alternatively, a simple timer circuit operating at 1 or 2 Hz can periodically calibrate the circuit. Any ambient temperature-induced drift is corrected by the periodic auto-zeroing. The circuit maintains a constant offset of less than 5μV referred to the input (RTI) regardless of temperature.

DESIGNING FOR LOW NOISE

Besides offset voltage error and drift, noise is a primary concern for precision amplifier applications. Highly accurate instruments require the noise floor to be as low as possible. In addition to choosing the lowest noise amplifier for a given circuit, there are other techniques which will keep noise to a minimum. A more detailed treatment of op amp noise is given in Section XI.

DESIGN FOR LOW NOISE

- Choose A Low Noise Amp With Low 1 / f Corner Frequency
- Use As Small Input Resistance As Practical To Reduce Johnson Noise And Effects Of Current Noise
- Limit Bandwidth

Figure 2.31

SELECTING A LOW NOISE OP AMP

Before selecting the appropriate low noise op amp, the op amp source impedance and feedback resistances must be known. For high gain amplifiers that measure low level voltages, low voltage noise is important. For high source resistances, low current noise may become more critical. Figure 2.32 compares input offset voltage and 1kHz input voltage noise for a number of popular precision op amps.

OP AMP NOISE AND OFFSET VOLTAGE CHARACTERISTICS

OP AMP PART #	INPUT NOISE VOLTAGE SPECTRAL DENSITY @ 1kHz, nV/$\sqrt{Hz}$	INPUT OFFSET VOLTAGE, µV
AD797	0.9	100
SSM-2017	0.95	1200
AD743	2.9	1000
AD745	2.9	250
OP-27	3.0	25
OP-37	3.0	25
OP-270	3.2	75
OP-470	3.2	400
OP-50	4.5	25
OP-471	6.5	800
OP-07	7.0	25
OP-271	7.6	200
AD645	9.0	250
OP-177	9.6	10
AD707	9.6	15
OP-77	9.6	25

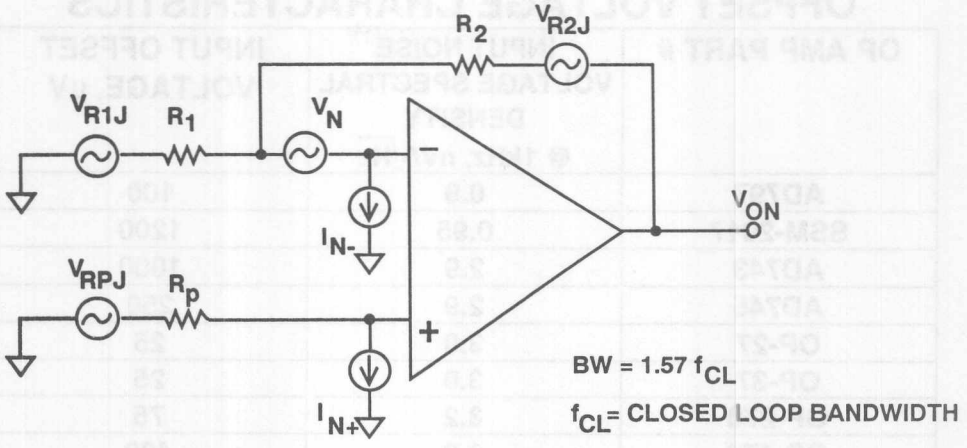
Figure 2.32

DETERMINE THE SOURCE RESISTANCE

While the amplifier's voltage noise is important, external resistances that are connected to the amplifier inputs may also generate additional noise at the op amp output. This noise is caused by the amplifier's input current noise as well as the individual resistors' thermal (Johnson) noise. All noise components are then root-sum-squared to calculate the total noise at the output of the op amp.

Virtually all amplifier circuits can be simplified to an equivalent circuit model that contains all noise sources as shown in Figure 2.33 .

OP AMP NOISE MODEL



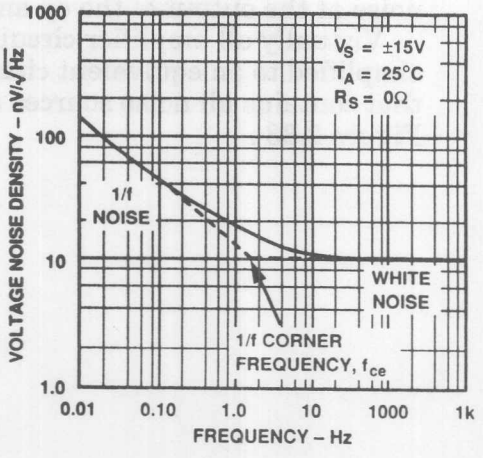
$$V_{ON} = \sqrt{BW}\sqrt{I_{N-}^2 R_2^2 + I_{N+}^2 R_p^2 \left[1+\frac{R_2}{R_1}\right]^2 + V_N^2 \left[1+\frac{R_2}{R_1}\right]^2 + 4kTR_2 + 4kTR_1\left[\frac{R_2}{R_1}\right]^2 + 4kTR_p\left[1+\frac{R_2}{R_1}\right]^2}$$

Figure 2.33

Each noise component must be integrated over the appropriate bandwidth . The typical noise spectral density of an op amp is shown in Figure 2. 34 for the OP-177.

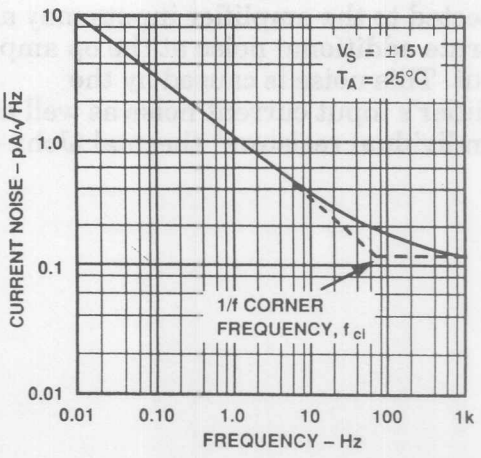
OP-177 INPUT NOISE SPECTRAL DENSITIES

OP-177 VOLTAGE NOISE



$$E_n(f_H,f_L) = e_{nW}\sqrt{f_{ce}\cdot \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$$

OP-177 CURRENT NOISE



$$I_n(f_H,f_L) = i_{nW}\sqrt{f_{ci}\cdot \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$$

Figure 2.34

The total rms output noise may be calculated using the equations shown in Figure 2.33 and Figure 2.34. A detailed description of this process is given in Section XI.

The above model may be used to estimate the RMS value of the output noise for virtually any amplifier circuit. Note that minimizing noise not only requires the use of low source resistances and low noise op amps, but also keeping the bandwidth as low as practical for the application. For very low bandwidth applications, choose an op amp that has a low voltage or current noise corner frequency, depending on which is the dominant contributor in the circuit.

It is important to note that JFET input op amps often have higher voltage noise and higher noise corner frequencies than bipolar op amps. For example, most JFET op amps' voltage noise is in the range of 30 to 40 nV/ √Hz with a noise corner frequency ranging from 100Hz to 500Hz. Bipolar op amps have a voltage noise ranging from a few nV/√Hz to 20 nV/√Hz, and their noise corner frequency is usually less than 100Hz.

New JFET input op amps have noise voltages and corner frequencies comparable with bipolar op amps. This trend is exemplified by the new AD745 ultra-low noise BiFET op amp. It achieves 2.9 nV/ √Hz voltage noise at 10kHz with a noise corner frequency of 50Hz. The combination of this low noise voltage and its 6.9 fA/√Hz noise current is unsurpassed for a FET-input monolithic op amp. Key specifications for the AD745 are given in Figure 2.35.

AD745 ULTRA-LOW NOISE, HIGH SPEED BiFET OP AMP

- **Ultra-Low Noise Density ..... 2.9 nV/ Hz @ 10kHz**
- **Low Voltage Noise ..... 0.38 μVp-p, 0.1Hz to 10Hz**
- **Ultra-Low Current Noise ..... 6.9 fA/ Hz @ 1kHz**
- **High Gain-Bandwidth 20MHz**
- **High Slew Rate ..... 12.5 V/μs**

Figure 2.35

The benefits of these specifications become evident as the source resistance goes up, as in the case of a high impedance bridge or a high impedance transducer such as an ultrasound sensor. In these high impedance applications, the current noise may be a significant contributor to the output noise. This is where the AD745's ultra-low voltage and current noise combination can keep the noise floor at a minimum, in spite of the presence of a high source resistance. Figure 2.36 illustrates how the source resistance effects the input noise for both the bipolar OP-37 and the BIFET AD745. Note that for high values of source resistance, the AD745 is the best choice.

CURRENT NOISE IS IMPORTANT AS SOURCE RESISTANCE INCREASES. AD745 COMBINES LOW VOLTAGE AND CURRENT NOISE TO ACCOMMODATE A WIDE RANGE OF SOURCE RESISTANCES

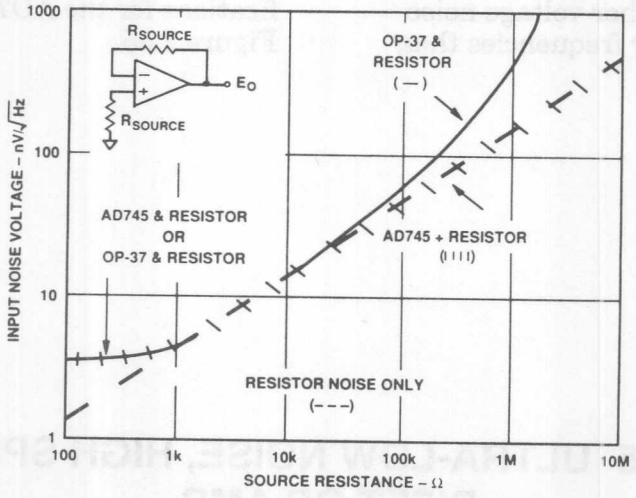


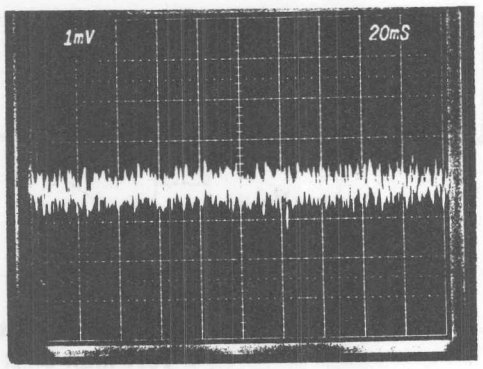
Figure 2.36

LIMIT BANDWIDTH TO REDUCE NOISE

As the noise equations suggest, noise is proportional to the square root of the circuit bandwidth. Therefore, noise can be minimized by limiting the bandwidth to that actually required by the signal. For example, if the measuring bandwidth of interest is only 1Hz, then signals above this frequency may be filtered to reduce the noise. Figure 2.37 shows the dramatic difference between the output noise level with a 1Hz lowpass filter and a 6kHz lowpass filter.

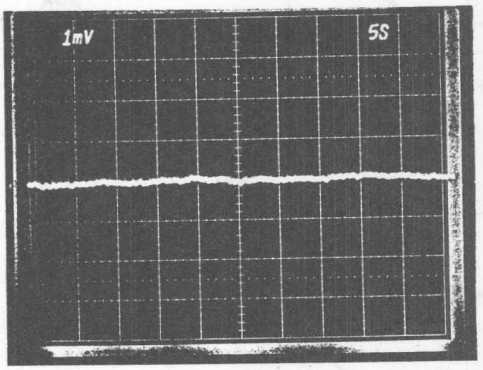
LIMITING BANDWIDTH TO REDUCE NOISE OP-177 @ GAIN = 1000

LOWPASS FILTER = 6kHz



VERTICAL SCALE: 1mV / div.
HORIZONTAL SCALE: 20ms / div.

LOWPASS FILTER = 1Hz



VERTICAL SCALE: 1mV / div.
HORIZONTAL SCALE: 5s / div.

Figure 2.37

Because the gain-bandwidth product of a voltage feedback op amp is constant, high gains imply proportionally lower closed loop bandwidths. This means that the amplifier's own reduced bandwidth can serve as a low-pass filter at high gains. In most cases this effect helps to reduce the output noise.

CHOOSING INSTRUMENTATION AMPLIFIERS

When amplifying low level signal in the presence of high common-mode voltages, such as in the case of a bridge circuit, an instrumentation amplifier may provide an efficient high performance solution. Although an instrumentation amplifier can be built easily with the traditional two or three op amp configurations, monolithically integrated designs offer superior performance at low cost as shown in Figure 2.38 . Monolithic instrumentation amplifiers such as the AD620 do not require the costly external resistor matching. On chip thin film laser trimmed resistors allow the gain to be set accurately with a single external resistor.

CHOOSING INSTRUMENTATION AMPLIFIER

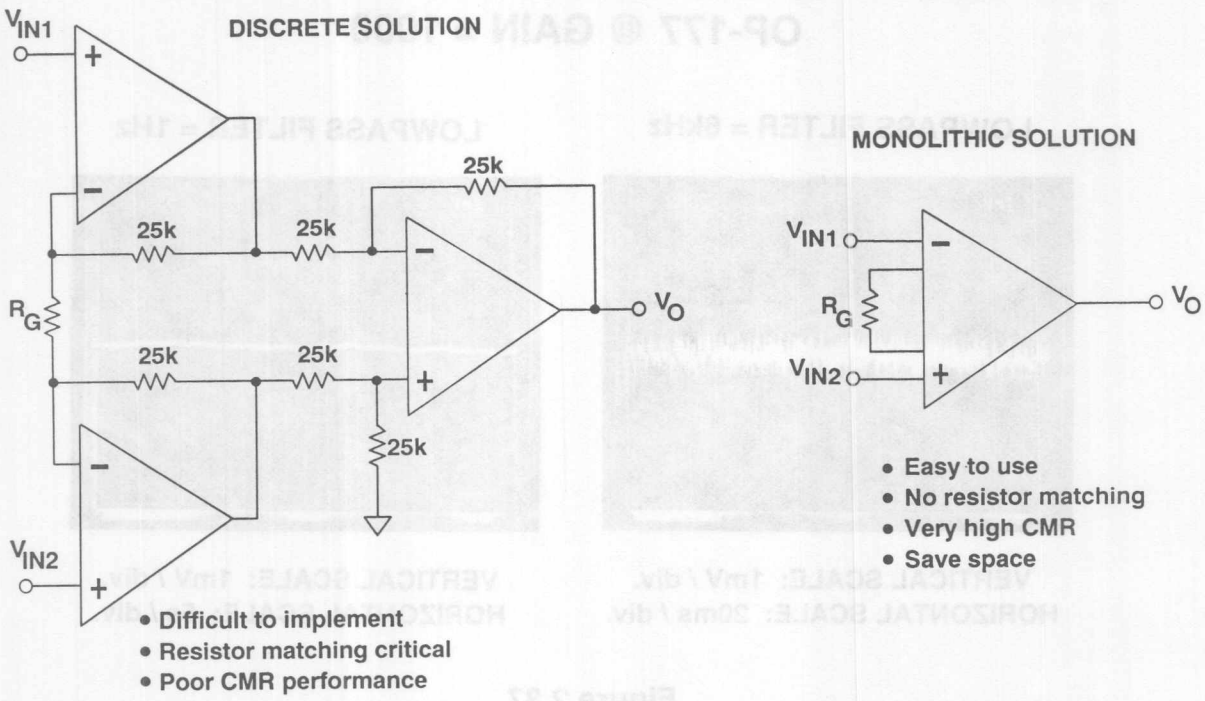


Figure 2.38

Instrumentation amplifiers may be implemented in discrete form if high performance levels are not required and printed circuit board area is available to accommodate the additional components required. For example, dual or quad op amps and 1% resistors may be used to build an instrumentation amplifier as shown in Figure 2.39.

This BiFET input instrumentation amplifier offers many performance benefits including low input bias currents, low input offset, and low offset voltage drift. It consumes only 1.0 mA quiescent current. For gains other than shown in the table, use the following equations:

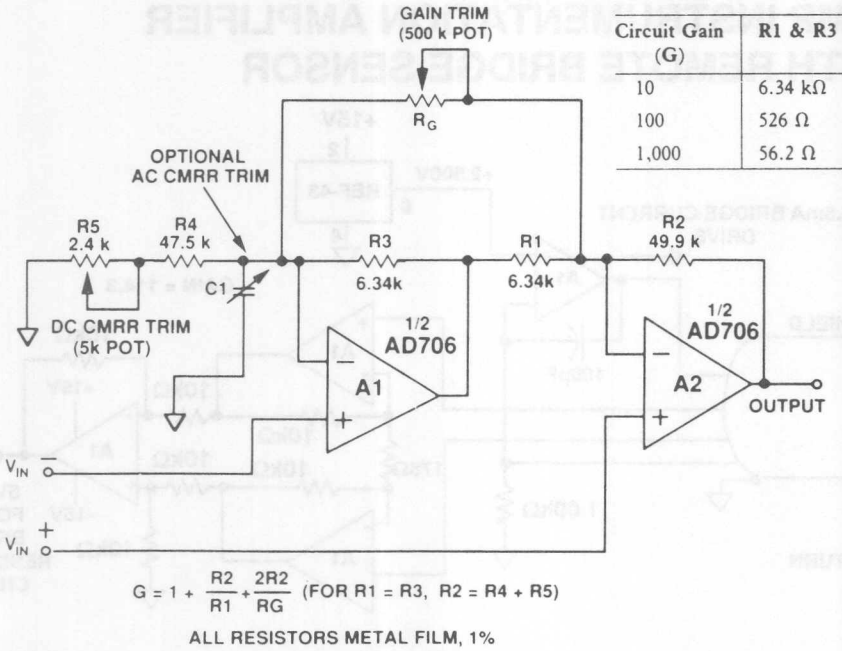
$$R2 = R4 + R5 = 49.9k\Omega$$

$$R1 = R3 = \frac{49.9k\Omega}{0.9G-1}$$

$$\text{Max Value of } R_G = \frac{99.8k\Omega}{0.06G}$$

$$C1 \sim \frac{1}{2\pi(R3)5 \times 10^5}$$

A DUAL OP AMP INSTRUMENTATION AMPLIFIER



Circuit Gain (G)	R1 & R3	R_G (Max Value of Potentiometer)	Bandwidth (−3 dB), Hz
10	6.34 kΩ	166 kΩ	50 k
100	526 Ω	16.6 kΩ	5 k
1,000	56.2 Ω	1.66 kΩ	0.5 k

Does not work for $q = 1$

Figure 2.39

The AC common mode rejection ratio maybe improved by adding the trim capacitor C1. The effects of adding this trim are shown in Figure 2.40.

AC COMMON-MODE REJECTION ENHANCEMENT USING A TRIMMING CAPACITOR

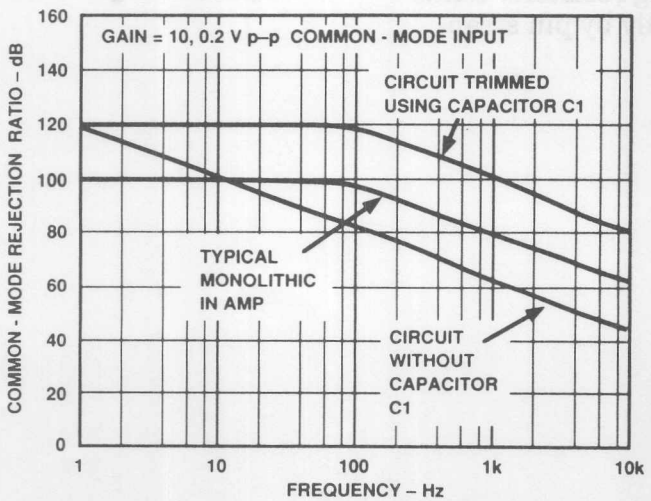
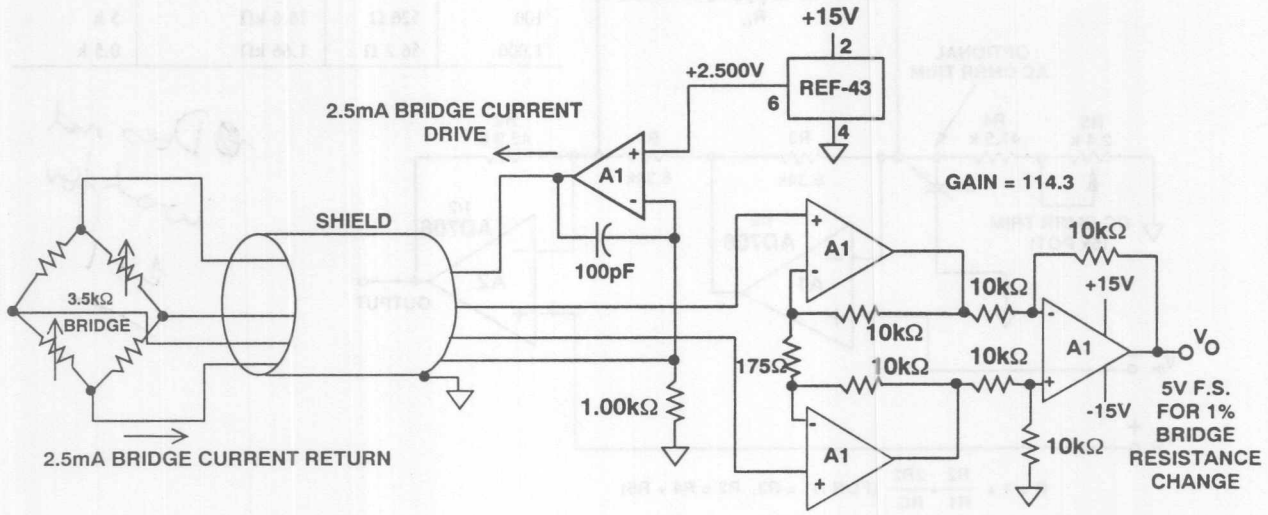


Figure 2.40

A three op amp instrumentation amplifier used in a remote bridge sensing application is shown in Figure 2.41.

3-OP AMP INSTRUMENTATION AMPLIFIER WITH REMOTE BRIDGE SENSOR



- A1 = OP-497 OR AD704
- ALL RESISTORS 1% OR BETTER

Figure 2.41

As precision and accuracy requirements increase, monolithic instrumentation amplifiers are much more cost effective and space efficient. Many designs have built-in gain setting resistors. Gains may be set either digitally by pin strapping. Some monolithic instrumentation amplifiers offer protection from input overvoltage. A comprehensive set of selection tables for instrumentation amplifiers is given in Figures 2.42 to 2.45.

INSTRUMENTATION AMPLIFIER SELECTION TABLE

HIGH PRECISION (G = 1000):

	ACCURACY %	V_{OS} µV	V_{OS} TC µV/°C	CMRR dB	INPUT NOISE (0.1-10hZ) µV p-p
AD524	0.5	50	0.5	115	0.3
AD620	0.5	50	0.6	120	0.28
AD624	1.0	25	0.25	130	0.2
AD625	0.02	25	0.25	120	0.2
AMP-01	0.6	50	0.3	125	0.12
AMP-02	0.5	100	2	115	0.4

Figure 2.42

INSTRUMENTATION AMPLIFIER SELECTION TABLE -- CONTINUED

SINGLE SUPPLY

	SUPPLY RANGE	SUPPLY CURRENT	V_{OS}	CMRR
AD626	+2.5→±7V	500µA	500µV	92dB
AMP-04	+4.5→±18	800µA	100µV	100dB

INPUT OVERVOLTAGE PROTECTED:

	Max Input Voltage
AD524	±36V
AMP-02	±60V

Figure 2.43

INSTRUMENTATION AMPLIFIER SELECTION TABLE -- CONTINUED

8-PIN PACKAGE:

	GAIN ACCURACY, %	V_{OS}, µV	CMRR, dB
AD620	0.5	50	120
AD626	0.02	500	92
AMP-02	0.5	100	115
AMP-04	0.2	100	100

Figure 2.44

INSTRUMENTATION AMPLIFIER SELECTION TABLE -- CONTINUED

HIGH INPUT IMPEDANCE:

	INPUT RESISTANCE	INPUT BIAS CURRENT
AMP-05	$10^{12}\Omega$	50pA

DIGITALLY PROGRAMMABLE GAIN:

	GAIN RANGE	GAIN ACCURACY
AD365	1,10,100,500	0.1% Max @ G = 500
AD526	1,2,4,6,16	0.02% Max @ G = 16

Figure 2.45

CMRR PERFORMANCE CRITICAL

Chief among parameters to look for in instrumentation amplifiers is the common-mode rejection performance, particularly over the rated operating temperature range.

Many monolithic instrumentation amplifiers employ the 3 op amp topology. The design is straight-forward, but depends heavily on stable on-chip laser trimmed resistors and tight resistor matching to achieve high common-mode rejection. Current feedback topology such as the AMP-01 as shown in Figure 2.46 solves some of these problems and yields exceptional CMRR performance over temperature.

AMP-01 USES CURRENT FEEDBACK TO ACHIEVE 125dB CMR @ GAIN = 1000

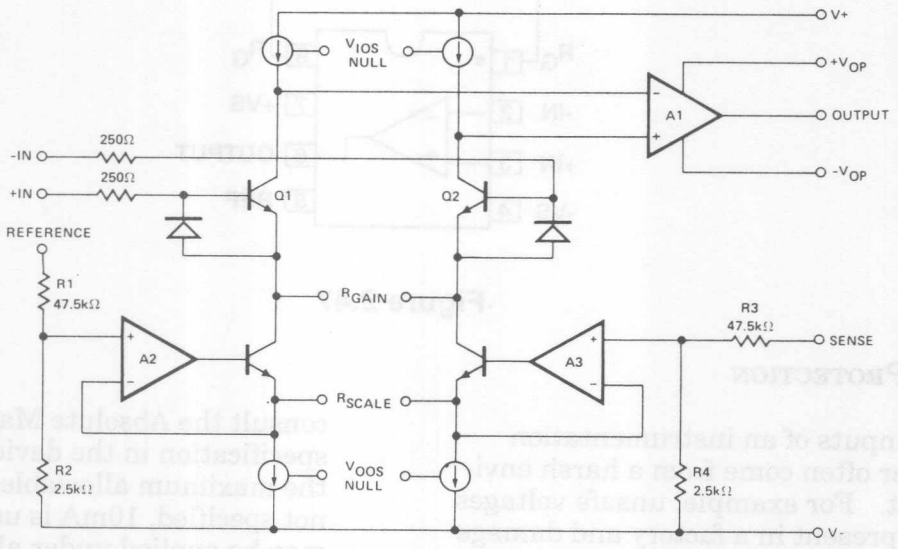


Figure 2.46

EASE OF USE IMPORTANT

Monolithic instrumentation amplifiers are quite simple to use. New designs such as the AD620 offered in 8-pin dual-in-line packages are even easier to use. Only a single external resistor is required to set the gain. The amplifier characteristics are highly predictable because the performance is fully specified as a complete unit, unlike discrete solutions. Key specifications for the AD620 instrumentation amplifier are summarized in Figure 2.47.

AD620
LOW POWER, PRECISION IN-AMP IN 8-PIN SO

- One Resistor Sets Gain From 1 to 1,000
- Low Offset Voltage . . . . . .125μV Max
- Low Offset Voltage Drift . . . . . 1.0μV/°C Max
- CMRR . . . . . 93dB, G = 10
- Wide Specified Supply Range . . . ±5V to ±15V
- Low Power . . . . . 900μA typ.
- Low Cost

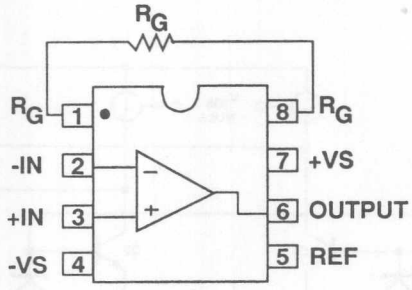


Figure 2.47

INPUT PROTECTION

The inputs of an instrumentation amplifier often come from a harsh environment. For example, unsafe voltages may be present in a factory and damage unprotected amplifier inputs if applied directly. If such a possibility exists, the inputs should be protected. The simplest method is to add resistor in series with each input to limit destructively high levels of current. One should always consult the Absolute Maximum Rating specification in the device data sheet for the maximum allowable input current. If not specified, 10mA is usually safe and may be applied under all overvoltage conditions. Figure 2.48 shows a protection scheme that will withstand +/-160V common-mode and differential overvoltage.

INPUT OVERVOLTAGE PROTECTION

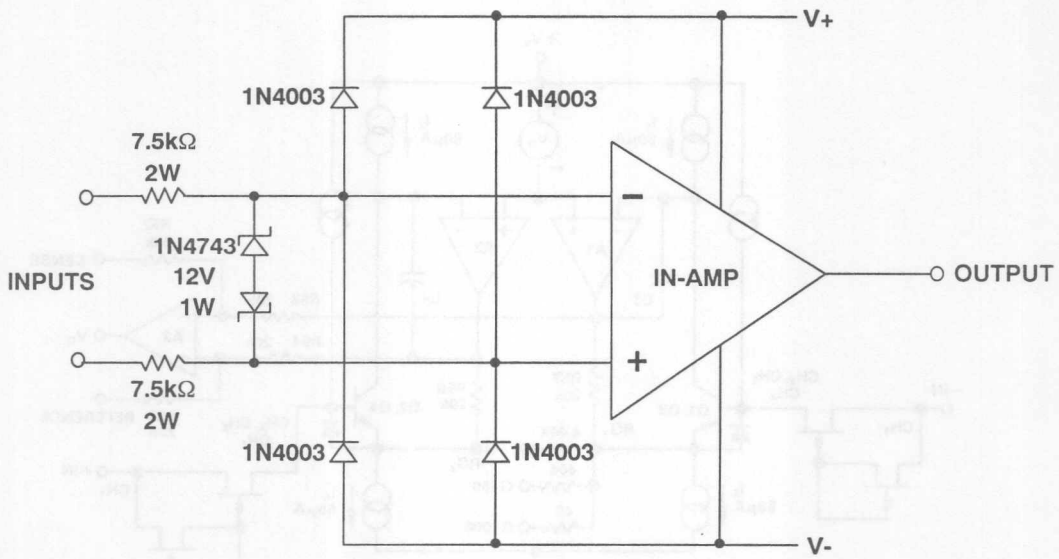


Figure 2.48

While the series input resistors provide overvoltage protection, they also increase the total output noise of the amplifier. Reducing the resistor values reduces the noise but the requires a higher wattage resistor to dissipate the power under full overvoltage conditions.

As mentioned before, some instrumentation amplifiers have built-in input protections. Figure 2.49 and Figure 2.50 show the two different input protection implementations of two different instrumentation amplifiers, the AD524 and the AMP-02, respectively. If additional protection is needed, a series resistor will help.

AD524's INTERNALLY PROTECTED INPUTS CAN WITHSTAND 36V BEYOND EITHER SUPPLY RAIL

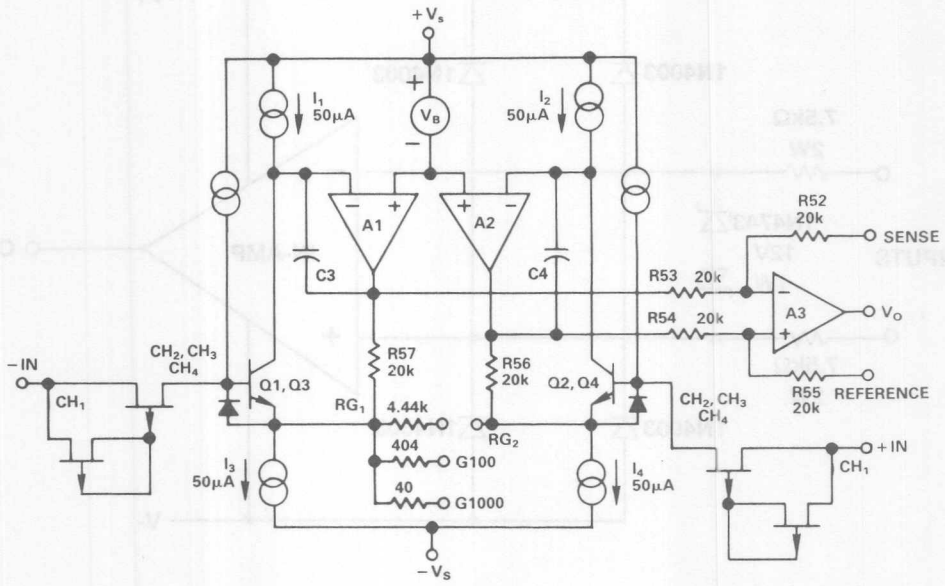


Figure 2.49

AMP-02's INTERNALLY PROTECTED INPUTS ALLOW ± 60V WITHOUT DAMAGE

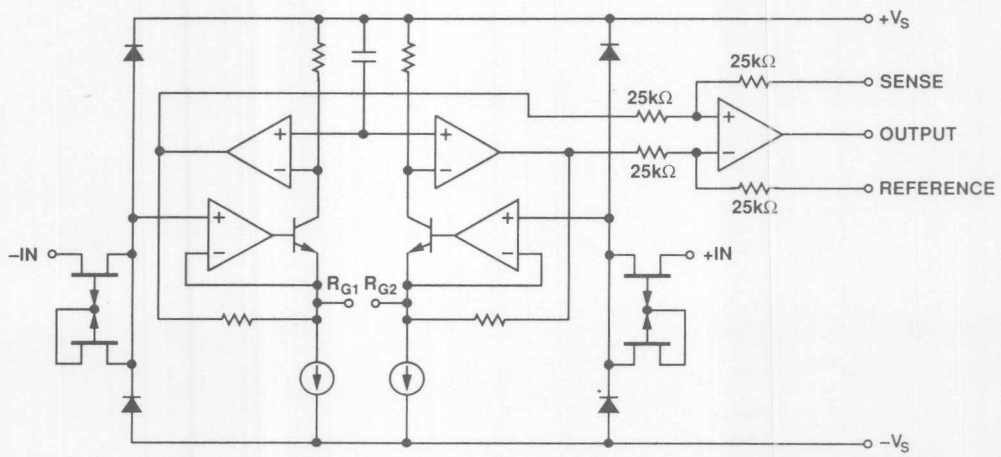


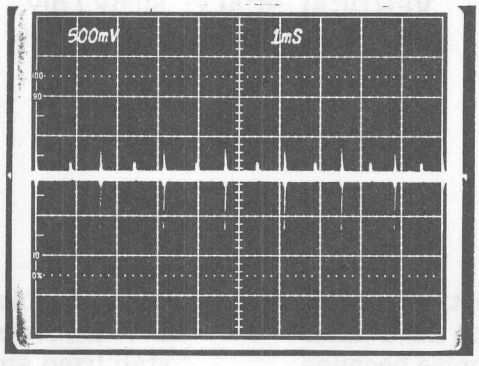
Figure 2.50

CHOPPER STABILIZED AMPLIFIERS

Chopper stabilized amplifiers offer virtually zero offset voltage and offset voltage drift by continuously nulling the offset. While this solves the problem of offset and drift, chopper stabilized amplifiers generate significantly more noise than their counterparts.

There are two sources of noise: glitch noise and intrinsic amplifier noise. The glitch noise amplitude is typically in the 100's of millivolts and is generated by the internal chopping action feeding through to the output. The chopping frequency is usually between a few hundred Hz to greater than 5kHz. Figure 2.51 shows the glitch noise that can be present at the output of a typical chopper amplifier. Adequate filtering is required to remove these glitches.

CHOPPER AMPLIFIERS HAVE SIGNIFICANT GLITCH NOISE AND REQUIRE OUTPUT FILTER



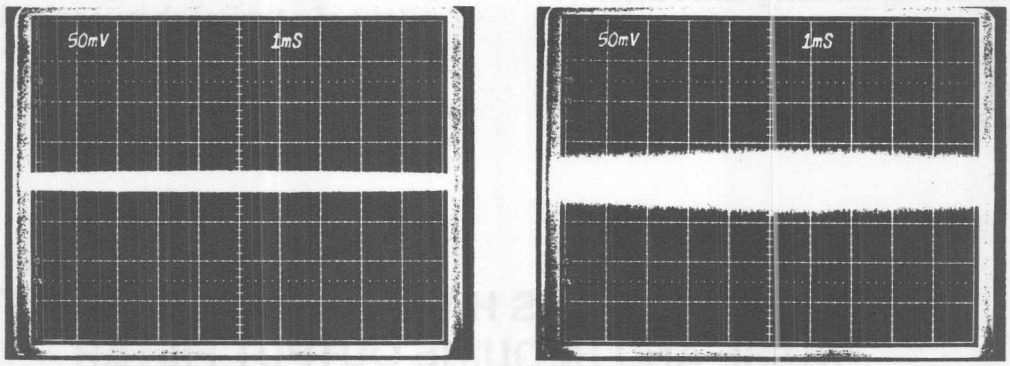
VERTICAL SCALE: 500mV / div.
HORIZONTAL SCALE: 1ms / div.

Figure 2.51

The other noise comes from the 1/f noise and the white noise of the amplifier, which is usually higher than low noise op amps. Figure 2.52 shows the unfiltered noise of a typical chopper stabilized amplifier. If not filtered, it significantly degrades the signal-to-noise performance of an amplifier circuit. Usually a two pole filter is required to reduce this noise to an acceptable level.

BIPOLAR OP AMP VERSUS CHOPPER WIDEBAND (UNFILTERED) NOISE G = 1000

BIPOLAR OP AMP **CHOPPER OP AMP**



VERTICAL SCALE: 50mV / div.
HORIZONTAL SCALE: 1ms / div.

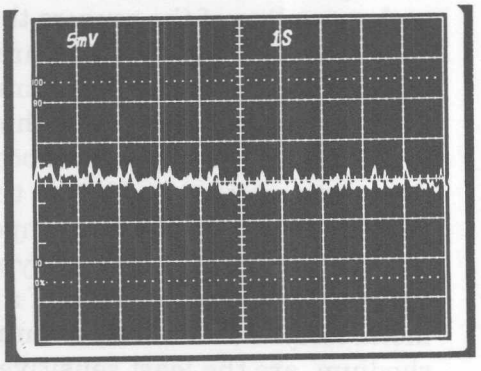
Figure 2.52

It is a common misconception that chopper stabilized amplifiers have inherently lower low-frequency noise because the low frequency noise behaves like an offset and therefore is nulled by the chopping action. This is incorrect because the switching action occurs at the inputs of the amplifier. The finite switch resistances and current noise spikes from the chopping action result in significantly higher noise below 10Hz. Figure 2.53 compares the 10Hz noise of a chopper with a bipolar precision op amp. The OP-177 has lower 10Hz noise than chopper stabilized amplifier.

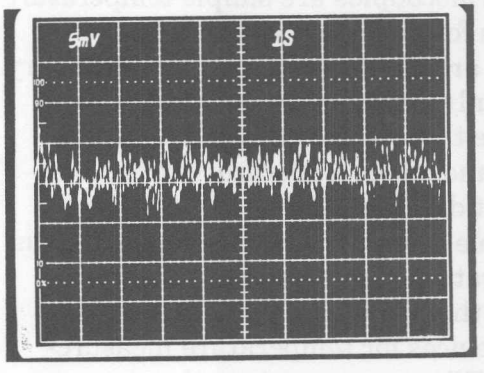
While chopper stabilized amplifiers do serve a useful solution in some applications where offset and drifts are critical, the designer should understand the tradeoffs before a selection is made. A useful comparison between chopper and a precision op amps is given in Figure 2.54.

BIPOLAR OP AMP VERSUS CHOPPER 0.1Hz TO 10Hz NOISE FOR GAIN = 1000

BIPOLAR OP AMP



CHOPPER OP AMP



VERTICAL SCALE: 5mV / div.
HORIZONTAL SCALE: 1s / div.

Figure 2.53

PRECISION OP AMP VERSUS CHOPPER: AN UNBIASED COMPARISON OF CRITICAL PARAMETERS

	BIPOLAR	CHOPPER
OFFSET VOLTAGE	10-50μV	<5μV
OFFSET DRIFT	0.1μV/°C	~0μV
OPEN LOOP GAIN	10 Million	10 Million
NOISE: HF GLITCH	None	>100mVp-p
NOISE: 0.1-10Hz	<0.2μVp-p	>1μVp-p
COST	Lower	Higher
EXTERNAL COMPONENTS	None	Most Require 2 Caps.
SATURATION RECOVERY	10-20μs	>100ms to seconds

Figure 2.54

SIGNAL CONDITIONING FOR TEMPERATURE MEASUREMENT

ADOLFO A. GARCIA

THERMOCOUPLE SIGNAL CONDITIONING

TEMPERATURE-VOLTAGE CHARACTERISTICS OF THERMOCOUPLES

Thermocouples are simple temperature sensors formed when any two dissimilar metals are joined together. They are very commonly used in hostile environments because their rugged construction can withstand wide temperature ranges without damage. These sensors are available in many varieties depending on temperature range and their low cost makes them one of the most commonly used devices for temperature measurement. When compared to other temperature sensors, thermocouples are the least stable and non-linear. Also, their low output voltages require very carefully designed, stable signal conditioning circuitry to keep measurement errors low. It is precisely this issue of signal conditioning for thermocouples that requires an understanding of the sensors themselves.

Illustrated in Figure 2.55 are voltage-temperature curves of four commonly used thermocouples. Of the thermocouples shown, Type J thermocouples are the most sensitive, producing the largest output voltage for a given temperature change. On the other hand, Type S thermocouples, constructed out of a noble metal alloy of platinum/platinum—rhodium, are the least sensitive to temperature changes. These characteristics are very important to consider when designing signal conditioning circuitry in that the thermocouples' relatively low output signals require low-noise, low-drift, high-gain stages.

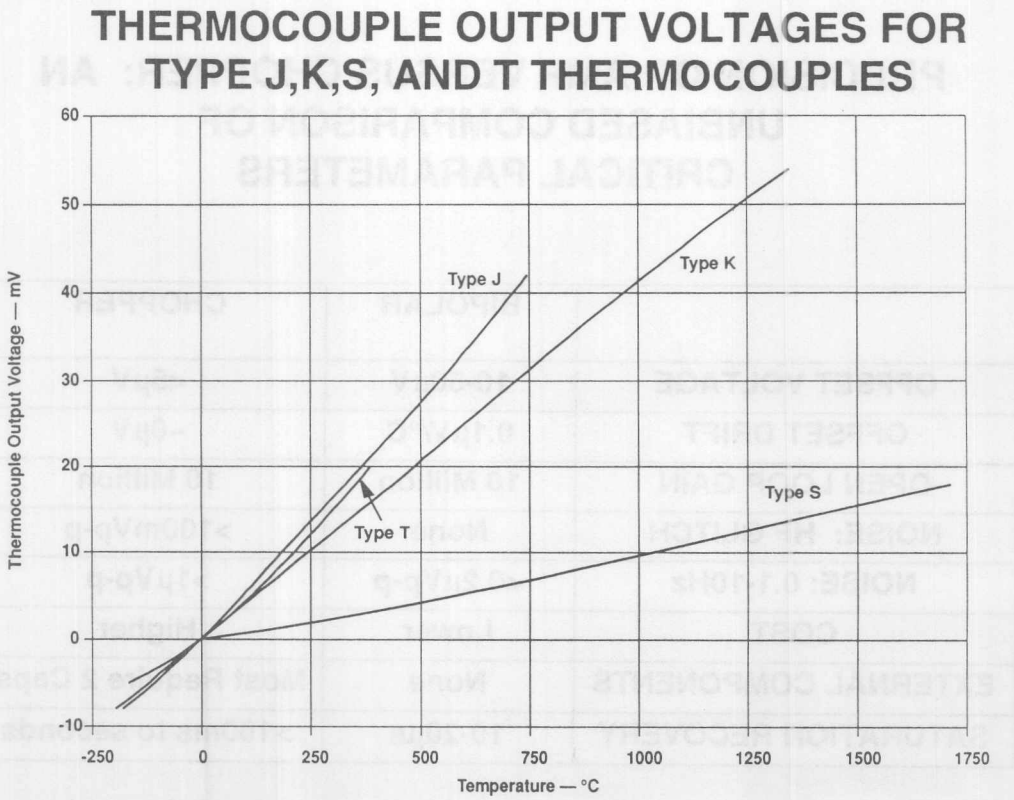


Figure 2.55

Most important in understanding thermocouple response is their non-linear temperature coefficient, or Seebeck coefficient. As was shown in Figure 2.55, each of the four thermocouple responses exhibit a non-linear output voltage versus temperature; however, the key to thermocouple signal conditioning is understanding the behavior of the coefficient of temperature and how it varies over temperature. Shown in Figure 2.56 are the Seebeck coefficients of the four thermocouples as a function of temperature. The important concept to remember when choosing a thermocouple for maximum linearity is selecting the temperature range where a thermocouple's Seebeck coefficient changes are small.

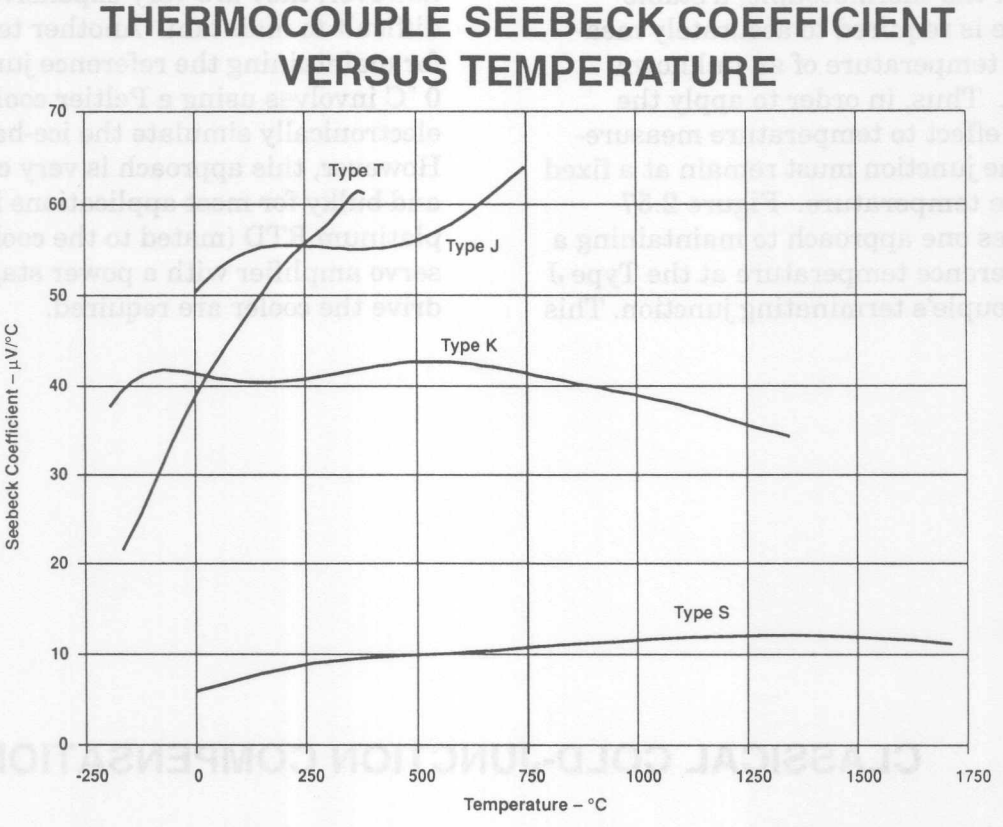


Figure 2.56

For example, a Type J thermocouple's Seebeck coefficient changes less than 1 μV/°C over any part of the range from 200°C to 500 °C. On the other hand, the Type T thermocouple's Seebeck coefficient increases non-linearly with increasing temperature; therefore, designing signal conditioning circuitry around the Type T thermocouple to cover accurately a wide temperature range would be a difficult task.

Presenting these data on thermocouples serves two purposes: Firstly, Figure 2.55 illustrates the range and sensitivity of the four thermocouple types. Thus, the system designer can, at a glance, determine that a Type S thermocouple has the widest useful temperature range, but a Type J thermocouple is more sensitive to temperature changes. Secondly, the variations of Seebeck coefficients provide a quick guide to a thermocouple's linearity, both from a qualitative point of view and a quantitative one. For example, using Figure 2.56, the system designer can choose a Type K thermocouple for its linear Seebeck coefficient over the range of 400 °C to 800 °C or

a Type S over the range of 900 °C to 1700°C. The behavior of a thermocouple's Seebeck coefficient is important in applications where the variations of temperature are key instead of the absolute magnitude. These data also indicate what level of performance is required of the associated signal conditioning circuitry.

PRINCIPLE OF THERMOCOUPLE AND REFERENCE COLD-JUNCTION

Although external excitation is not required because of the inherent voltage output of the thermocouple, a stable reference is required to accurately measure the temperature of an unknown medium. Thus, in order to apply the Seebeck effect to temperature measurement, one junction must remain at a fixed reference temperature. Figure 2.57 illustrates one approach to maintaining a fixed reference temperature at the Type J thermocouple's terminating junction. This solution requires ice-point references which are very accurate and easy to build; however, they are very expensive and difficult to maintain. Another technique for maintaining the reference junction at 0 °C involves using a Peltier cooler to electronically simulate the ice-bath. However, this approach is very complex and bulky for most applications in that a platinum RTD (mated to the cooler) and a servo amplifier with a power stage to drive the cooler are required.

CLASSICAL COLD-JUNCTION COMPENSATION

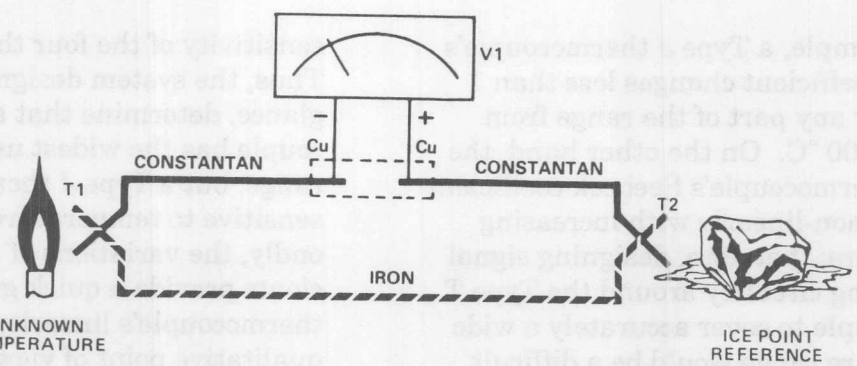


Figure 2.57

The third, and most commonly used approach, is an electronic compensation circuitry that provides an artificial reference level that is allowed to track ambient temperature variations of the reference junction. This approach is shown in Figure 2.58. A temperature sensor, T3, is placed in thermal proximity to the reference junction and generates a voltage, V3, equal to and opposite in polarity to that generated by the cold junction. This voltage is then added to the one produced by the thermocouple circuit. The result of this operation is that the voltage produced by the thermocouple at the measurement temperature. This has the same effect as maintaining the cold junction at a constant temperature, and it offers good accuracy and requires minimal maintenance.

USING A TEMPERATURE SENSOR FOR COLD-JUNCTION COMPENSATION

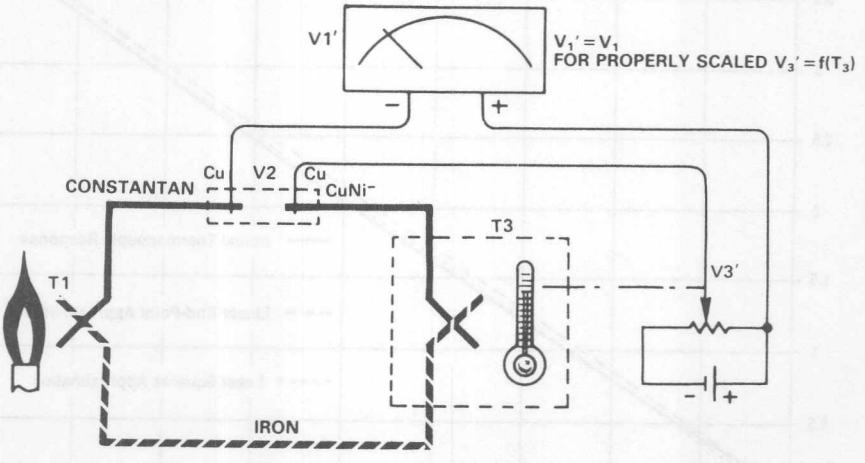


Figure 2.58

THERMOCOUPLE AMPLIFIER DESIGN CONSIDERATIONS

There are a number of ways to approach the design of thermocouple signal conditioning amplifiers. The appropriate thermocouple type for the temperature range should be chosen to reduce the accuracy requirements placed on the circuit design. In selecting the most linear thermocouple for a temperature range allows for straightforward designs with a minimum of components. Tight measurement accuracy over wide temperature ranges increases system costs by requiring more elaborate designs that linearize the thermocouple's inherently non-linear response. The keys to accurate measurements over narrow or wide temperature ranges are to use cold-junction compensation and a thermocouple whose Seebeck coefficient is linear over the temperature range of interest. It is not, however, just that straightforward — in many cases, a designer must use whatever thermocouple is at hand to do the job. To illustrate the issues of thermo-

couple signal conditioning, we'll begin by considering two approaches for a Type T thermocouple amplifier.

Once the measurement temperature range is known, the next step is to decide what type of an approximation will be applied to the thermocouple's non-linear response. As we have shown before, thermocouples do not have a unique and constant Seebeck coefficient over temperature. Hence, some type of linear approximation must be used. For the first example, a signal conditioning amplifier is required for a Type T thermocouple which measures temperatures over the range of 0 °C to 100 °C. As illustrated in Figure 2.59, a Type T thermocouple's response is shown with two linear approximations: end-point and least squares.

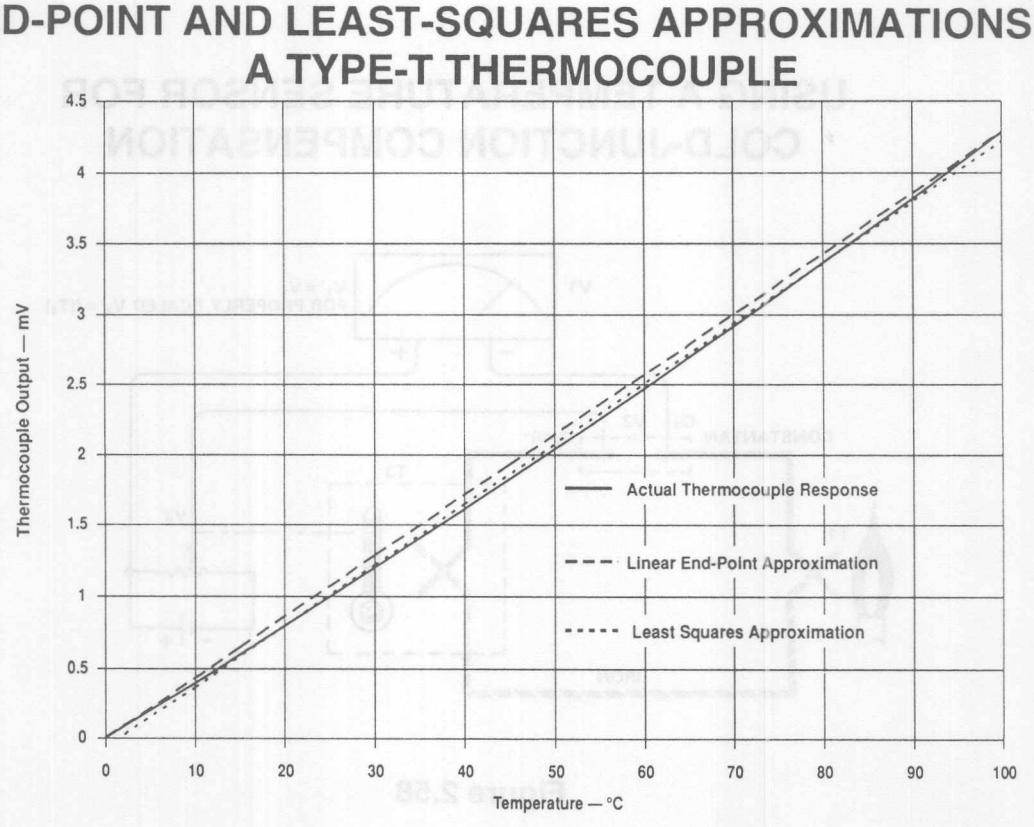


Figure 2.59

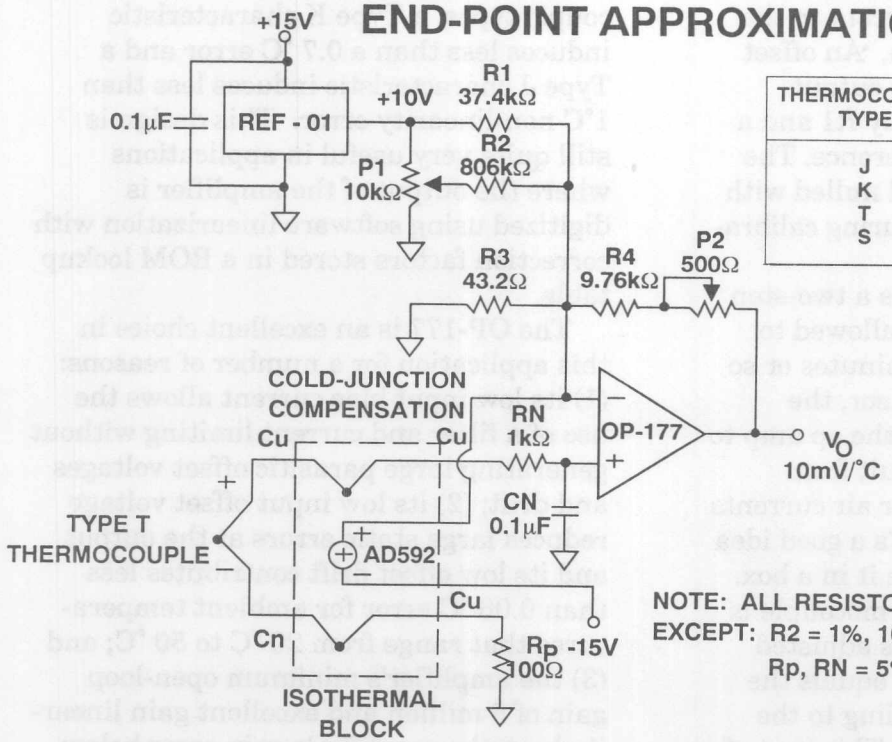
An end-point approximation applies a straight line on the thermocouple's response and intersects the two endpoints of the temperature range. The error in this approximation is zero at the endpoints and is a maximum at the midpoint of the temperature range, which is -2.5 °C at 50 °C in this example. The slope of the approximation is 42.8 μV/°C and is the Seebeck coefficient value when the cold-junction compensator is designed. On the other hand, a least squares approximation to the thermocouple's response intersects the response at two points and exhibits a minimum mean-square error over the temperature range of interest. The error in this example is zero at 20 °C and at 80°C with the maximum error occurring at the midpoint and the endpoints. Typically what happens with this approach is that the error becomes too large at either temperature extreme, and the designer is forced to adjust the slope or the intercept of the line to reduce the overall error. Fortunately, most all scientific calculators make the job easier by providing a least

squares curve fitting capability. The algorithm only works if enough data points are entered. In this example, data points were entered in 5 °C increments from 0 °C to 100 °C, and the approximation yielded an error of -1.5 °C at the endpoints and + 0.9 °C at midscale. This corresponded to a Seebeck coefficient of 42.8 μV/°C and with an intercept of -65 μV. Therefore, the only difference between the two approximations is an offset term. The only way to reduce the error in the approximation, be it end-point or least squares, is to narrow the measurement temperature range or use linearization techniques. Through this example, we have shown that linear approximations to a thermocouple's characteristic are more accurate for small deviations over temperature.

THERMOCOUPLE AMPLIFIER DESIGN #1

To demonstrate the design of a Type T thermocouple amplifier, a Seebeck coefficient of 42.8 μV/°C is used for a circuit which measures temperature over the range of 0 °C to 100 °C to an accuracy of ±0.4 °C. The amplifier, shown in Figure 2.60, is designed to provide a 10 mV/°C output and requires a gain of 233.8 to produce a 1 V output at 100 °C. Changing R3 as shown in the table allows the circuit to accommodate other thermocouple types.

COLD-JUNCTION COMPENSATED GROUNDED TYPE T THERMOCOUPLE AMPLIFIER USING END-POINT APPROXIMATION



THERMOCOUPLE TYPE	SEEBECK COEFFICIENT (0°C ≤ Tm ≤ 100°C)	R3 (Ω)
J	52.68μV/°C	53.6Ω
K	40.95μV/°C	41.2Ω
T	42.8μV/°C	43.2Ω
S	6.45μV/°C	6.49Ω

NOTE: ALL RESISTORS ARE 1% 25 ppm/°C
EXCEPT: R2 = 1%, 100 ppm/°C
Rp, RN = 5% CARBON

Figure 2.60

A grounded thermocouple is used here because this configuration minimizes noise pickup from long leads. Two other components, R_N and C_N, serve as a noise filter to any ambient induced noise that the lead wires pick up. The filter's cutoff frequency of 1.6 kHz can be lowered by, preferably, increasing C_N. Although larger values for R_N can be used at the input of the OP-177, its value should be weighed against input bias-current induced offset and drift effects. Lastly, a resistor, R_P, is used in series with exposed thermocouples as protection in the event that it makes electrical contact to some high voltage potential. Otherwise, the thermocouple would be a dead short to ground and would certainly be destroyed without current limiting.

Cold-junction compensation is achieved using a AD592 monolithic temperature sensor located in thermal proximity to the thermocouple's terminating junction. The sensor continuously monitors the temperature of the cold-junction and provides a temperature-dependent current to the amplifier's summing junction. An offset current equal to the sensor's output current at 0 °C is generated by R1 and a REF-01, a precision 10 V reference. The offset current is summed and nulled with the sensor's initial current during calibration.

Calibration of the circuit is a two-step process. First, the circuit is allowed to warm-up and settle after 5 minutes or so to allow the temperature sensor, the reference, the resistors, and the op amp to stabilize. To protect the circuit from ambient thermal gradients or air currents that can affect calibration, it's a good idea to cover the circuit or enclose it in a box. For 0 °C calibration, the thermocouple is replaced by a short, and P1 is adjusted such that the output voltage equals the ambient temperature, according to the relationship 10 mV/°C • T_A. This part of the procedure trims out initial amplifier offset voltage and bias currents, resistor tolerances, and initial errors in the reference and the temperature sensor. For full-scale span adjust, the short is replaced by a precision dc voltage source with a value equal to the thermocouple's output voltage at 100 °C. For a Type T thermocouple, the voltage source is set to 4.277 mV. P2 is then adjusted such that the output voltage is 1V above the previously measured value; that is, V_{OUT} = 1V + 10 mV/°C • T_A. For example, if the ambient temperature of factory or a lab is 45 °C (whew!!), then P2 is adjusted so that V_{OUT} = 1.45 V.

The largest source of error over this temperature range comes from the approximation made to the thermocouple's characteristic. As we have shown before, a Type T thermocouple, although very sensitive to temperature changes, exhibits a Seebeck coefficient of 38.9 μV/°C at 0 °C that increases to 46.3 μV/°C at 100 °C. Therefore, using a constant 42.8 μV/°C over this range induces a 2.5 °C error in the measurements. For other thermocouple types, a Type K characteristic induces less than a 0.7 °C error and a Type J characteristic induces less than 1°C non-linearity error. This design is still quite very useful in applications where the output of the amplifier is digitized using software linearization with correction factors stored in a ROM lookup table.

The OP-177 is an excellent choice in this application for a number of reasons: (1) its low input bias current allows the use of a filter and current limiting without generating large parasitic offset voltages and drift; (2) its low input offset voltage reduces large static errors at the output and its low offset drift contributes less than 0.06 °C error for ambient temperatures that range from 20 °C to 50 °C; and (3) the amplifier's minimum open-loop gain of 5 million and excellent gain linearity keep the amplifier's gain error below an immeasurable 0.004 °C over the entire ambient temperature range.

THERMOCOUPLE LINEARIZATION TECHNIQUES

To improve measurement accuracy, linearization of the thermocouple's response can be applied. There are a number of techniques that can be used to linearize a thermocouple's characteristic. Some of the techniques are: offset addition, breakpoint correction, analog computation, and digital correction (Reference 1). Offset addition biases the non-linear characteristic with a constant offset. By adding an offset term, a least squares approximation is applied to the thermocouple response. Recall that the approximation's errors are high at the endpoints and low throughout the span. Offset correction can be implemented using the circuit in Figure 2.60 by adjusting the offset current and circuit gain during calibration so that the error in minimized at two points located roughly at one-third and at two-thirds of the measurement range.

Thermocouple non-linearity correction using analog computation techniques uses analog multipliers and operational amplifiers to synthesize a function that describes the thermocouple's voltage-temperature characteristic. For more detailed information on this subject, the interested reader should consult References 2 and 3.

An increasingly popular technique for thermocouple linearization is to digitize the output of an accurate thermocouple amplifier and apply continuous correction to thermocouple output with factors that are stored in ROM (Reference 4). One method uses a power series polynomial to implement the correction and has the form:

$$T = a_0 + a_1X + a_2X^2 + \ldots + a_nX^n$$

where T is the thermocouple temperature, X is the thermoelectric voltage, and a_0, a_1, a_2, ..., and a_n are the coefficients of the polynomial for each type of thermocouple. The coefficients for each thermocouple can be found in Reference 5. Another advantage to digital techniques is the elimination of circuit calibration via trimming potentiometers. Computers and microprocessors can be programmed to execute a calibration sequence at any time and are far more efficient than analog linearization circuits in implementing this algorithm.

Another technique for linearizing a thermocouple's response is to use breakpoints that change the gain of the circuit as the signal increases. Breakpoints use as many straight-line segments as required by system accuracy to fit the thermocouple's characteristic. This approach is circuit intensive in that the number of linear segments determine the number of amplifiers the linearizer requires. In the next example, a design for such a linearizer will be described.

THERMOCOUPLE AMPLIFIER DESIGN #2

Shown in Figure 2.61 is a circuit that uses one breakpoint and two linear segments to approximate a Type T thermocouple's response from 0 °C to 100°C. The input amplifier is built around the AD707 and employs cold-junction compensation using an AD592 temperature sensor. The linearizing circuitry uses an AD706 dual to set the breakpoint of the approximation and changes the gain of the circuit as the signal increases. The output of the amplifier is designed to provide a 10 mV/°C output such that the output is 1 V when the thermocouple is at 100 °C.

COLD-JUNCTION COMPENSATED TYPE T THERMOCOUPLE USING A TWO-SEGMENT APPROXIMATION

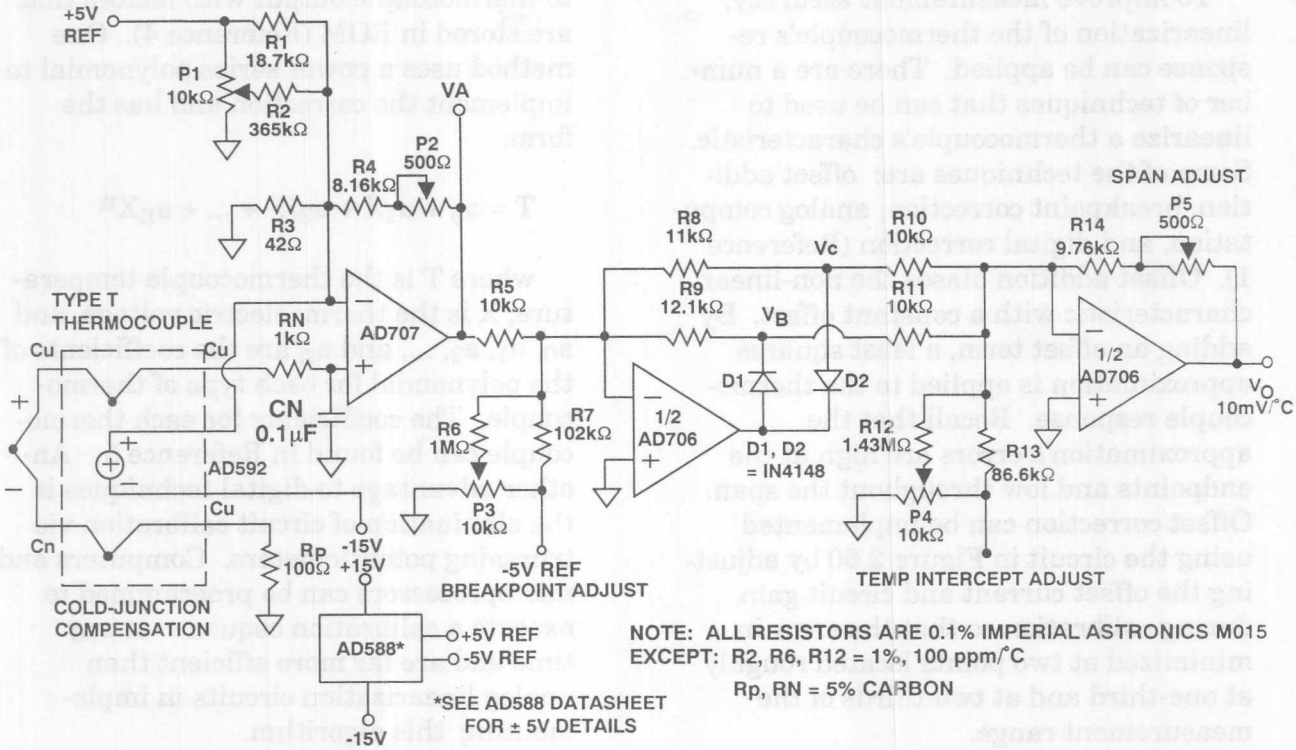


Figure 2.61

The input amplifier is virtually identical to the amplifier in Figure 2.60 except for one twist: although the gain that the thermocouple sees is 200, the cold-junction compensation circuitry is designed to track the terminating junction over a temperature range of 20 °C to 50 °C with a Seebeck coefficient of 41.7 μV/°C. The amplifier is then configured for a fixed gain of 200 to amplify the thermocouple's signal before being applied to the linearizer. An AD588 precision reference is configured for ± 5V and is used in the offset current, breakpoint adjust, and offset temperature adjust circuitry.

Designing the linearizing circuit is a straightforward process. On a piece of paper, a graph is drawn showing the thermocouple's voltage-temperature characteristic from 0 °C to 100 °C and is illustrated in Figure 2.62. On the ordinate is plotted the thermocouple's output voltage, and on the abscissa is plotted the temperature of the thermocouple.

LINEARIZING A TYPE-T THERMOCOUPLE'S RESPONSE USING TWO-SEGMENT APPROXIMATION

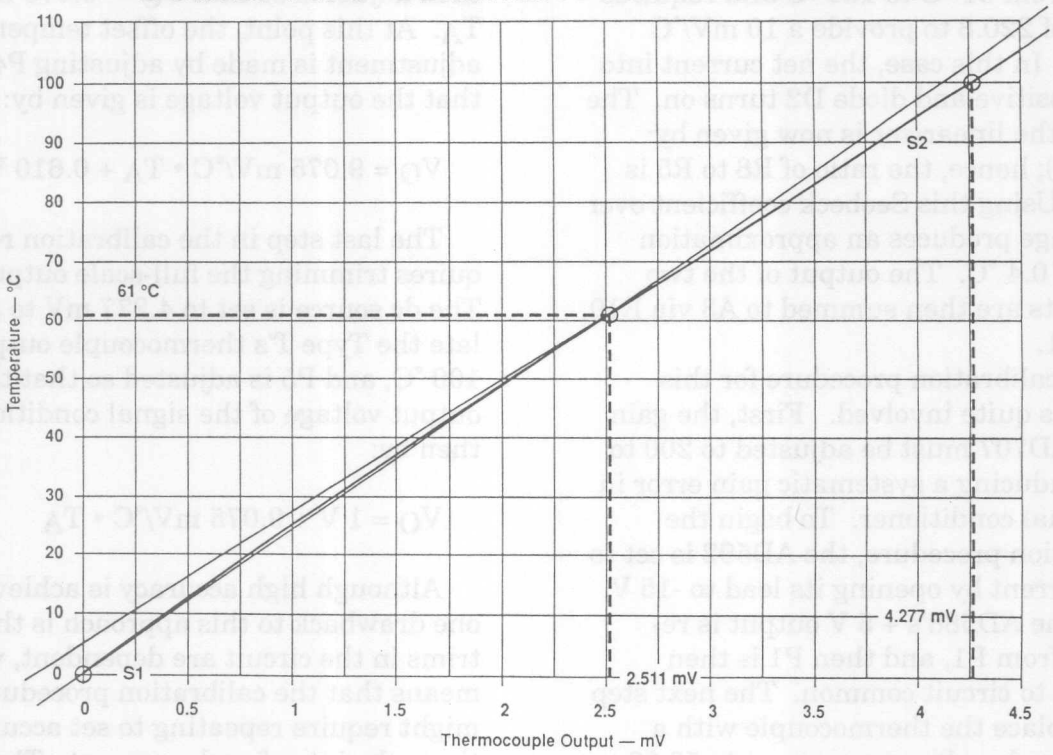


Figure 2.62

Two linear segments are drawn on the graph: S1, starting from the origin toward the full-scale output following the thermocouple's characteristic, and S2, second segment starting at 100 °C back toward the origin. The point of intersection sets the breakpoint for the approximation. The two segments intersect the thermocouple's temperature-voltage characteristic at about 61°C, which corresponds to a thermocouple output voltage of 2.511 mV.

To incorporate both segments into one stage, a high-accuracy dual-slope diode circuit built around the AD706 was used as the core of the linearizer. In order to change the gains in the circuit, there must be zero net current into A2 at the breakpoint. Thus, R7 and the AD588's -5V output are used together to provide that offset current. The breakpoint is set when the output of A1 is 502.2 mV (200 • 2.511 mV). Since the net input current into A2 is zero, both diodes D1 and D2 are turned off, and the net input current into A3 is also zero. At this point, the output of the signal conditioner should reflect a thermocouple temperature of 61 °C or 0.61 V. With A3's feedback network nominally set to 10 kΩ, R13 and the AD588's -5 V output supply another offset current to generate a 0.61 V output.

To set the gains of the linearizer, an equivalent Seebeck coefficient for each segment is calculated. From 0 °C to 61°C, the thermoelectric voltage of the thermocouple is less than 2.511 mV, making A2's net input current negative. Diode D1 turns on and the gain of the linearizer is given by: -(R9/R5). The slope of the first segment yields a Seebeck coefficient of 41.2 μV/°C and requires a gain of 242.9 to produce a 10 mV/°C output. Since the gain of the input stage is 200, the ratio of R9 to R5 is 1.214. The error in the approximation over this range of temperatures is less than 0.8 °C.

The second segment's slope yields 45.3 μV/°C from 61 °C to 100 °C and requires a gain of 220.8 to provide a 10 mV/°C output. In this case, the net current into A2 is positive and diode D2 turns on. The gain of the linearizer is now given by: -(R8/R5); hence, the ratio of R8 to R5 is 1.104. Using this Seebeck coefficient over this range produces an approximation error of 0.4 °C. The output of the two segments are then summed to A3 via R10 and R11.

The calibration procedure for this circuit is quite involved. First, the gain of the AD707 must be adjusted to 200 to avoid inducing a systematic gain error in the signal conditioner. To begin the calibration procedure, the AD592 is set to zero current by opening its lead to -15 V. Next, the AD588's + 5 V output is removed from P1, and then P1 is then shorted to circuit common. The next step is to replace the thermocouple with a precision dc voltage source set to 50.00 mV. P2 is adjusted so that the output of the AD707 is 10.00 V.

The calibration of the signal conditioner for 0 °C trim begins with reconnecting the AD592 and the AD588's + 5 V output back into the circuit. The dc source is set to 0.00 V, and P1 is adjusted so that the output of A1 is 8.338 mV/°C • T_A, the ambient temperature of the circuit. For example, if the ambient temperature were 25 °C, then P1 would be adjusted to set V_A equal to 208.45 mV.

The next step in the procedure is setting the breakpoint of the linearizer. The precision dc source is set to 2.511 mV to simulate the thermocouple's output at 61 °C. Since the AD707's gain was trimmed to 200, its output voltage is given by:

$$V_A = 2.511\ mV \bullet 200 + 8.338\ mV/°C \bullet T_A.$$

At this point, the net input current into A2 is positive and diode D2 is on. P3 is then adjusted so that V_C = -9.075 mV/°C • T_A. At this point, the offset temperature adjustment is made by adjusting P4 so that the output voltage is given by:

$$V_O = 9.075\ mV/°C \bullet T_A + 0.610\ V$$

The last step in the calibration requires trimming the full-scale output. The dc source is set to 4.277 mV to simulate the Type T's thermocouple output at 100 °C, and P5 is adjusted so that the output voltage of the signal conditioner is then by:

$$V_O = 1\ V + 9.075\ mV/°C \bullet T_A$$

Although high accuracy is achievable, one drawback to this approach is that the trims in the circuit are dependent, which means that the calibration procedure might require repeating to set accurately the endpoints of each segment. The simplicity of a digital approach to provide correction at any time is evident when compared to this analog approach.

Once all the adjustments are completed, the precision dc source is removed and the thermocouple is connected. Over an ambient temperature range of 20 °C to 50 °C, the accuracy of the circuit is ± 0.3°C. The largest source of error is in the matching of the resistors used in the linearizer. Tight tolerance, low-TCR resistors are required to minimize trim interactions and segment gain errors. In fact, a 10 kΩ thin-film resistor network can be used for R5, R10, R11, and R14 to help reduce circuit costs. Resistor networks can be acquired with tolerances as tight as 0.1 % and tracking temperature coefficients of 5 ppm/°C. The AD707 and the AD706 work very well in this application because their high open-loop gains, low input offset voltages and currents all combine to induce less than a 0.06 °C measurement error .

THERMOCOUPLE AMPLIFIER DESIGN #3

The design of the linearized Type T thermocouple amplifier can be extended to other thermocouples where in Figure 2.63 is illustrated a circuit that uses an OP-177 and an OP-297 dual operational amplifier to condition a Type S thermocouple's output. The circuit is designed to measure temperatures over the range of 200 °C to 1300 °C and does so to an accuracy of ± 0.5 °C. The measurement accuracy is lower in this circuit because of the larger gain required to scale the thermocouple's output to 10 mV/°C. The design procedure is identical to the Type T design where two segments were used to approximate the thermocouple's characteristic. In this design, the two segments intersect at 800°C where the thermocouple's output is 7.345 mV. From 200 °C to 800 °C, the approximation yields a Seebeck coefficient of 9.84 μV/°C with an error of 16 °C. Over the range of 800 °C to 1300 °C, the second segment uses a Seebeck coefficient of 11.7 μV/°C and exhibits an approximation error of 8 °C. To reduce the approximation errors, a narrower temperature range could have been chosen or more segments could have been used albeit at the price of increased circuit complexity and cost.

COLD-JUNCTION COMPENSATED TYPE S THERMOCOUPLE AMPLIFIER USING A TWO-SEGMENT APPROXIMATION OPERATING OVER 200° TO 1300°C

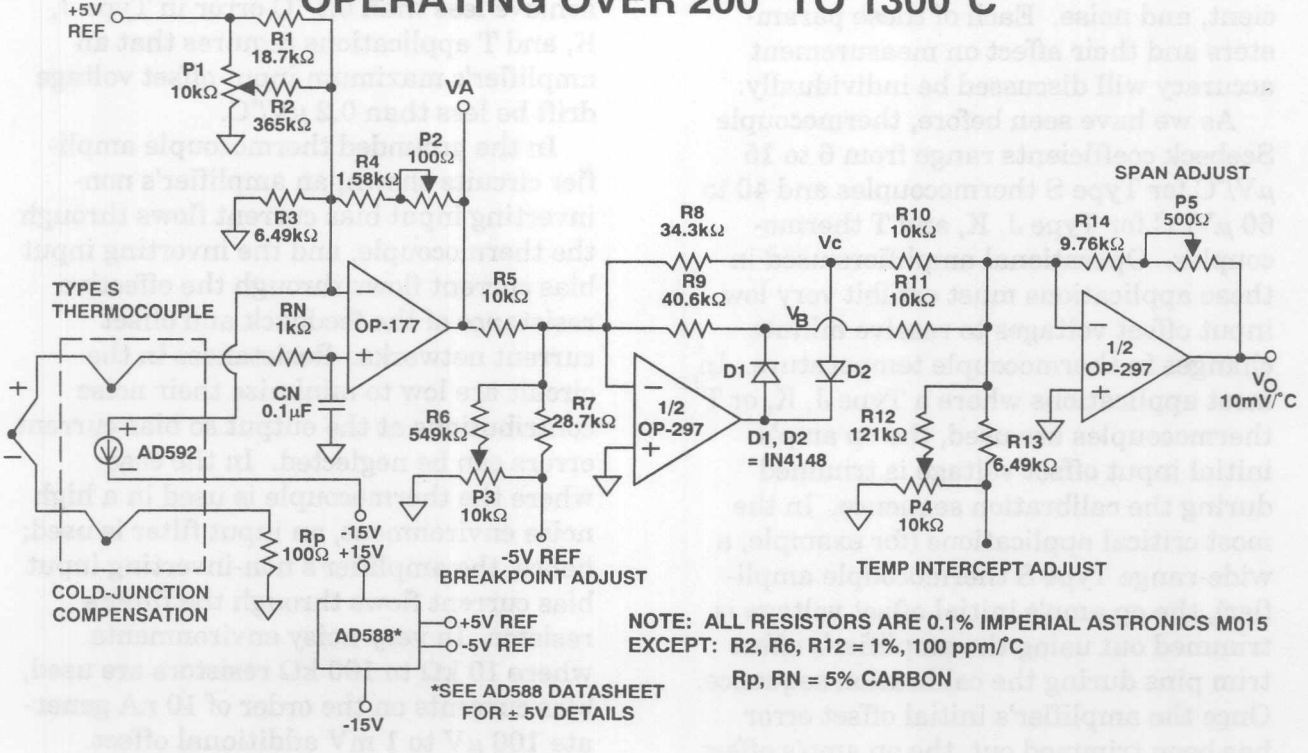


Figure 2.63

COMMON PITFALLS OF THERMOCOUPLE AMPLIFIER CIRCUITS

At this point, it is germane to discuss other circuit errors that doom thermocouple circuit accuracy. To achieve good accuracy in these systems requires diligence and care because, in general, achieving system accuracies better than 0.5 °C is very difficult. Thermocouple non-linearities notwithstanding, major (but common) pitfalls that affect accuracy include amplifier errors, choosing the right resistor tolerance and temperature coefficient, cold-junction considerations, and printed circuit board errors.

OPERATIONAL AMPLIFIER ERRORS

A critical design consideration in thermocouple signal conditioning is minimizing measurements errors in the recording equipment. The operational amplifier is a key element to accurate temperature measurement. Using the wrong one would ruin the measurement no matter how accurate the associated circuitry might be. The parameters that most affect the overall accuracy of the measurements are input offset voltage and drift, input bias current and drift, open-loop gain and temperature coefficient, and noise. Each of these parameters and their affect on measurement accuracy will discussed be individually.

As we have seen before, thermocouple Seebeck coefficients range from 6 to 15 μV/°C for Type S thermocouples and 40 to 60 μV/°C for Type J, K, and T thermocouples. Operational amplifiers used in these applications must exhibit very low input offset voltages to resolve minute changes in thermocouple temperature. In most applications where a Type J, K, or T thermocouples are used, the op amp's initial input offset voltage is trimmed during the calibration sequence. In the most critical applications (for example, a wide-range Type S thermocouple amplifier), the op amp's initial offset voltage is trimmed out using the amplifier's offset trim pins during the calibration sequence. Once the amplifier's initial offset error has been trimmed out, the op amp's offset voltage drift can contribute a significant measurement error. The offset voltage drift appears in series with the thermocouple signal and is amplified to the output. For example, in the Type T amplifier design, if an amplifier that exhibits a 1 μV/°C offset drift were used, the error at the output over a 25 °C change in ambient temperature is 0.6 °C (Drift error = 1 μV/°C • 25 °C • 233.8 ÷ 10 mV/°C). In a Type S thermocouple amplifier, this drift would induce an error of approximately 4 °C over the same ambient conditions. In these applications, halving in the input offset voltage drift halves the output measurement error. To achieve less than 0.1 °C error in Type J, K, and T applications requires that an amplifier's maximum input offset voltage drift be less than 0.2 μV/°C.

In the grounded thermocouple amplifier circuits shown, an amplifier's non-inverting input bias current flows through the thermocouple, and the inverting input bias current flows through the effective resistance of the feedback and offset current networks. Resistances in the circuit are low to minimize their noise contributions at the output so bias current errors can be neglected. In the case where the thermocouple is used in a high noise environment, an input filter is used; hence, the amplifier's non-inverting input bias current flows through the filter's resistor. In very noisy environments where 10 kΩ to 100 kΩ resistors are used, bias currents on the order of 10 nA generate 100 μV to 1 mV additional offset. Although these initial bias current errors might be trimmed at calibration, low input bias current drift is required to

minimize measurement error over temperature. Hence, to achieve less than 0.1°C error over a 25°C change in ambient temperature requires an operational amplifier whose input bias current drift is less than 2 pA/°C when series resistors as high as 100 kΩ are used.

In each of the circuits illustrated thus far, the gain factors of the amplifiers were set to provide a 10 mV/°C outputs which allows the temperature to be converted into digital form using standard analog-to-digital converters or to be read directly off a 4 1/2- or a 5 1/2-digit precision digital voltmeter. Each of these circuits used a single high-gain stage to amplify the thermocouple's output. For the thermocouples discussed, the closed-loop gains range from 190 for Type J thermocouples to over 1500 for Type S thermocouples. If an output scaling of 100 mV/°C were used, all these gain factors would increase by an order of magnitude. High open-loop gain operational amplifiers are required for these applications to minimize gain-errors that produce false readings. To see how this works, recall from feedback theory that the exact expression for the closed-loop gain of an amplifier is given by:

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{1}{\beta}\left(\frac{1}{1+\frac{1}{a\beta}}\right)$$

where A = the amplifier's closed-loop gain,

a = the amplifier's open-loop gain, and

β = the amplifier's feedback factor

Differentiating the closed-loop gain with respect to the open-loop gain and manipulating the algebra yields the sensitivity of the closed-loop gain (and, therefore, the output voltage) to the open-loop gain. This is given by:

$$\frac{dA}{A} = \frac{1}{1+a\beta} \bullet \frac{da}{a}$$

For example, let's say that a Type J thermocouple amplifier requires a closed-loop gain of 2000 to produce a 100 mV/°C output. If an op amp with an open-loop gain of 75,000 is used, the amplifier's initial gain error would be 2.6 % which can be trimmed during calibration. However, over temperature, that open-loop gain could change as much as 25 % which would then cause a gain-error of 3.5 % or 0.7 °C. If, on the other hand, an amplifier with an open-loop gain of 1 million were used, then the gain error over temperature would be less than 0.27 % or 0.06 °C. Therefore, to keep open-loop gain errors below 0.1 °C, the minimum recommended open-loop gain for Type J, K, and T thermocouples is 500,000. For Type S thermocouples amplifiers with 10 mV/°C outputs, the recommended open-loop gain of 500,000 is sufficient.

Another cause of measurement inaccuracy is operational amplifier noise. This error most greatly affects Type S thermocouple signal conditioning amplifiers which must resolve microvolts of thermocouple output. Wide-band circuit noise ultimately determines how small a signal the amplifier can resolve. To minimize an amplifier's noise, here are a few tips: (1) Design the circuit with low resistances – Using low resistances minimizes the effect of amplifier current noise flowing through the effective resistances appearing at the amplifier's input terminals. Using low-value resistors in the design also reduces their thermal noise and stray radio-frequency noise pick-up. For example, reconsider the first thermocouple amplifier design. Although the circuit required a gain of 233.8 to amplify the thermocouple's signal, the effective resistances at the amplifiers terminals were 43Ω (at IN-) and 1.1 kΩ (at IN+). These low resistances, coupled with the OP-177's

low input noise voltage of 11 nV/√Hz and low input current noise of 0.17 pA/√Hz, only increased the total equivalent input referred noise to 11.8 nV/√Hz. The idea here is to let the amplifier's input voltage noise dominate. (2) Restrict the system bandwidth – Noise is generated outside the circuit and is all around it. External noise can best be dealt with by filtering, either at the thermocouple output or at the amplifier's output. The power supply leads are also a wonderful way high frequency supply noise can enter the circuit. In these applications (and most others that require high precision), we often recommend a stiff 10 μF tantalum electrolytic capacitor in parallel with a 0.1 μF or 0.01 μF ceramic disk capacitor right at the amplifier's supply pins. (3) Select a low-noise operational amplifier – Operational amplifiers that fall under the category of "high-accuracy" are specifically designed with input stages which use high currents and input bias current cancellation schemes to lower input voltage and current noise. For this reason, amplifiers used for thermocouple applications should exhibit less than 15 nV/√Hz equivalent input voltage noise.

Operational amplifiers such as the OP-177 and the AD707 are ideal amplifiers for these applications because they meet all the critical specifications that thermocouple signal conditioning requires. Both devices exhibit very high open-loop gains, excellent gain linearity, low input offset voltages and drift, low input bias currents, and low noise. For less critical applications, the AD705 and the OP-97 (and their duals, the AD706 and the OP-297) should be also considered as excellent thermocouple amplifiers for their high open-loop gains, low input offset voltages, very low input bias currents and drift (100 pA, 0.3 pA/°C), low noise, and low supply currents.

RESISTORS AND POTENTIOMETERS

Careful selection of resistors also greatly affects the accuracy of thermocouple signal conditioning amplifiers. Carbon composition resistors should not be used anywhere in the circuit except for input filtering and current-limiting protection for the thermocouple. In this role, their absolute value and temperature coefficient are unimportant. Referring to the circuit in Figure 2.60, R1, R3, and R4 should be precision wirewound or metal film resistors with 1 % tolerance and temperature coefficients of 25 ppm/°C. Measurement inaccuracies over temperature are dominated by these resistors and add a ± 0.2 °C error over a 25 °C change in ambient temperature. Using lower TCR resistors lowers this error but increases circuit cost. Loose tolerance resistors should be avoided because wide trim ranges would be required which would degrade circuit accuracy. R2's TCR, on the other hand, is not that critical in this application and a 1 %, 100 ppm/°C resistor is good enough.

In the examples of thermocouple signal conditioning circuits, trimming potentiometers are used for calibrating the circuit's response at two points, usually at zero and at full-scale. Although useful, trimming can lead to very large circuit errors if done improperly. In all the designs, potentiometers are placed where their absolute resistance is not important and their temperature coefficient is not critical. For example, in the first thermocouple amplifier design, the amplifier's nominal feedback network is 10 kΩ which is made up of a 9.76 kΩ resistor in series with a 500 Ω rheostat-connected potentiometer. The value of the potentiometer to achieve trim is roughly at 50 % of its value (i.e, trim range = 250 Ω ÷ 10 kΩ • 100 = 2.5 %).

What this means is that non-linearities of the potentiometer are avoided because mid-range values are more well-behaved than end-range values. Let's look at what happens to the feedback network over temperature. In these applications, R4 should be a 25 ppm/°C resistor, and cermet potentiometers typically exhibit a temperature coefficient of 100 ppm/°C. If the nominal feedback resistance were trimmed to 10 kΩ during calibration, then over a 25 °C change in ambient temperature the feedback network resistance would only increase by 7 Ω for an error of less than 0.02 °C. The same approach is used for trimming the offset current for cold-junction compensation. In this case, R2 is chosen so that the trim range is again 2 — 5 % of the total offset current required to bring the circuit in trim. So the moral of the story is: do your homework when it comes to applying trimming potentiometers to high accuracy circuits and use multi-turn stable cermet potentiometers for setting accuracy and low cost.

MAINTAINING PROPER COLD-JUNCTION COMPENSATION

One of the largest sources of error in thermocouple signal conditioning circuits is the failure of maintaining proper cold-junction compensation. Since a thermocouple's output voltage is a function of the temperature difference between its two junctions, any temperature delta between the terminating junction and the cold-junction temperature sensor will produce an error signal equal to their difference. It is therefore imperative that the layout of the temperature sensor and the thermocouple's terminating junction minimize any effects due to temperature gradients that might exist. Many times errors are inadvertently introduced when the cold junction is not properly transferred to the PC board. An example of transferring the cold junction to the pc board is shown in Figure 2.64.

TRANSFERRING THE COLD-JUNCTION FROM AN ENCLOSURE OR CONNECTOR TO THE PCB

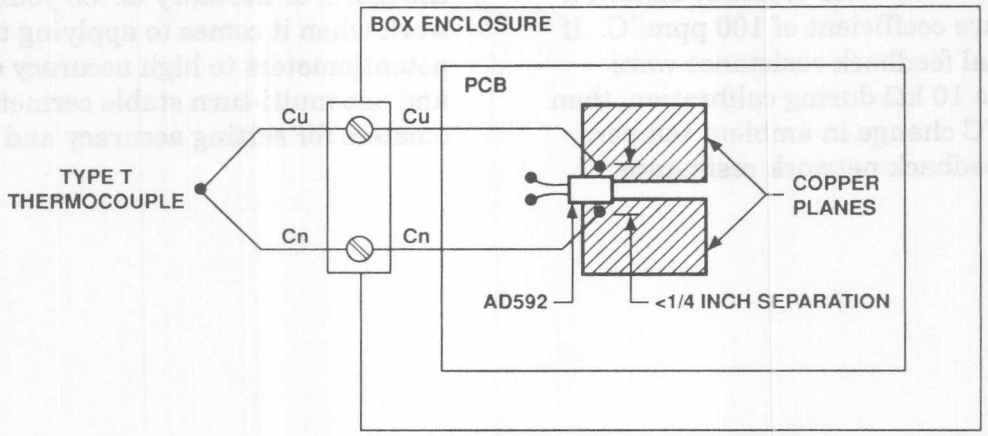


Figure 2.64

The layout illustrates how to extend properly the cold-junction reference plane from the terminal block (or connector) to the pc board, and how to locate the temperature sensor with reference to the thermocouple's terminating junction.

Bear in mind that the extension wires from the terminal block (or connector) to the pc board must be of the same wire type as that used for the thermocouple wires.

MINIMIZING PARASITIC PCB THERMOCOUPLE ERRORS

Thermocouple voltages are generated whenever dissimilar materials are joined. This includes the leads of IC packages, which may be kovar in TO-5 cans, alloy—42 or copper in dual-in-line packages, and a variety of other materials in plating finishes and solders. The net effect of these thermocouples is "zero" if all are at exactly the same temperature, but temperature gradients exist within IC packages and across printed circuit boards whenever power is dissipated. It is for this reason that extreme care must be used to ensure that no temperature gradients exist in the vicinity of thermocouple junctions, the temperature sensor, or the thermocouple amplifier. If a gradient cannot be eliminated, leads should be positioned isothermally, especially the temperature sensor, the amplifier inputs pins and the gain setting resistor leads. When the leads are positioned isothermally, parasitic thermocouple junctions cancel each other out because the leads

are placed orthogonal to the temperature gradient. These critical components must also be placed as closely together as possible to prevent varying temperature gradients from affecting the components as well. To illustrate these two issues, Figure 2.65 is an example of a printed circuit board layout illustrating the isothermal placement and tight arrangement of the thermocouple terminating junction, the temperature sensor, the amplifier input pins, and the gain setting resistors.

An effect to watch for is amplifier offset voltage warm-up drift caused by mismatched thermocouple materials in the wire bond/lead system of the package. This effect can be as high as tens of microvolts in TO-5 cans with kovar leads. It has nothing to do with the actual offset drift specification and can occur in amplifiers with measured "zero" drift. Warm-up drift is directly proportional to amplifier power dissipation and can be minimized by avoiding TO-5 cans, using low-supply current amplifiers, and by using the lowest possible supply voltages. Finally, it can be accommodated by calibrating and specifying the system after a five minute warm-up period.

PROPERLY LOCATING ALL COMPONENTS THAT ARE SENSITIVE TO THERMAL GRADIENTS

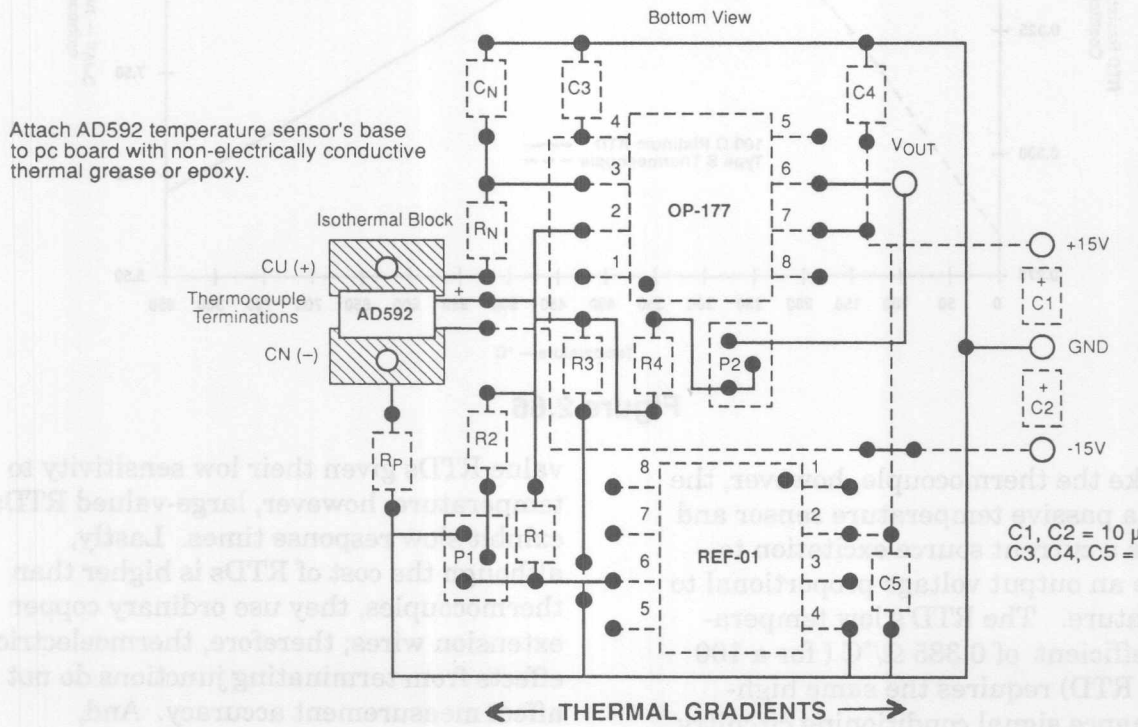


Figure 2.65

RESISTANCE TEMPERATURE DETECTOR (RTD) SIGNAL CONDITIONING

Of the commonly used temperature transducers, the resistance temperature detector, or the RTD, is one type of sensor whose resistance changes with temperature. Typically built of a platinum wire wrapped around a ceramic bobbin, the RTD exhibits a resistance versus temperature behavior which is more accurate and more linear over wide temperature ranges than a thermocouple. Figure 2.66 illustrates the resistance temperature coefficient of a 100-ohm RTD and the Seebeck coefficient of a Type S thermocouple. Over the entire temperature range, the RTD is a more linear temperature sensing device. Hence, linearizing an RTD's response requires less complexity than a thermocouple.

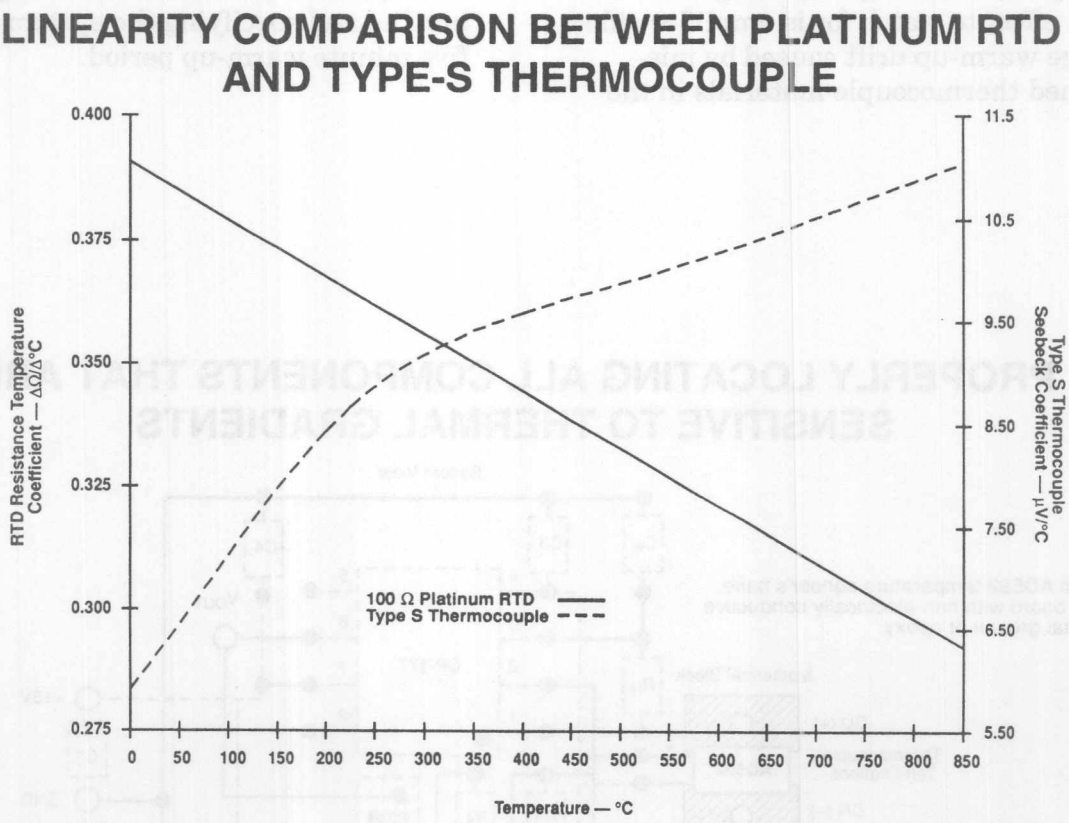


Figure 2.66

Unlike the thermocouple, however, the RTD is a passive temperature sensor and requires a current source excitation to produce an output voltage proportional to temperature. The RTD's low temperature coefficient of 0.385 Ω/°C (for a 100 ohm Pt RTD) requires the same high-performance signal conditioning circuitry as the thermocouple; however, the voltage drop across an RTD is a much larger signal than a thermocouple output voltage. A system designer may opt for large value RTDs given their low sensitivity to temperature; however, large-valued RTDs exhibit slow response times. Lastly, although the cost of RTDs is higher than thermocouples, they use ordinary copper extension wires; therefore, thermoelectric effects from terminating junctions do not affect measurement accuracy. And, because their resistance is a function of the absolute temperature, RTDs require no cold-junction compensation circuitry.

SECOND-ORDER EFFECTS

Caution must be exercised using current source excitation because the current through the RTD causes Joule, or I^2R, heating within the RTD. This self-heating effect changes the temperature of the RTD and appears as a measurement error. Hence, careful attention must be paid during the design of the signal conditioning circuitry so that self-heating is kept below a typical value of 0.5 °C/mW in free air. Manufacturers typically specify self-heating errors for various RTD values and sizes in still and in moving air. To reduce the error due to self-heating, the smallest amount of current through the RTD should be used for the required system resolution, and the largest RTD value should be chosen that results in an acceptable response time.

Another effect that can produce measurement error is that due to RTD lead wires. This is especially critical in low-valued, 2-wire RTDs because the temperature coefficient and the absolute value of the RTD are both small quantities. If the RTD is located a long distance from the signal conditioning circuitry, then the lead wires can be on the order of ohms or tens of ohms. Therefore, a small amount of lead resistance can contribute a significant error to the temperature measurement. To illustrate this point, let us assume that a 100-Ω platinum RTD with 30-gauge copper lead wires is used in a carpet manufacturing facility to sense the temperature of an adhesive and is located about 100 feet from a controller's display console. Since the resistance of 30-gauge copper wire is 0.105 Ω/ft, then the two leads of the RTD contribute a total 21 Ω to the network which is shown in Figure 2.67. This additional resistance will induce a 55 °C error in the measurement! Also not included in this example is the effect of the lead wires' temperature coefficient which can contribute an additional, and possibly significant, error to the measurement. To alleviate the effect of the lead wires, a 4-wire technique is used.

A 100Ω PLATINUM RTD WITH 100 FEET OF 30-GUAGE LEAD WIRES

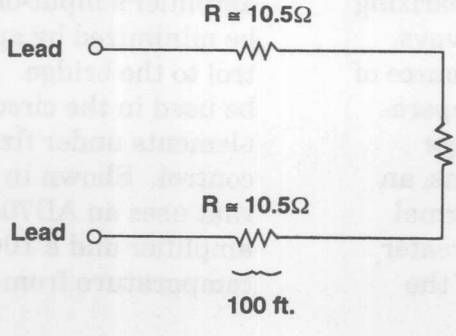


Figure 2.67

As shown in Figure 2.68, a 4-wire, or Kelvin, connection is made to the RTD. A constant current is applied though the FORCE leads of the RTD and the voltage drop can be measured remotely via the SENSE leads. The measuring device can be a DVM or an instrumentation amplifier, and high accuracy can be achieved provided that the measuring device exhibits high input impedance or low input bias currents. Since the SENSE leads do not carry current, this approach is insensitive to lead wire length. Sources of errors in this approach are the stability of the constant current source and the input impedance of the DVM or bias currents in the amplifier.

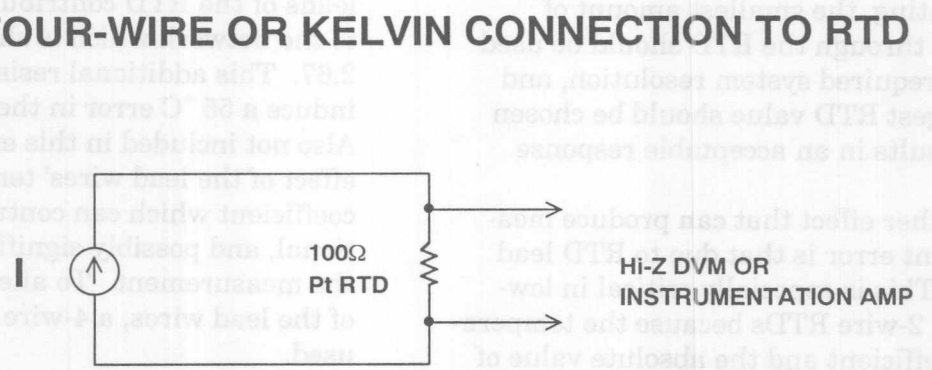


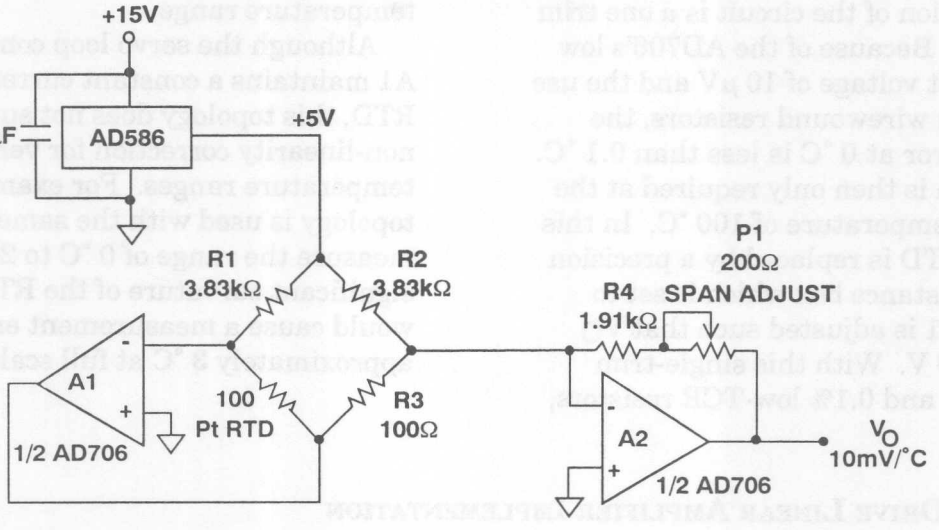
Figure 2.68

BRIDGE AMPLIFIER IMPLEMENTATION

Bridge circuits used in RTD signal conditioning do quite a nice job linearizing transducer outputs. They don't always, however, compensate for a major source of bridge-instrumentation error: an operational amplifier's input-offset-voltage drift. In many bridge circuit designs, an amplifier's input-offset-voltage thermal drift can be amplified four times greater than the sensor's signal because of the bridge's voltage-divider effects.

Without sacrificing linearity, an amplifier's input-offset-voltage drift can be minimized by applying feedback control to the bridge. A pair of op amps can be used in the circuit to place all bridge elements under fixed bias or feedback control. Shown in Figure 2.69 is a circuit that uses an AD706 dual operational amplifier and a 100 Ω Pt RTD to measure temperature from 0 °C to 100 °C.

RTD BRIDGE AMPLIFIER



NOTE: ALL FIXED RESISTORS ARE 0.1% IMPERIAL ASTRONICS M015

Figure 2.69

A1's inverting sum node forces a null at one bridge node such that a constant current, developed by the AD586 and R1, flows through the RTD. Amplifier A2 is then used to establish a null at the other bridge node. Therefore, any variation of the RTD over temperature generates a signal voltage at the output of A1 which is then developed into a signal current for A2 by R3. This signal current is then compared to the current generated by the reference's 5 V output and R2, with the result scaled by R4 to provide a 10 mV/°C output. Since the AD706's input bias currents are typically 30 pA, their error contribution can be neglected. Thus, a simplified equation for the output voltage is given by:

$$V_O = \frac{R_4}{R_3} \bullet \frac{\Delta R}{R_1} V_{REF} + V_{OS2}\left(1 + \frac{R_4}{R_2}\right)$$
$$= \frac{R_4}{R_3}\left(V_{OS2} - V_{OS1}\right)$$

where ΔR is the change in the RTD's resistance over temperature from its 0 °C value. Substituting in values for the resistors yields:

$$V_O = 25.85E\text{-}3 \bullet \Delta R + 1.52 \bullet V_{OS2} + 19.8 \bullet (V_{OS2} - V_{OS1})$$

The circuit's response is now dominated by the RTD and the circuit achieves a much lower sensitivity to amplifier input offset voltage and drift. By placing the RTD in the feedback path of A1, A1's input offset voltage effects at the output are effectively suppressed and the circuit's response is very accurate. Although the output AD706's input offset voltage term appears at the output, it is not amplified by the same gain as in conventional approaches and introduces less than 0.002°C error at 0 °C and 0.04 °C error

over a 20 °C to 50 °C range in ambient temperature.

Calibration of the circuit is a one trim procedure. Because of the AD706's low initial offset voltage of 10 μV and the use of precision wirewound resistors, the circuit's error at 0 °C is less than 0.1 °C. Calibration is then only required at the full-scale temperature of 100 °C. In this case, the RTD is replaced by a precision decade resistance box which is set to 138.5 Ω. P1 is adjusted such that V_O equals 1.00 V. With this single-trim calibration and 0.1% low-TCR resistors, the measurement error is better than ±0.2 °C over a 20 °C to 50 °C ambient temperature range.

Although the servo loop controlled by A1 maintains a constant current in the RTD, this topology does not supply RTD non-linearity correction for very wide temperature ranges. For example, if this topology is used with the same RTD to measure the range of 0 °C to 200 °C, significant curvature of the RTD response would cause a measurement error of approximately 3 °C at full scale.

CURRENT DRIVE LINEAR AMPLIFIER IMPLEMENTATION

It was previously pointed out that the lead wires in a remotely located, low-valued RTD will introduce a measurement error. For example, a 2.6 °C error occurs for every ohm of lead wire resistance in a 100 Ω Pt RTD. In these applications, a 4-wire connection to the RTD should be used to eliminate the effect of lead wires. Figure 2.70 shows a circuit that uses a remotely located, 4-wire connection to the RTD and measures temperature from 0 °C to 100 °C with an accuracy of ± 0.8 °C.

FOUR-WIRE LINEAR AMPLIFIER WITH CONSTANT CURRENT SOURCE EXCITATION

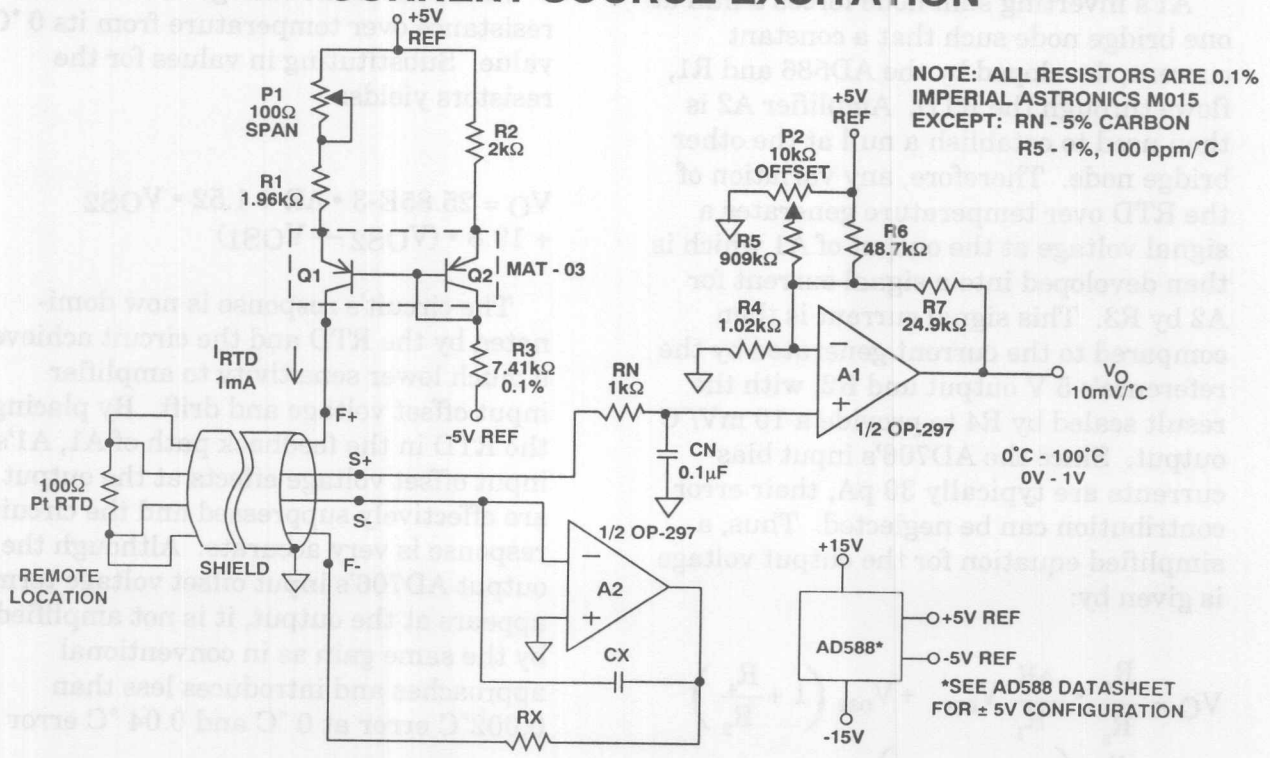


Figure 2.70

In this circuit, a 1 mA constant current is applied to the RTD, and the voltage developed across it is amplified by A1 to provide a 10 mV/°C output. What is unique about this circuit is that A2 servos the return end of the RTD to zero volts thereby eliminating the error induced by the lead wire. The only error the OP-297 introduces after trim is input offset voltage drift. For a 25 °C change in ambient temperature, the error is less than 0.04°C. For very remote locations where the parasitic capacitance of the cable might cause problems for the amplifier, R_X and C_X can compensate A2's response without loss of accuracy.

The 1 mA constant-current source consists of a matched pair of MAT-03 transistors and low-TCR precision resistors. In order to insure that the current source has a low sensitivity to its supply voltages, an AD588 precision voltage reference is configured for ± 5V outputs to drive the current mirror. The AD588's low 3 ppm/°C drift for ± 5 V outputs keeps its error contribution below ± 0.03 °C over a 25 °C change in ambient temperature. R2 and R3 set Q2's collector current accurately to 1 mA which is mirrored over to Q1. To adjust the RTD's current exactly for the full-scale span, a 100 Ω rheostat-connected potentiometer is provided in series with R1.

The gain of amplifier A1 is determined by the change in the RTD's resistance over the temperature range. From 0 °C to 100 °C, the change in the resistance of the RTD is 38.5 Ω. Using a 1 mA constant-current excitation, the full-scale voltage change is 38.5 mV; therefore, to produce a 1 V full-scale output requires a gain of 25.97 and can be adjusted at full-scale with P1. The AD588's 5 V output and R6 provide an offset current for the RTD's initial resistance of 100 Ω at 0 °C with adjustment for this and A1's input offset voltage supplied by P2 and R5. For very remotely located RTDs in industrial environments, R_N and C_N can be used as a filter for noise. Typical values of 1 kΩ for R_N and 0.1 μF for C_N effectively filter out induced noise above 1.6 kHz. Larger values can be used for R_N without introducing errors because of the OP-297's very low bias currents and drift.

To calibrate this circuit, a precision set of resistors or a precision decade box in place of the RTD work equally well. First, 100.00 Ω is substituted for the RTD at 0°C, and P2 is adjusted so that the output of A1 reads 0 V. Next, the decade box is set to 138.5 Ω for the RTD at 100 °C. The constant-current excitation is adjusted with P1 so that A1's output reads 1.0000 V. The trim sequence might need repeating to fix the two end points.

By far the largest source of error in the circuit is the temperature dependence of Q1's output current. Since the temperature coefficient of a base-emitter junction is approximately -2.1 mV/°C, a 25°C change in the ambient temperature will cause an error of 0.7 °C. To reduce the circuit's sensitivity to changes in the current mirror's base-emitter junctions over temperature, temperature independent biasing techniques can be applied in the design of the current source.

Although the circuit is initially designed for 100 Ω Pt RTDs, other RTD values can be used with only one modification to the amplifier's circuit. For example, 1 kΩ is another commonly used RTD value in many applications, and using it only requires changing R4 from 1.02 kΩ to 23.7 kΩ. Since the RTD's value at 100 °C is 1.385kΩ, the full-scale RTD voltage at 1 mA is 1.385 V. This large output voltage might be a source of measurement error due to Early voltage modulation of Q1's collector-base junction. However, because of the MAT-03's low output conductance of 10 μA/V at 1mA, the 1.25 V change in Q1's collector-base voltage induces less than a 2 % change in Q1's collector current. This delta can be easily trimmed at full-scale with P1.

THERMISTOR SIGNAL CONDITIONING

THERMISTOR BASICS

Similar in function to the RTD, thermistors are low-cost temperature-sensitive resistors and are constructed of solid semiconductor materials which exhibit a either positive or negative temperature coefficient. Although positive temperature coefficient devices are available, the most commonly used thermistors are those that exhibit a negative temperature coefficient. Figure 2.71 shows the resistance-temperature characteristic of a commonly used NTC (Negative Temperature Coefficient) thermistor. The thermistor is highly non-linear and, of the three temperature sensors discussed, is the most temperature sensitive.

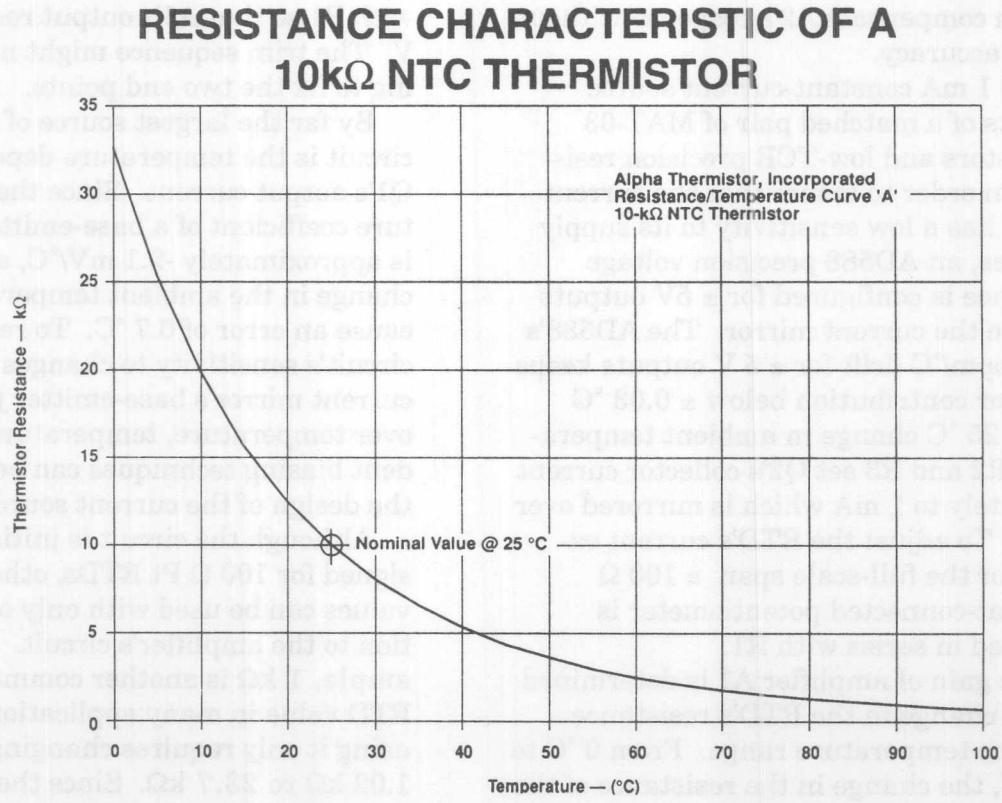


Figure 2.71

The thermistor's high sensitivity to temperature (typically, -44,000 ppm/°C at 25 °C), as shown in Figure 2.72, allows it to detect minute variations in temperature which would not be observed with an RTD or thermocouple. This high sensitivity to temperature is a distinct advantage over the RTD in that 4-wire Kelvin connections to the thermistor are not needed to compensate for lead wire errors. To illustrate this point, suppose a 10 kΩ NTC thermistor, with a typical 25 °C temperature coefficient of -44,000 ppm/°C, were substituted for the 100Ω Pt RTD in the example given earlier, then a total lead wire resistance of 21Ω would generate less than 0.05 °C error in the measurement. This is roughly a factor of 500 improvement in error over the equivalent RTD error.

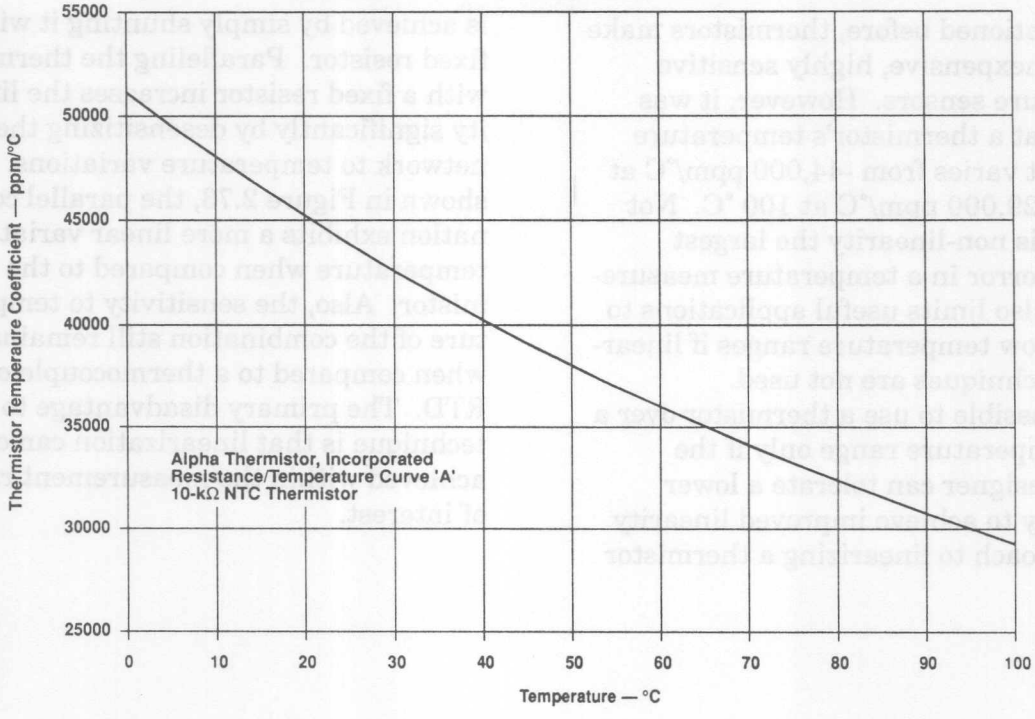


Figure 2.72

The thermistor's high sensitivity to temperature does not, however, come without a price. As was shown in Figure 2.72, the temperature coefficient of thermistors does not linearly decrease with increasing temperature as it does with RTDs; therefore, linearization is required for all but the narrowest of temperature ranges. Thermistor applications are limited to a few hundred degrees at best because they are more susceptible to permanent decalibration at high temperatures. Compared to thermocouples and RTDs, thermistors are quite fragile in construction and require careful mounting procedures to prevent crushing or bond separation. Although a thermistor's response time is quite short due to its small size, its small thermal mass makes it very sensitive to self-heating errors.

TYPICAL AMPLIFIER CONFIGURATION

As mentioned before, thermistors make for very inexpensive, highly sensitive temperature sensors. However, it was shown that a thermistor's temperature coefficient varies from -44,000 ppm/°C at 25 °C to -29,000 ppm/°C at 100 °C. Not only is this non-linearity the largest source of error in a temperature measurement, it also limits useful applications to very narrow temperature ranges if linearization techniques are not used.

It is possible to use a thermistor over a wider temperature range only if the system designer can tolerate a lower sensitivity to achieve improved linearity. One approach to linearizing a thermistor is achieved by simply shunting it with a fixed resistor. Paralleling the thermistor with a fixed resistor increases the linearity significantly by desensitizing the network to temperature variations. As shown in Figure 2.73, the parallel combination exhibits a more linear variation to temperature when compared to the thermistor. Also, the sensitivity to temperature of the combination still remains high when compared to a thermocouple or an RTD. The primary disadvantage to this technique is that linearization can only be achieved within the measurement range of interest.

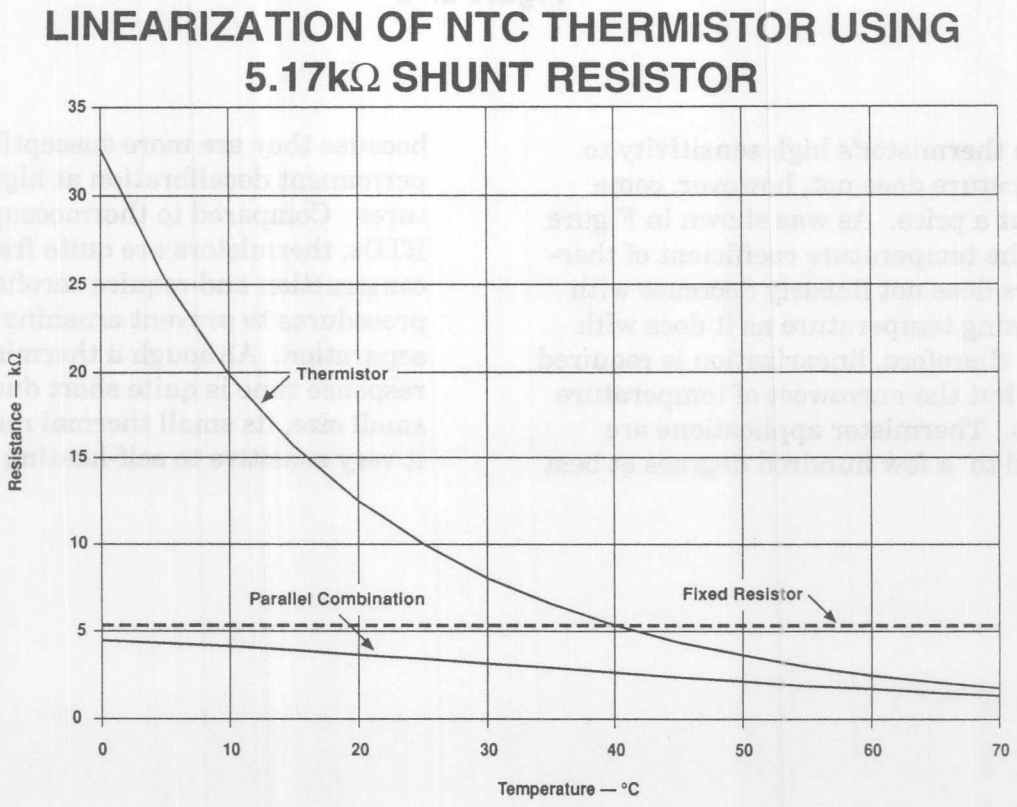


Figure 2.73

To implement this technique, a straight line is drawn through three equally spaced points along a thermistor's resistance-temperature characteristic. The three points are the midpoint and the two endpoints and must be within the measurement range. Thus, the value of the fixed resistor can be calculated from the following equation:

$$R = \frac{RT2(RT1 + RT3) - 2 \cdot RT1 \cdot RT3}{RT1 + RT3 - 2 \cdot RT2}$$

where RT1 = Thermistor resistance at T1, RT2 = Thermistor resistance at T2, RT3 = Thermistor resistance at T3.

For a typical 10 kΩ NTC thermistor, RT1 = 32,650 Ω at 0°C, RT2 = 6,532 Ω at 35 °C, and RT3 = 1,752 Ω at 70 °C. This results in a value of 5.17 kΩ for R. Of particular importance in linearizing a thermistor's response is the overall linearity deviation of the combined network. Accuracy requirements of the signal conditioning circuitry is dependent on the linearity deviation of the linearized network. For the example given above, Figure 2.74 illustrates the actual response of the combined network to the linear approximation and yields a departure from linearity of -2.3 °C/ + 2.0 °C.

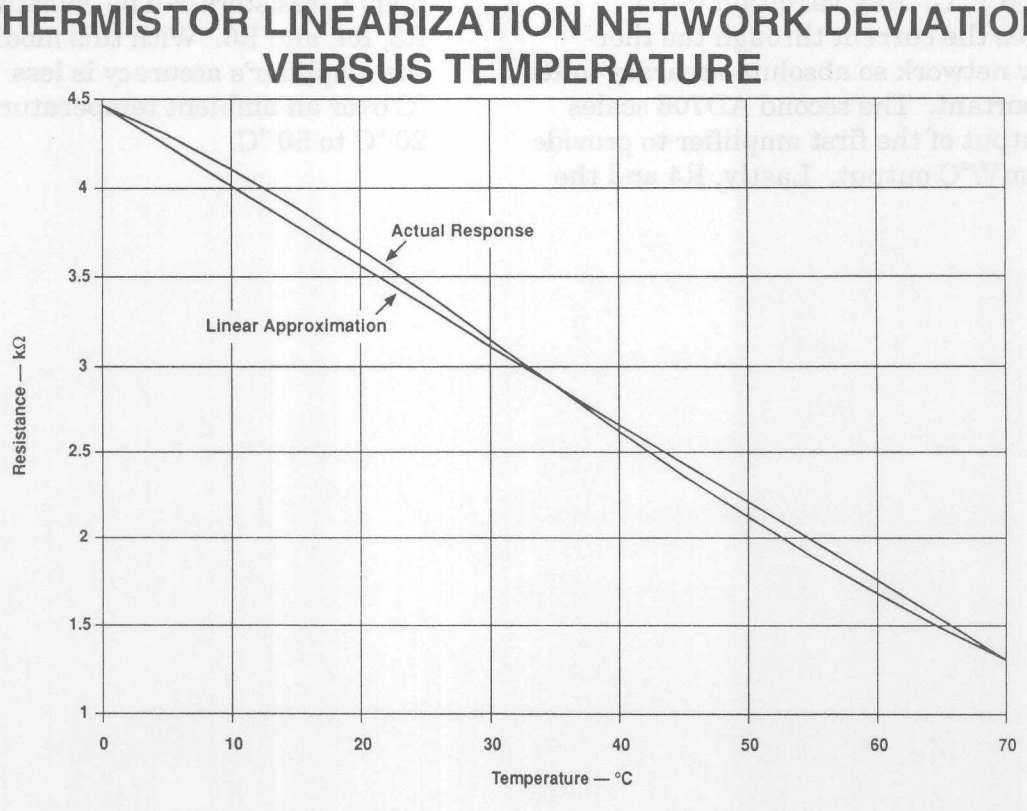


Figure 2.74

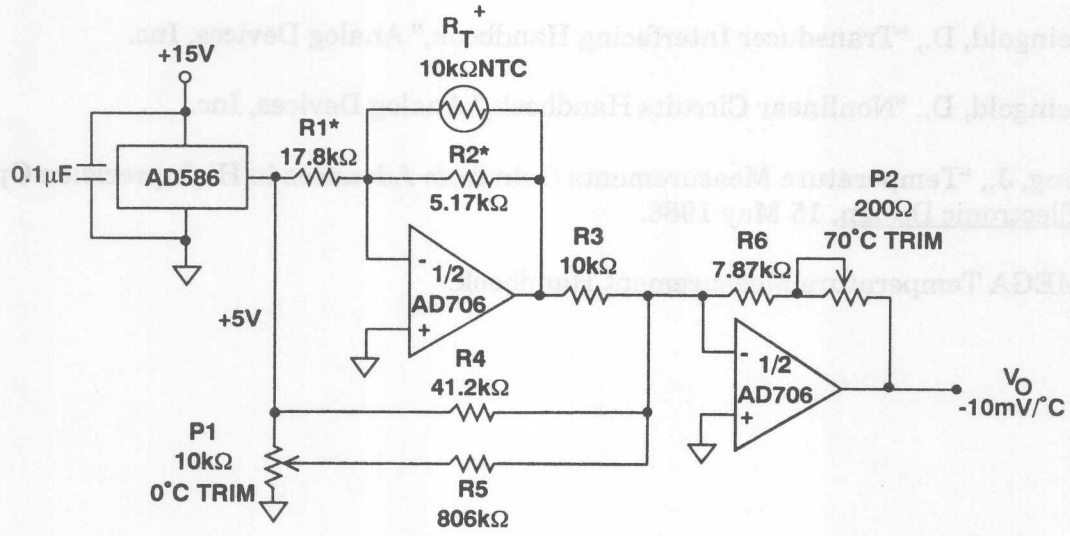
With this composite thermistor/resistor network, Figure 2.75 illustrates a linearized thermistor amplifier designed around the AD706 to measure temperatures over the range of 0 °C to 70 °C to an accuracy of ± 0.2 °C. The 10 kΩ thermistor and R2 form the feedback network of an inverting amplifier whose gain increases with temperature. High absolute accuracy in R2 is required to maintain the linearity deviation of the network under -2.3 °C/+ 2 °C. Much better linearity can be achieved with a narrower measurement temperature range. In many cases, the thermistor is placed some distance from the signal conditioning circuit. Under this condition, a 0.1 μF capacitor placed across R2 will help to suppress noise pickup.

In the circuit, R1 and the AD586 provide a constant current of 281 μA to the linearized network such that the thermistor's self-heating error is kept below 0.1 °C. Any variation in R1 changes the current through the thermistor network so absolute accuracy in R1 is important. The second AD706 scales the output of the first amplifier to provide a -10 mV/°C output. Lastly, R4 and the reference generate an offset current such that the output of the second amplifier is 0 V at 0 °C.

A calibration procedure is required for this circuit to trim resistor tolerance and the AD706s' initial offset voltages. To start, a precision decade box can be used in place of the thermistor. For 0°C trim, the decade box is set to 32.650 kΩ, and P1 is adjusted until the circuit's output reads 0 V. To trim the circuit at the full-scale temperature of 70 °C, the decade box in then set to 1.752 kΩ and P2 is adjusted until the circuit reads -0.70 V.

Since the AD706 exhibits very low input bias currents, measurement errors attributed to them can be neglected in this application. It's high open-loop gain and low input offset voltage drift keep their error contribution below 0.003 °C over a 25 °C change in ambient temperature. To help reduce component costs, 50 ppm/°C resistors can be substituted for R3, R4, and R6. With this modification, the amplifier's accuracy is less than ± 0.3 °C over an ambient temperature range of 20 °C to 50 °C.

LINEARIZED THERMISTOR AMPLIFIER



NOTES: + = ALPHA THERMISTOR 13A1002-C3
* = 0.1% IMPERIAL ASTRONICS M015
ALL RESISTORS ARE 1%, 25 ppm/°C EXCEPT
R5 = 1%, 100 ppm/°C

Figure 2.75

REFERENCES

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2. Sheingold, D., "Transducer Interfacing Handbook," Analog Devices, Inc.

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5. OMEGA Temperature Measurement Handbook.

SECTION III
HIGH IMPEDANCE, LOW CURRENT APPLICATIONS

- Precision Photodiode Preamplifier Design Analysis: Photodiode Characteristics, DC Analysis, AC Analysis, Noise Analysis, Circuit Tradeoffs, "T" Network Analysis

- High Speed Photodiode Preamplifiers: Characteristics of High Speed Photodiodes, Determining Circuit Frequency Response, Selecting the Proper Op Amp, Noise Analysis, Achieving More Bandwidth by Using Two Stages, Using a Composite Amplifier to Increase the Gain Bandwidth Product, High Speed Fiber Optic Receivers

- Other High Impedance Transducer Applications: A pH Probe Buffer Amplifier, High Impedance Charge Output Transducers, Accelerometer Amplifiers, Hydrophone Amplifiers, Op Amp Performance: JFET Versus Bipolar, Using Decompensated Op Amps as I/V Converters, A High Performance Audio I/V Converter

SECTION III

HIGH IMPEDANCE, LOW CURRENT APPLICATIONS

WALT KESTER, SCOTT WURCER, CHUCK KITCHIN

PRECISION PHOTODIODE PREAMPLIFIER CIRCUIT ANALYSIS

WALT KESTER

In this portion of the seminar we will conduct a detailed design analysis of a precision photodiode preamplifier circuit. This particular application was chosen because it illustrates most of the key points which must be considered when dealing with precision low-noise op amps. The circuit designed is extremely useful in converting any precision low-level current into a voltage.

PHOTODIODE APPLICATIONS AND CHARACTERISTICS

Photodiodes generate a small current which is proportional to the level of illumination. They have many applications ranging from precision light meters to high-speed fiber optic receivers.

The equivalent circuit for a photodiode is shown in Figure 3.2. One of the standard methods for specifying the sensitivity of a photodiode is to state its short circuit photocurrent (I_{SC}) at a given light level from a well defined light source. The most commonly used source is an incandescent tungsten lamp running at a color temperature of 2850K. At 100 fc (foot-candles) illumination (approximately the light level on an overcast day), the short circuit current is usually in the picoamps to hundreds of microamps range for small area (less than $1mm^2$) diodes.

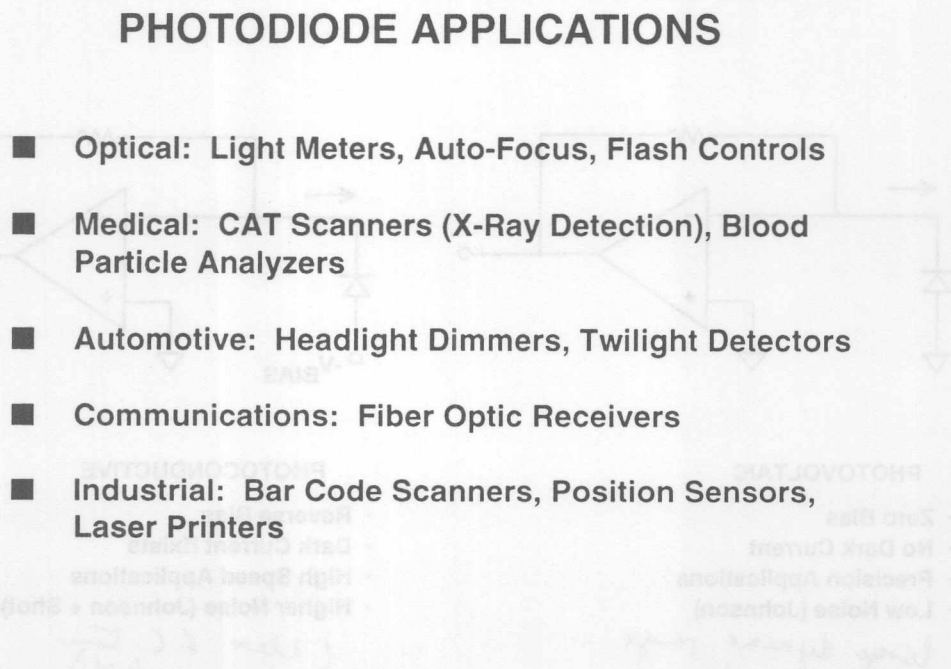


Figure 3.1

PHOTODIODE EQUIVALENT CIRCUIT

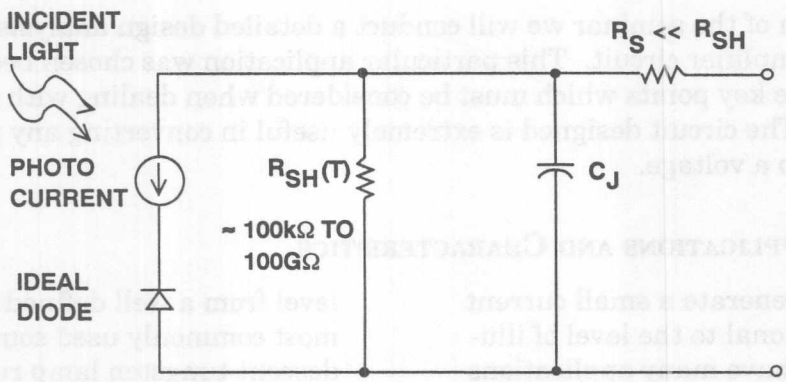
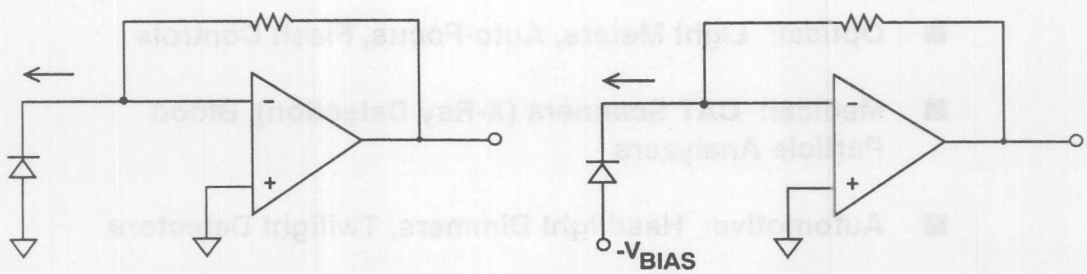


Figure 3.2

PHOTODIODE MODES OF OPERATION



PHOTOVOLTAIC

- Zero Bias
- No Dark Current
- Precision Applications
- Low Noise (Johnson)

large dynamic range (no current when no light)

PHOTOCONDUCTIVE

- Reverse Bias
- Dark Current Exists
- High Speed Applications
- Higher Noise (Johnson + Shot)

(lower RC time constant)

Figure 3.3

The short circuit current is very linear over 6 to 9 decades of light intensity, and is therefore often used as a measure of absolute light levels. The open circuit forward voltage drop across the photodiode varies logarithmically with light level, but, because of its large temperature coefficient, the diode voltage is seldom used as an accurate measure of light intensity.

The shunt resistance is usually in the order of 1000MΩ at room temperature, and decreases by a factor of 2 for every 10°C rise in temperature. Diode capacitance is a function of junction area and the diode bias voltage. A value of 50pF at zero bias is typical for small area diodes.

Photodiodes may either be operated with zero bias (*photovoltaic* mode) or reverse bias (*photoconductive* mode) as shown in Figure 3.3. The most precise linear operation is obtained in the photovoltaic mode, while higher switching speeds are realizable when the diode is operated in the photoconductive mode. Under reverse bias conditions, a small amount of current called *dark current* will flow even when there is no illumination. There is no dark current in the photovoltaic mode. In the photovoltaic mode, the diode noise is basically the thermal noise generated by the shunt resistance. In the photoconductive mode, shot noise due to conduction is an additional source of noise. Photodiodes are usually optimized during the design process for use in either the photovoltaic mode or the photoconductive mode, but not both.

Figure 3.4 shows the photosensitivity for a small photodiode (Silicon Detector Part Number SD-020-12-001), and specifications for the diode are summarized in Figure 3.5.

SHORT CIRCUIT CURRENT VERSUS LIGHT INTENSITY FOR PHOTODIODE (PHOTOVOLTAIC MODE)

ENVIRONMENT	ILLUMINATION (fc)	SHORT CIRCUIT CURRENT
Direct Sunlight	1000	30μA
Overcast Day	100	3μA
Twilight	1	0.03μA
Full Moonlit Night	0.1	3000pA
Clear Night / No Moon	0.001	30pA

Figure 3.4

PHOTODIODE SPECIFICATIONS
Silicon Detector Part Number SD-020-12-12-001

- **Area: 0.2mm^2**
- **Capacitance: 50pF**
- **Shunt Resistance at 25°C: 1000 megohms**
- **Maximum Linear Output Current: 40mA**
- **Response Time: 12ns**
- **Photosensitivity: 0.03μA / fc**

Figure 3.5

PHOTODIODE PREAMP CIRCUIT CONSIDERATIONS

A convenient way to convert the photodiode current into a usable voltage is to use an op amp as a current-to-voltage converter as shown in Figure 3.6. The diode bias is maintained at zero volts by the virtual ground of the op amp, and the short circuit current is converted into a voltage. If we wish to operate at maximum sensitivity, we must be able to detect a diode current of 30pA. This implies that the feedback resistor must be very large. For example, 1000MΩ will yield a corresponding voltage of 30mV for this amount of current. Larger resistor values are impractical, so we will use 1000MΩ for the most sensitive range. This will give an output voltage range of 10mV for 10pA of diode current and 10V for 10nA of diode current. This yields a range of 60dB. For higher values of light intensity, the gain of the circuit must be reduced by using a smaller feedback resistor. For this range of maximum sensitivity, we should be able to easily distinguish between the light intensity on a clear moonless night (0.001fc) and that of a full moon (0.1fc)!

Notice that we have chosen to get as much gain as possible from one stage, rather than cascading two stages. This is in order to maximize the signal-to-noise ratio (SNR). If we halve the feedback resistor value, the signal level decreases by a factor of 2, while the noise due to the feedback resistor (Noise Voltage = $\sqrt{4kTR \cdot \text{Bandwidth}}$) decreases by only $\sqrt{2}$. This reduces the SNR by 3dB, assuming the closed loop bandwidth remains constant. Later in the analysis, we will see that the resistors are one of the largest contributors to the overall output noise.

SIMPLIFIED OP-AMP CURRENT-TO-VOLTAGE CONVERTER

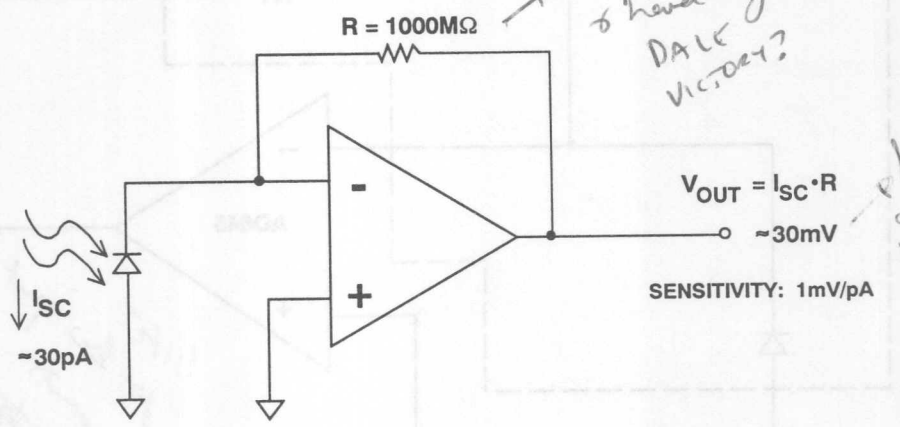


Figure 3.6

PRECAUTIONS FOR PICOAMPERE CIRCUITS

Since the diode current is measured in terms of picoamperes, extreme attention must be given to potential leakage paths in the actual circuit. Two parallel conductor stripes on a high-quality well-cleaned epoxy-glass PC board 0.05 inches apart running parallel for 1 inch have a leakage resistance of approximately 10^{11} ohms at +125°C (Reference 4, p.293). If there is 15 volts between these runs, there will be a current flow of 150pA.

The critical leakage paths for the photodiode circuit are enclosed by the dotted lines in Figure 3.7. The feedback resistor should be thin film on ceramic or glass with glass insulation. The compensation capacitor across the feedback resistor should have a polypropylene or polystyrene dielectric. All connections to the summing junction should be kept short. If a cable is used to connect the photodiode to the preamp, it should be kept as short as possible and have Teflon insulation.

Guard rings (on both sides of the PC board) should be used around the inverting input pin of the op amp as shown in Figure 3.8. The case ground of the op amp (usually Pin 8) should also be connected to the grounded guard ring. Maintaining the guard ring potential the same as the inverting input potential minimizes any leakage current due to PC board resistance.

Ideally, all connections to the summing input of the op amp should be made to a virgin Teflon standoff insulator ("Virgin" Teflon is a solid piece of new Teflon material which has been machined to shape and has not been welded together from powder or grains). If mechanical and manufacturing considerations allow, the inverting input pin of the op amp should be soldered directly to the Teflon standoff

LEAKAGE CURRENT PATHS

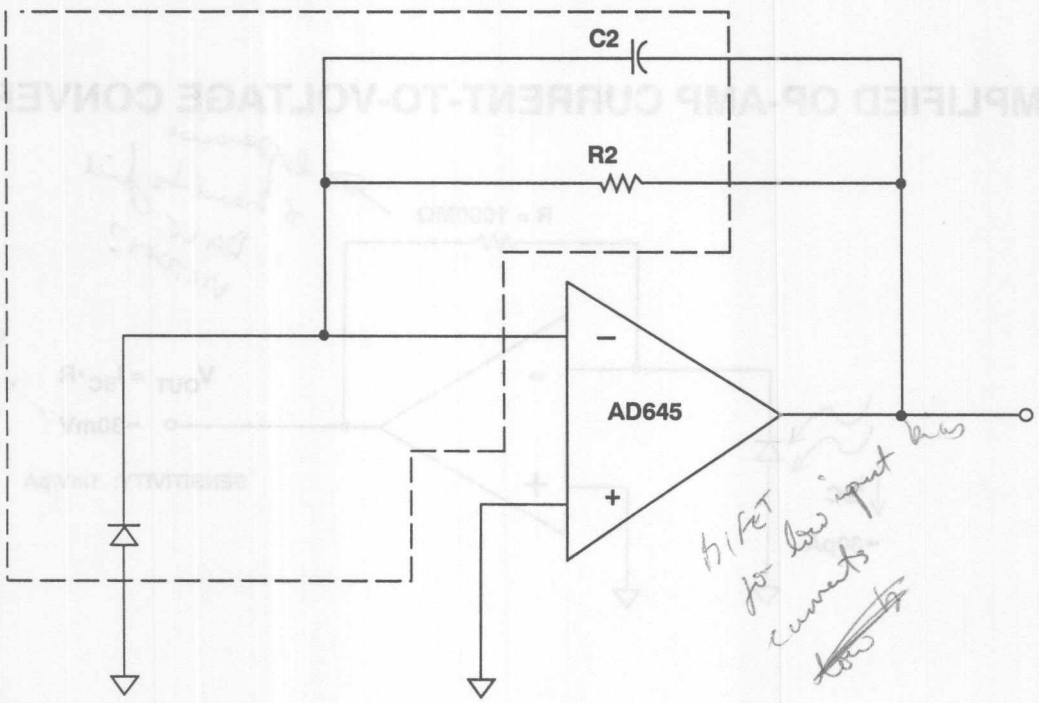
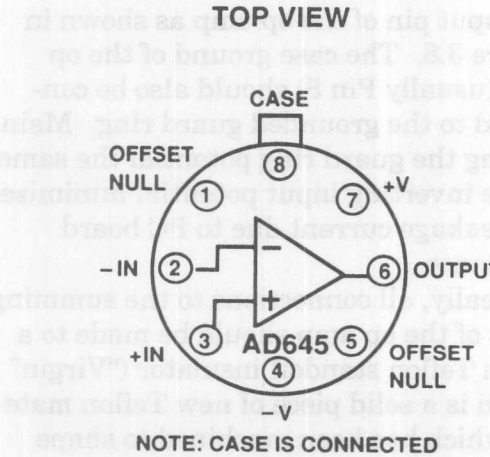


Figure 3.7

PC BOARD LAYOUT FOR GUARDING TO-99 PACKAGE



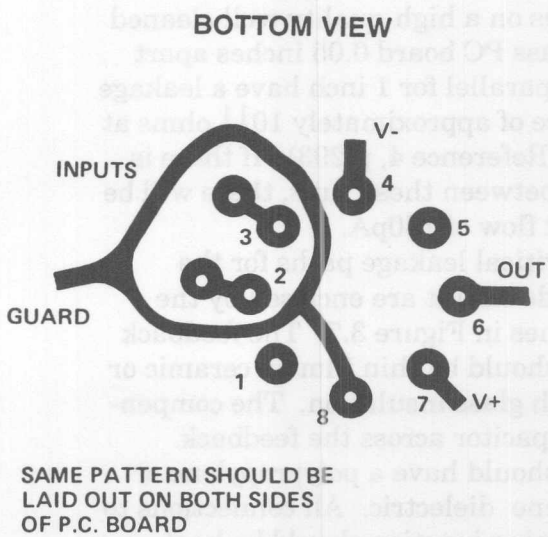


Figure 3.8

(see Figure 3.9) rather than going through a hole in the PC board. The PC board itself must be cleaned carefully and then sealed against humidity and dirt using a high quality conformal coating material.

In addition to minimizing leakage currents, the entire circuit should be well shielded with a grounded metal shield to prevent stray signal pickup. Details regarding proper grounding, shielding, and noise reduction techniques are given in References 8 and 9 at the end of this section.

A VIRGIN TEFLON STANDOFF INSULATOR HAS MUCH LOWER LEAKAGE THAN A PCB TRACK

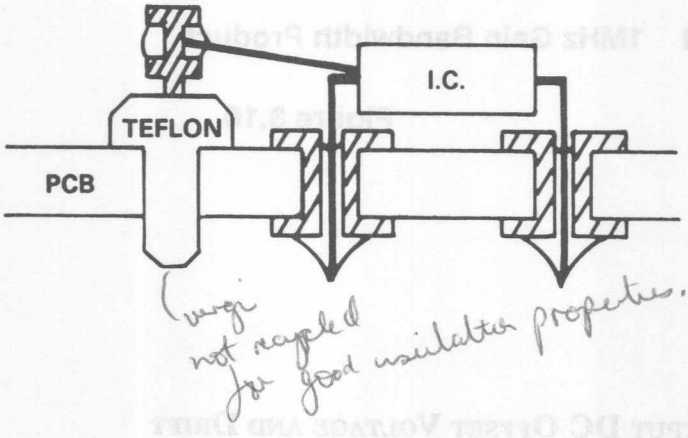


Figure 3.9

AMPLIFIER SELECTION AND DC CIRCUIT ANALYSIS

If we wish to accurately measure photodiode currents in the tens of picoamps range, the bias current of the op amp should be no more than a few picoamps. This narrows the choice considerably. The industry-standard AD OP-07 is an ultra-low offset voltage (10μV) bipolar op amp , but its bias current is 4nA (4000pA!). Even super-beta bipolar op amps with bias current compensation (such as the AD OP-97) have bias currents of 100pA at room temperature. For this reason, an FET-input electometer-grade op amp such as the AD645 is required for our photodiode preamp. The AD645 utilizes a BiFET process in conjunction with laser wafer trimming to achieve the specifications shown in Figure 3.10.

AD645 BiFET OP AMP KEY SPECIFICATIONS

- **Offset Voltage: 250μV Maximum at 25°C**
- **Offset Voltage Drift: 1μV/°C Maximum (C Grade)**
- **Input Bias Current: 1.5pA at 25°C**
- **2.5μV p-p Noise, 0.1Hz to 10Hz**
- **20nV/$\sqrt{Hz}$ Noise at 100Hz**
- **11fA p-p Current Noise, 0.1Hz to 10Hz**
- **0.6fA/$\sqrt{Hz}$ Current Noise at 20kHz**
- **90mW Power Dissipation at ± 15V**
- **1MHz Gain Bandwidth Product**

Figure 3.10

ANALYSIS OF OUTPUT DC OFFSET VOLTAGE AND DRIFT

The general offset voltage and bias current model for an op amp is shown in Figure 3.11. This model can be modified as needed to fit any particular application circuit which uses an op amp either in the inverting or the non-inverting mode. In our example, R_p=0, R_2=1000MΩ, and R_1=photodiode shunt resistance. Unfortunately, the diode shunt resistance is a function of temperature (halves every 10°C rise) which complicates our analysis somewhat.

At this point, we need to define the *noise gain* of our circuit. The noise gain is the gain the amplifier circuit presents to the input offset voltage and the input noise voltage. For dc, its value is $1 + R_2/R_1$. Noise gain must be distinguished from *signal gain*! In the inverting mode, the signal gain of an op amp for dc is $-R_2/R_1$. In the non-inverting mode, the signal gain is $1 + R_2/R_1$. In both cases, the noise gain is $1 + R_2/R_1$.

In our example, since R_1 is a function of temperature, the noise gain will also be a function of temperature. In fact, at -25°C the noise gain is 1.03, while at +85°C it increases to 64.7 (corresponding to R_1 going from 31,920MΩ to 15.7MΩ).

All the individual dc error sources and their sum are shown in Figure 3.12. This curve assumes a room temperature offset voltage of 0.250mV, a temperature coefficient of 1μV/°C, and a room temperature

bias current of 1.5pA. The majority of the output voltage drift comes from the effects of the op amp bias current which, even though it is very low at room temperature (1.5pA), nevertheless, doubles for every 10°C rise in temperature (at +85°C, the bias current is 96pA). For this reason, every attempt should be made to minimize the self-heating of the op amp. An adequate heatsink should be used to minimize the junction temperature rise above ambient, and output loading should also be minimal to prevent increased chip power dissipation due to load current. In the next sections we will explore several methods to improve the dc drift over temperature.

OFFSET VOLTAGE AND BIAS CURRENT MODEL

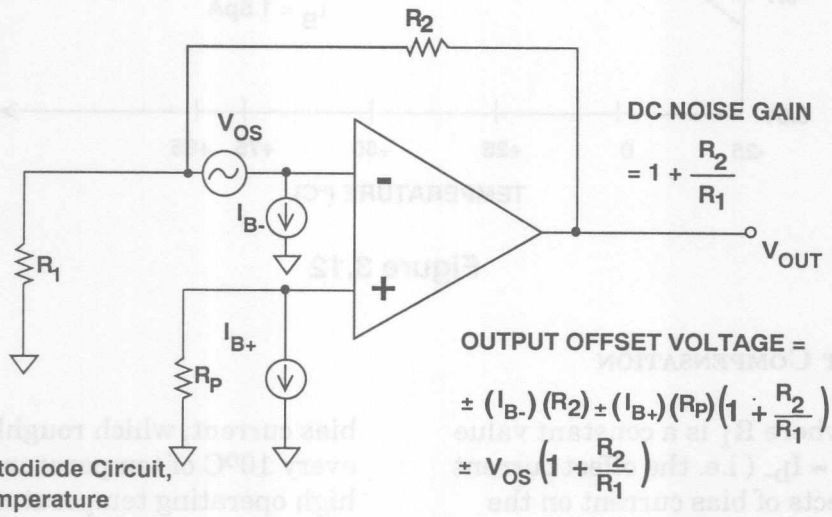


Figure 3.11

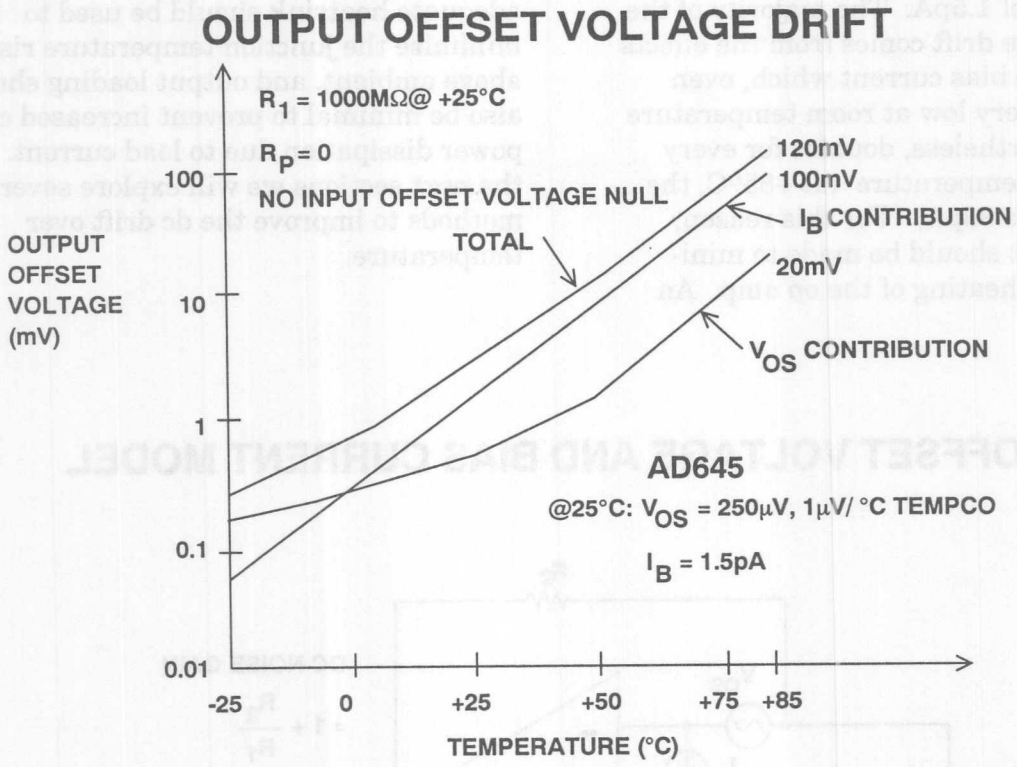


Figure 3.12

BIAS CURRENT COMPENSATION

In circuits where R_1 is a constant value and where $I_{b+} \approx I_{b-}$ (i.e. the offset current is low), the effects of bias current on the output voltage offset can be cancelled by inserting a resistor in the non-inverting input whose value is equal to the parallel combination of R_1 and R_2. This is shown in Figure 3.13. Normal practice is to bypass this resistor with a capacitor so that the resistor noise is not multiplied by the noise gain and combined with the output noise. This scheme works very well for bipolar op amps where the input bias currents tend to be well matched. FET-input devices have the lowest bias currents, although on a percentage basis, their offset currents are not as low as those of bipolar devices. Their input and offset currents are, however, low enough in absolute level that in many circuits they do not need bias-current compensation. A disadvantage of FET-input devices is the temperature dependence of bias current, which roughly doubles for every 10°C of temperature rise. If very high operating temperatures are required, this characteristic tends to defeat their low-input-current superiority somewhat, although the degree to which this is true depends, of course, on the device and at how high a temperature one must operate it.

If we apply this bias current compensation technique to the photodiode circuit using the room temperature value of R_1 (1000MΩ) to calculate R_p, we find that R_p = 500MΩ (See Figure 3.14). If, however, we run through the calculations at +85°C, we find that R_1 = 15.7MΩ, Noise Gain = 64.7, I_b = 96pA, and the output offset voltage is 3V !! Also, the 96pA of bias current flowing through Rp develops a voltage of 48mV which appears across the photodiode. The effect of this voltage is to cause non-linearity in the diode response to light intensity.

INPUT BIAS CURRENT CANCELLATION

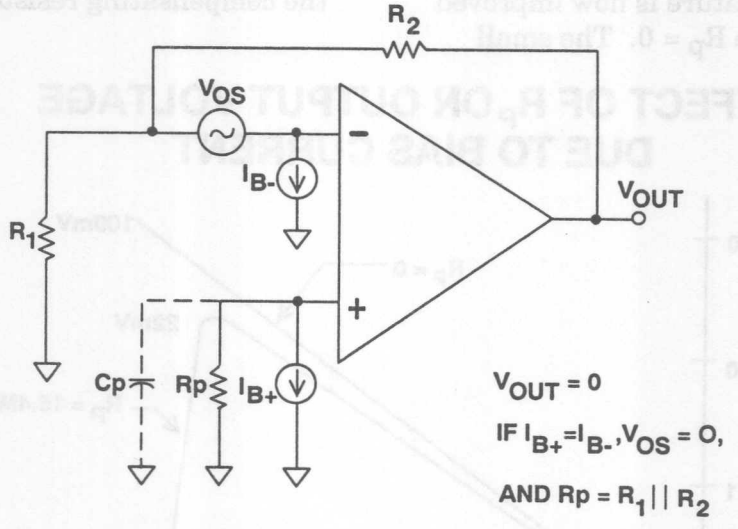


Figure 3.13

A BIAS CURRENT CANCELLATION DISASTER

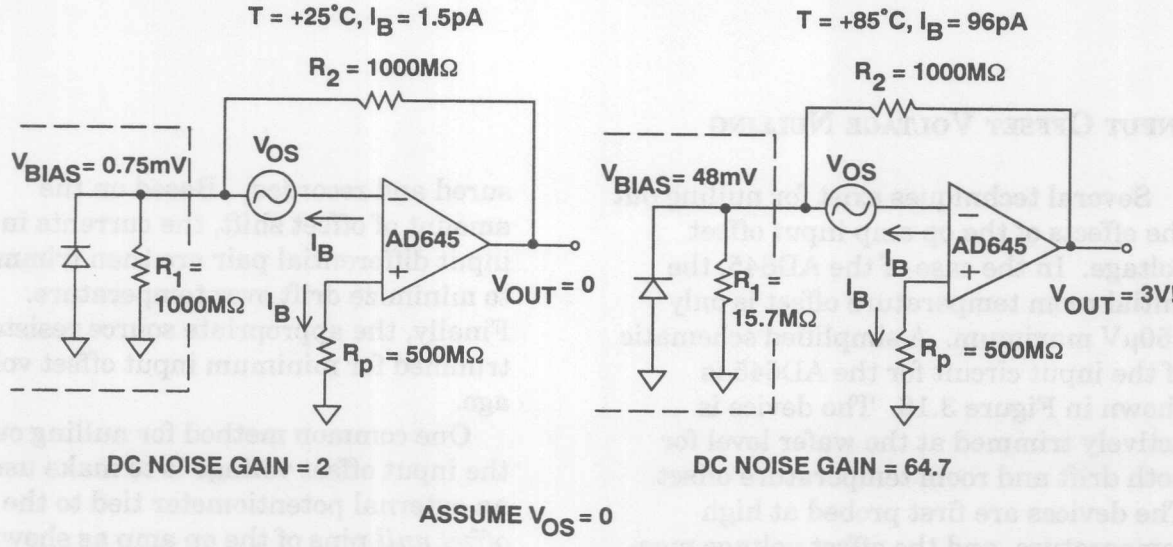


Figure 3.14

Rather than select Rp based on the room temperature value of R_1, it should be selected based on R_1's value at +85°C which is 15.7MΩ. For this value of R_1, R_p should be 15.4MΩ. Output voltage versus drift versus temperature is now improved over the case where $R_p = 0$. The small amount of bias voltage developed across the photodiode due to I_b flowing in R_p (1.5mV) is not sufficient to cause linearity problems. Figure 3.15 shows output voltage drift due to I_b with and without the compensating resistor.

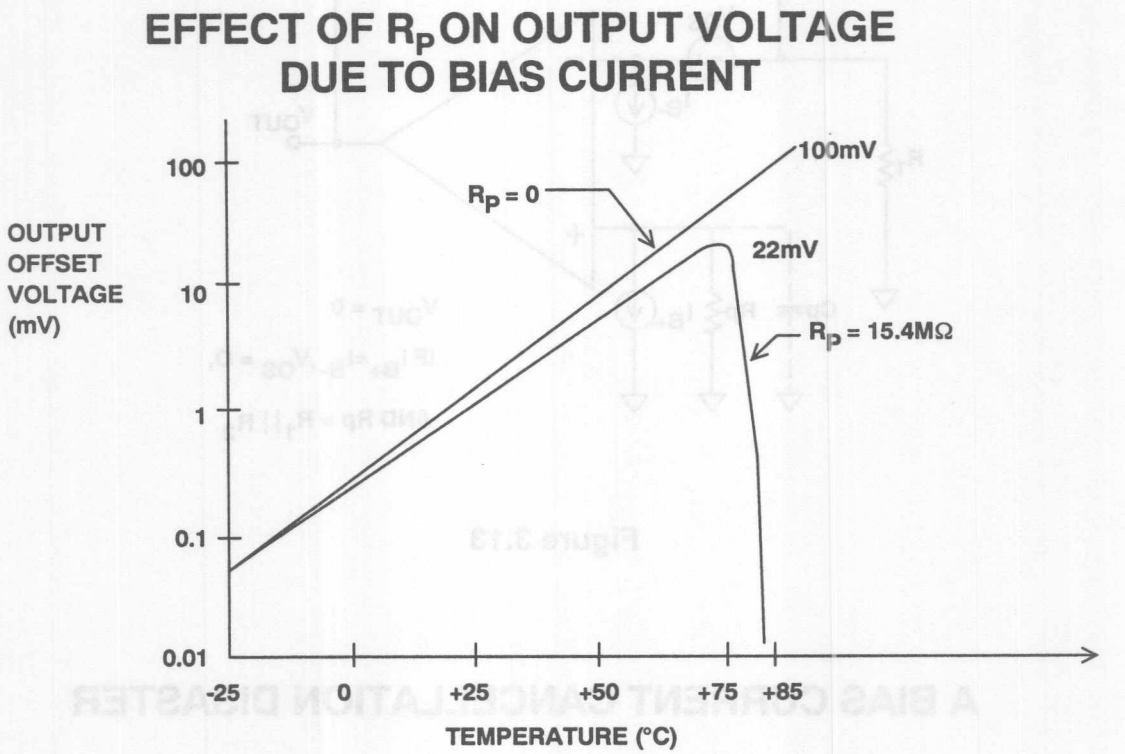


Figure 3.15

INPUT OFFSET VOLTAGE NULLING

Several techniques exist for nulling out the effects of the op amp input offset voltage. In the case of the AD645, the initial room temperature offset is only 250μV maximum. A simplified schematic of the input circuit for the AD645 is shown in Figure 3.16. The device is actively trimmed at the wafer level for both drift and room temperature offset. The devices are first probed at high temperature, and the offset voltage measured and recorded. The devices are probed a second time at room temperature, and the offset voltage is again measured and recorded. Based on the amount of offset shift, the currents in the input differential pair are then trimmed to minimize drift over temperature. Finally, the appropriate source resistor is trimmed for minimum input offset voltage.

One common method for nulling out the input offset voltage is to make use of an external potentiometer tied to the *offset null* pins of the op amp as shown in Figure 3.17. Unfortunately, this method of nulling will actually increase the temperature coefficient of offset voltage

BiFET OP AMP SIMPLIFIED INPUT CIRCUIT

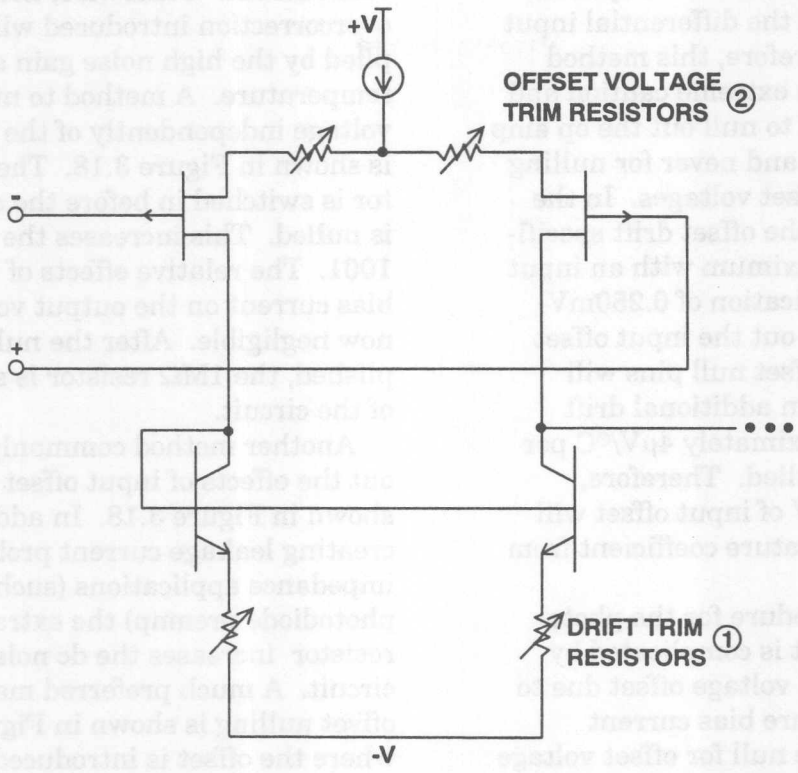
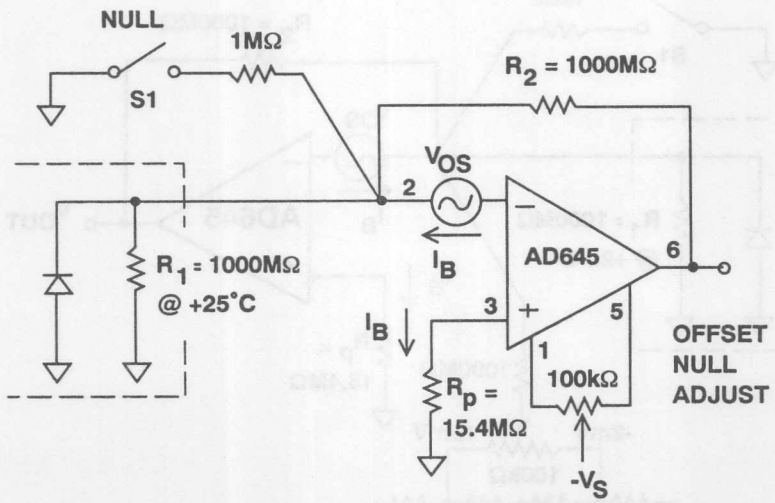


Figure 3.16

USING OFFSET VOLTAGE NULL PINS



- S1 ALLOWS V_{OS} NULL INDEPENDENT OF I_B
- V_{OS} TEMPCO INCREASES 4μV/°C/mV NULL

Figure 3.17

because the nulling is achieved by creating an imbalance in the differential input FET currents. Therefore, this method should be used with extreme caution and should only be used to null out the op amp input offset voltage and never for nulling out large system offset voltages. In the case of the AD645, the offset drift specification is 1μV/°C maximum with an input offset voltage specification of 0.250mV maximum. Nulling out the input offset voltage using the offset null pins will actually introduce an additional drift component of approximately 4μV/°C per millivolt of offset nulled. Therefore, nulling out 0.250mV of input offset will increase the temperature coefficient from 1μV/°C to 2μV/°C!!

The nulling procedure for the photodiode preamp circuit is complicated by effects of the output voltage offset due to the room temperature bias current (typically 1pA). The null for offset voltage should not correct for the nominal offset (2mV at the output) due to the 1pA input bias current. Otherwise, the amount of overcorrection introduced will be multiplied by the high noise gain at the high temperature. A method to null the offset voltage independently of the bias current is shown in Figure 3.18. The 1MΩ resistor is switched in before the offset voltage is nulled. This increases the noise gain to 1001. The relative effects of the input bias current on the output voltage are now negligible. After the null is accomplished, the 1MΩ resistor is switched out of the circuit.

Another method commonly used to null out the effects of input offset voltage is shown in Figure 3.18. In addition to creating leakage current problems in high impedance applications (such as the photodiode preamp) the extra summing resistor increases the dc noise gain of the circuit. A much preferred method for offset nulling is shown in Figure 3.19, where the offset is introduced across a small resistor which is inserted in the non-inverting input.

OFFSET VOLTAGE NULLING USING INVERTING INPUT

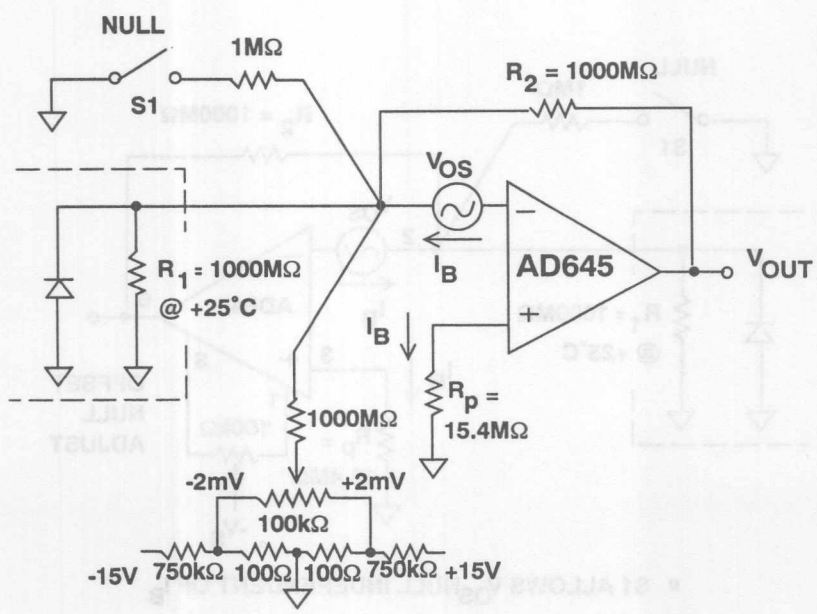


Figure 3.18

OFFSET VOLTAGE NULLING USING NON-INVERTING INPUT

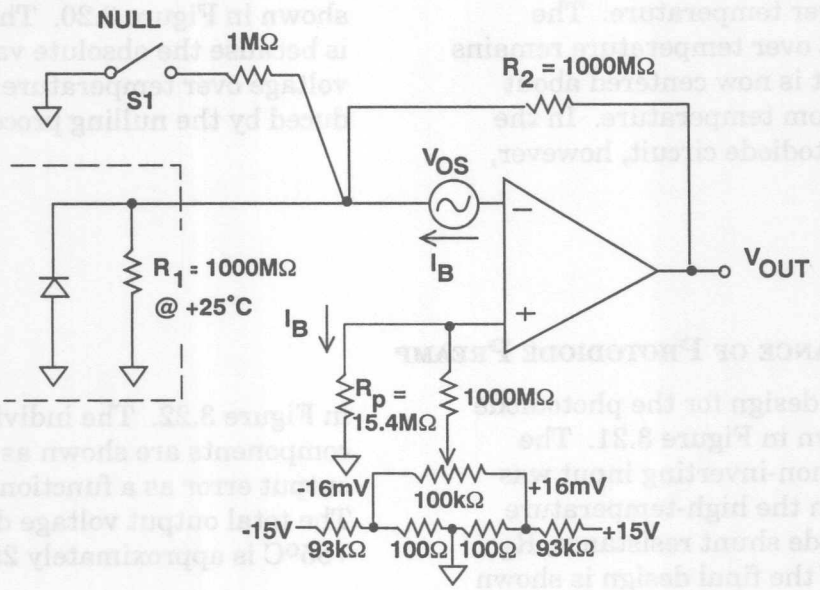


Figure 3.19

OUTPUT OFFSET VOLTAGE DUE TO V_{OS}

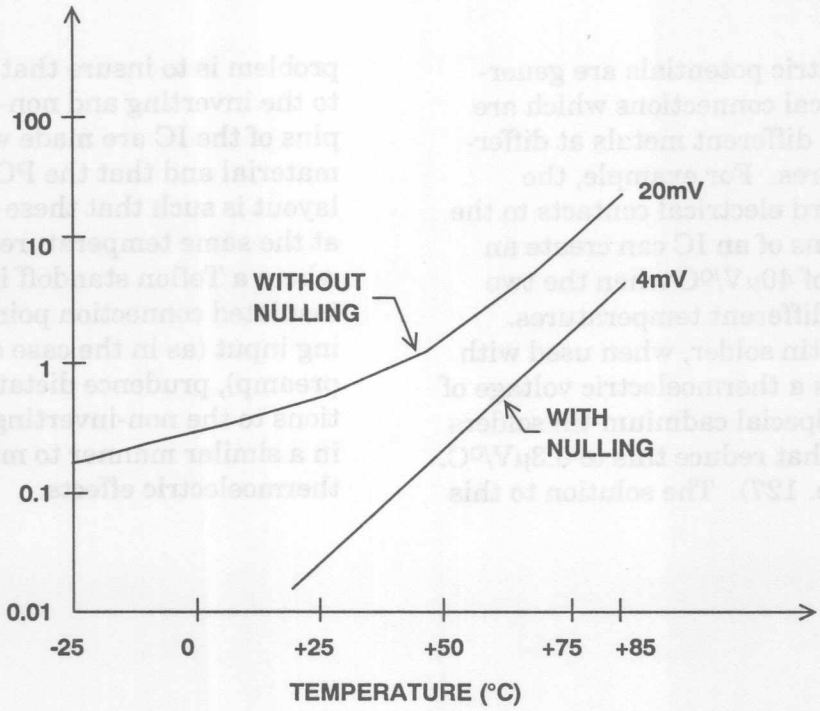


Figure 3.20

In applications where all the external feedback resistors are fixed, offset nulling (using the non-inverting input) will have no effect on the overall amount of output voltage drift over temperature. The amount of drift over temperature remains the same, but it is now centered about zero volts at room temperature. In the case of the photodiode circuit, however, where the diode shunt resistance (and hence the noise gain) is a function of temperature, offset nulling actually improves the drift characteristic as shown in Figure 3.20. This improvement is because the absolute value of the offset voltage over temperature has been reduced by the nulling process.

DC PERFORMANCE OF PHOTODIODE PREAMP

The final dc design for the photodiode preamp is shown in Figure 3.21. The resistor in the non-inverting input was chosen based on the high-temperature value of the diode shunt resistance, R_1. Performance of the final design is shown in Figure 3.22. The individual error components are shown as well as the total output error as a function of temperature. The total output voltage drift from -25 to +85°C is approximately 25mV.

THERMOELECTRIC VOLTAGES AS SOURCES OF INPUT OFFSET VOLTAGE

Thermoelectric potentials are generated by electrical connections which are made between different metals at different temperatures. For example, the copper PC board electrical contacts to the kovar input pins of an IC can create an offset voltage of 40μV/°C when the two metals are at different temperatures. Common lead-tin solder, when used with copper, creates a thermoelectric voltage of 1 to 3μV/°C. Special cadmium-tin solders are available that reduce this to 0.3μV/°C. (Reference 4, p. 127). The solution to this problem is to insure that the connections to the inverting and non-inverting input pins of the IC are made with the same material and that the PC board thermal layout is such that these two pins remain at the same temperature. In the case where a Teflon standoff is used as an insulated connection point for the inverting input (as in the case of the photodiode preamp), prudence dictates that connections to the non-inverting inputs be made in a similar manner to minimize possible thermoelectric effects.

FINAL DC DESIGN FOR PHOTODIODE PREAMP

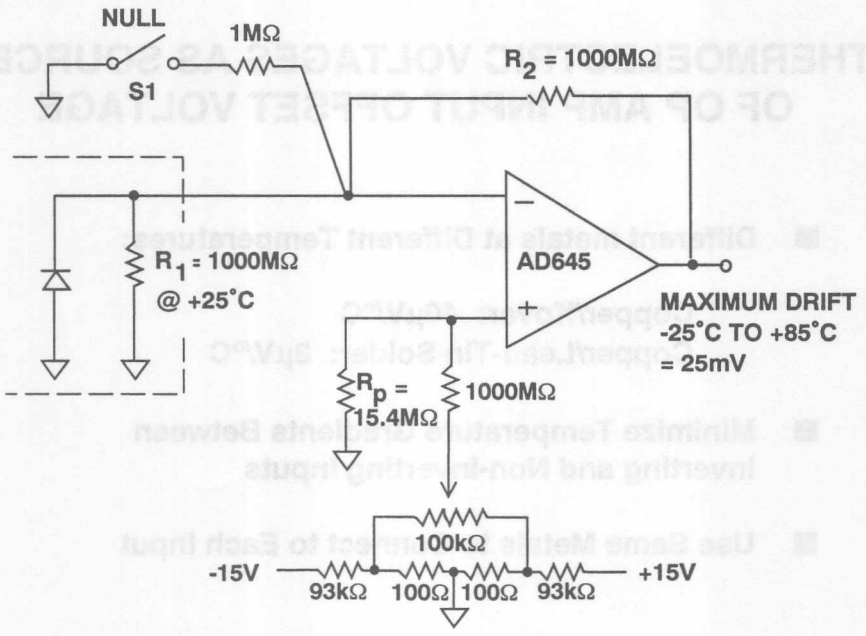


Figure 3.21

OUTPUT VOLTAGE OFFSET FOR FINAL DESIGN

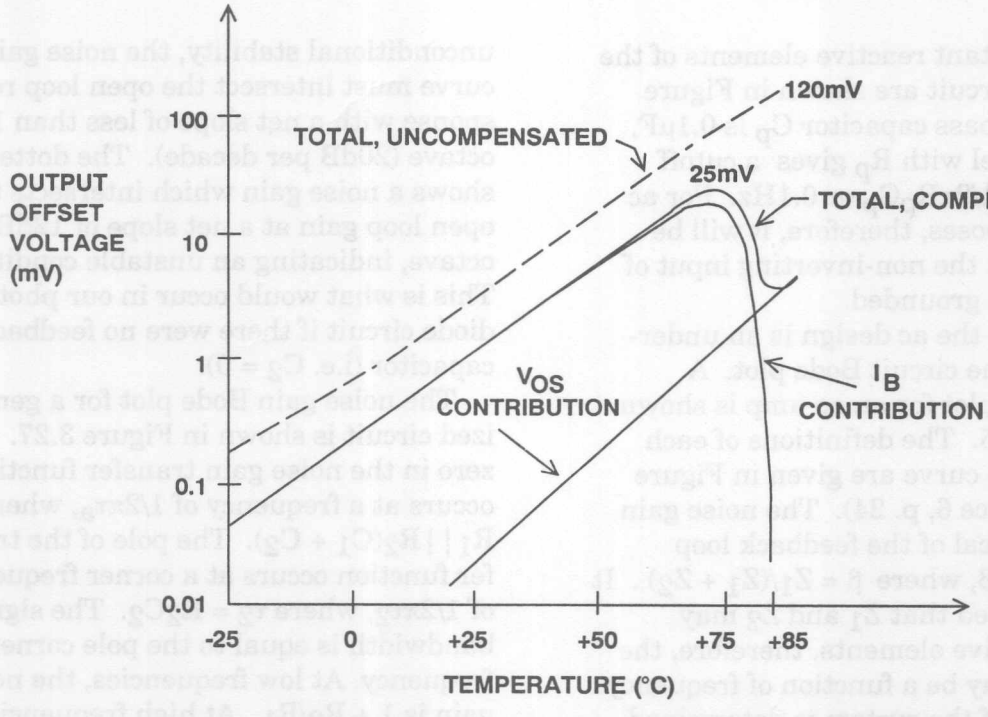


Figure 3.22

THERMOELECTRIC VOLTAGES AS SOURCES OF OP AMP INPUT OFFSET VOLTAGE

- **Different metals at Different Temperatures:**

  Copper/Kovar: 40μV/°C
  Copper/Lead-Tin Solder: 3μV/°C

- **Minimize Temperature Gradients Between Inverting and Non-Inverting Inputs**

- **Use Same Metals to Connect to Each Input**

Figure 3.23

AC DESIGN, BANDWIDTH, AND STABILITY

The important reactive elements of the photodiode circuit are shown in Figure 3.24. The bypass capacitor C_p is 0.1μF, and in parallel with R_p gives a cutoff frequency of $1/2\pi R_p C_p$ or 0.1Hz. For ac analysis purposes, therefore, it will be assumed that the non-inverting input of the op amp is grounded.

The key to the ac design is an understanding of the circuit Bode plot. A typical Bode plot for an op amp is shown in Figure 3.25. The definitions of each portion of the curve are given in Figure 3.26 (Reference 6, p. 24). The noise gain is the reciprocal of the feedback loop attenuation, β, where $\beta = Z_1/(Z_1 + Z_2)$. It should be noted that Z_1 and Z_2 may contain reactive elements, therefore, the noise gain may be a function of frequency.

Stability of the system is determined by the net slope of the noise gain and the open loop gain where they intersect. For unconditional stability, the noise gain curve must intersect the open loop response with a net slope of less than 12dB/octave (20dB per decade). The dotted line shows a noise gain which intersects the open loop gain at a net slope of 12dB/octave, indicating an unstable condition. This is what would occur in our photodiode circuit if there were no feedback capacitor (i.e. $C_2 = 0$).

The noise gain Bode plot for a generalized circuit is shown in Figure 3.27. A zero in the noise gain transfer function occurs at a frequency of $1/2\pi\tau_a$, where $\tau_a = R_1 || R_2(C_1 + C_2)$. The pole of the transfer function occurs at a corner frequency of $1/2\pi\tau_2$, where $\tau_2 = R_2C_2$. The signal bandwidth is equal to the pole corner frequency. At low frequencies, the noise gain is $1 + R_2/R_1$. At high frequencies, it is $1 + C_1/C_2$.

REACTIVE PORTION OF PHOTODIODE CIRCUIT

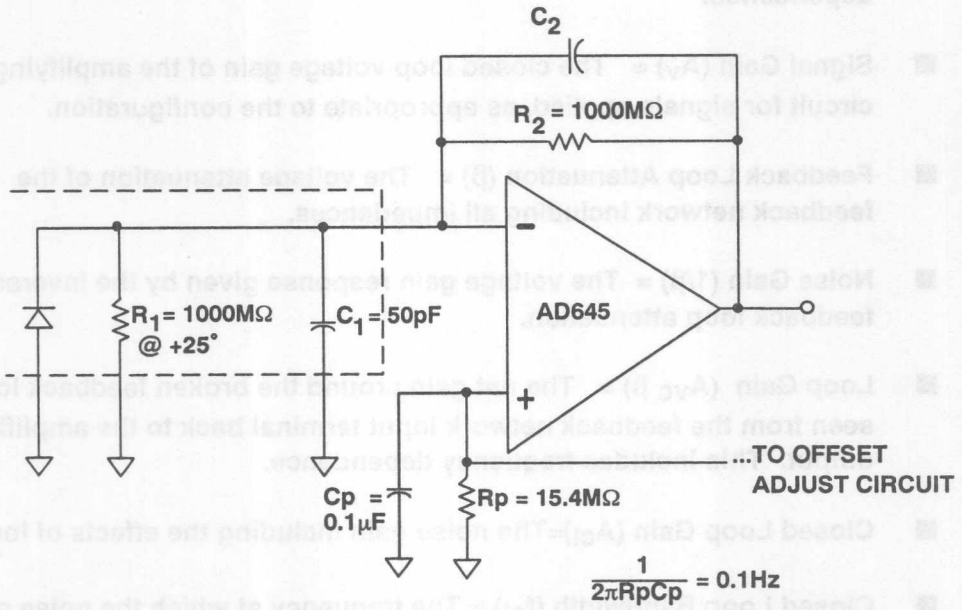


Figure 3.24

BODE PLOT

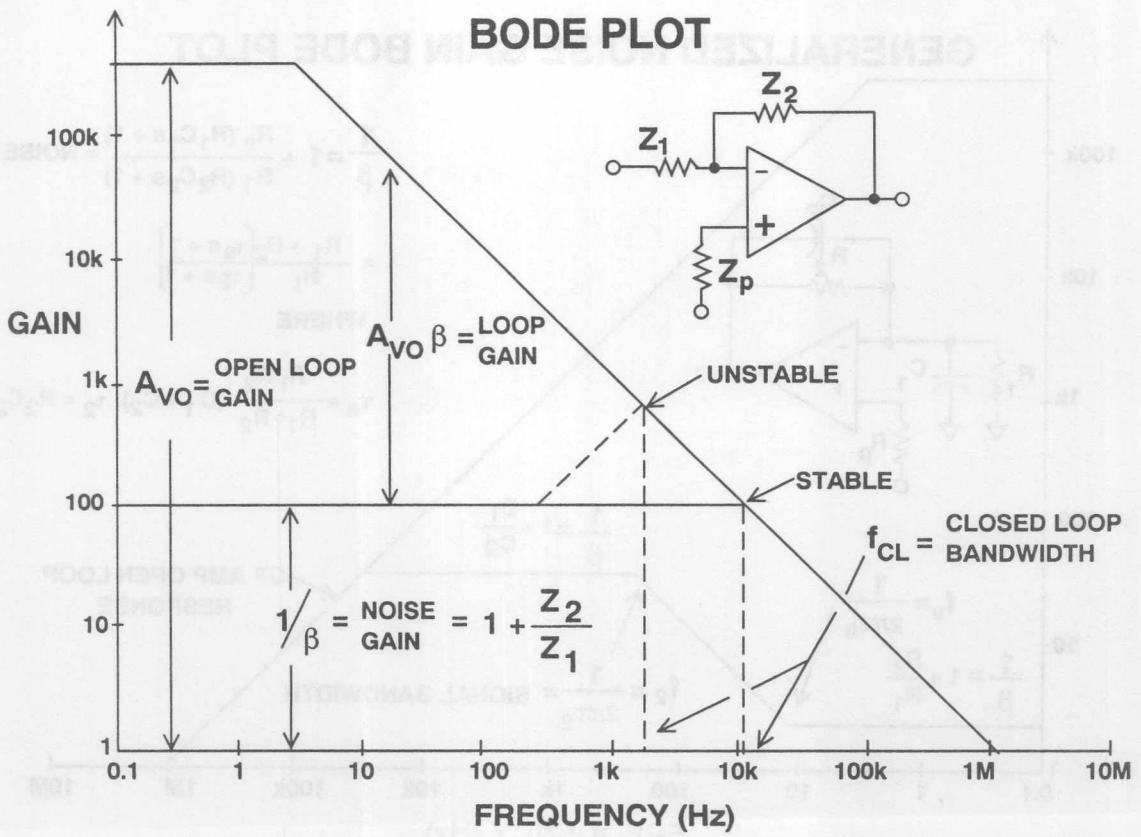


Figure 3.25

BODE PLOT DEFINITIONS

- Open Loop Gain (A_{VO}) = The open loop voltage gain of the basic amplifier without feedback but with loading. This includes frequency dependence.
- Signal Gain (A_V) = The closed loop voltage gain of the amplifying circuit for signals applied, as appropriate to the configuration.
- Feedback Loop Attenuation (β) = The voltage attenuation of the feedback network including all impedances.
- Noise Gain ($1/\beta$) = The voltage gain response given by the inverse of the feedback loop attenuation.
- Loop Gain ($A_{VO}\,\beta$) = The net gain around the broken feedback loop as seen from the feedback network input terminal back to the amplifier output. This includes frequency dependence.
- Closed Loop Gain (A_{CL})=The noise gain including the effects of loop gain.
- Closed Loop Bandwidth (f_{CL}) = The frequency at which the noise gain intersects the open loop gain.

Figure 3.26

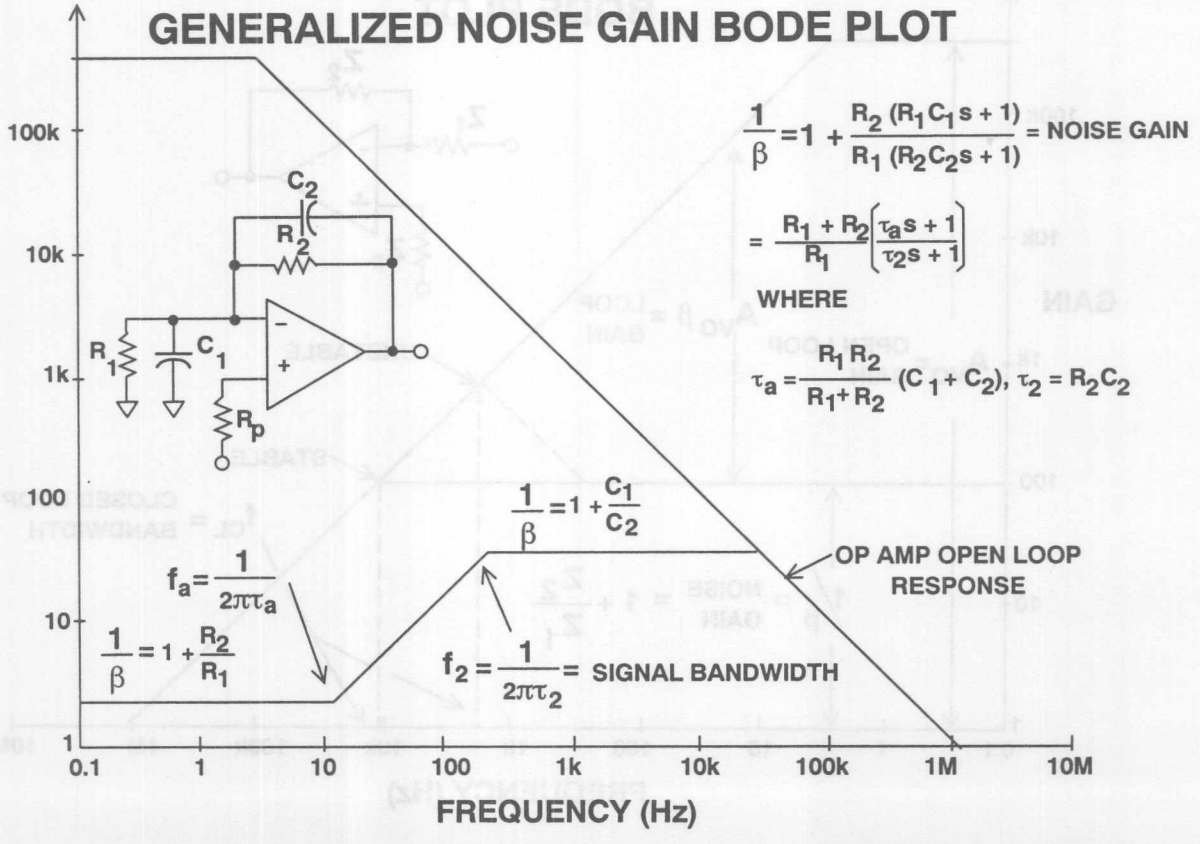


Figure 3.27

In our circuit, the diode capacitance C_1 = 50pF. If we select the feedback capacitor C_2 such that $R_1C_1 = R_2C_2$, the noise gain curve will be flat across the frequency of interest. Remember, however, that since R_1 is a function of temperature, the noise gain curve will be also. If we select C_2 = 50pF, the room temperature noise gain curve will be flat. Figure 3.28 shows the resulting noise gain curve for -25°C, +25°C, and +85°C. Note that the circuit is unconditionally stable at all temperatures.

With C_2 = 50pF, the signal bandwidth is only 3.2Hz. Signal bandwidth can be increased by lowering the value of C_2. This will cause a small amount of peaking in the noise gain. If we choose C_2 = 10pF, the signal bandwidth is increased to 16Hz. The corresponding noise gain curves are shown in Figure 3.29. The penalty for increasing the signal bandwidth is to increase the total amount of noise. This tradeoff will be examined more closely in the next section.

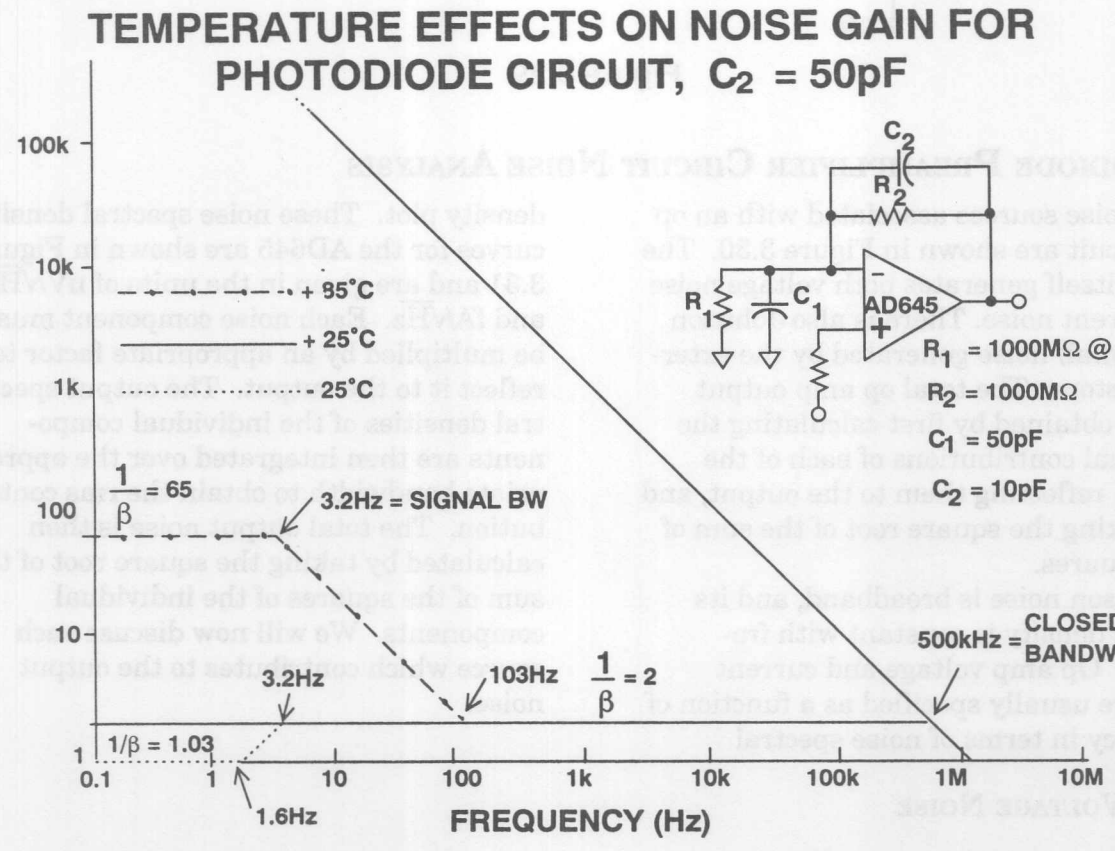


Figure 3.28

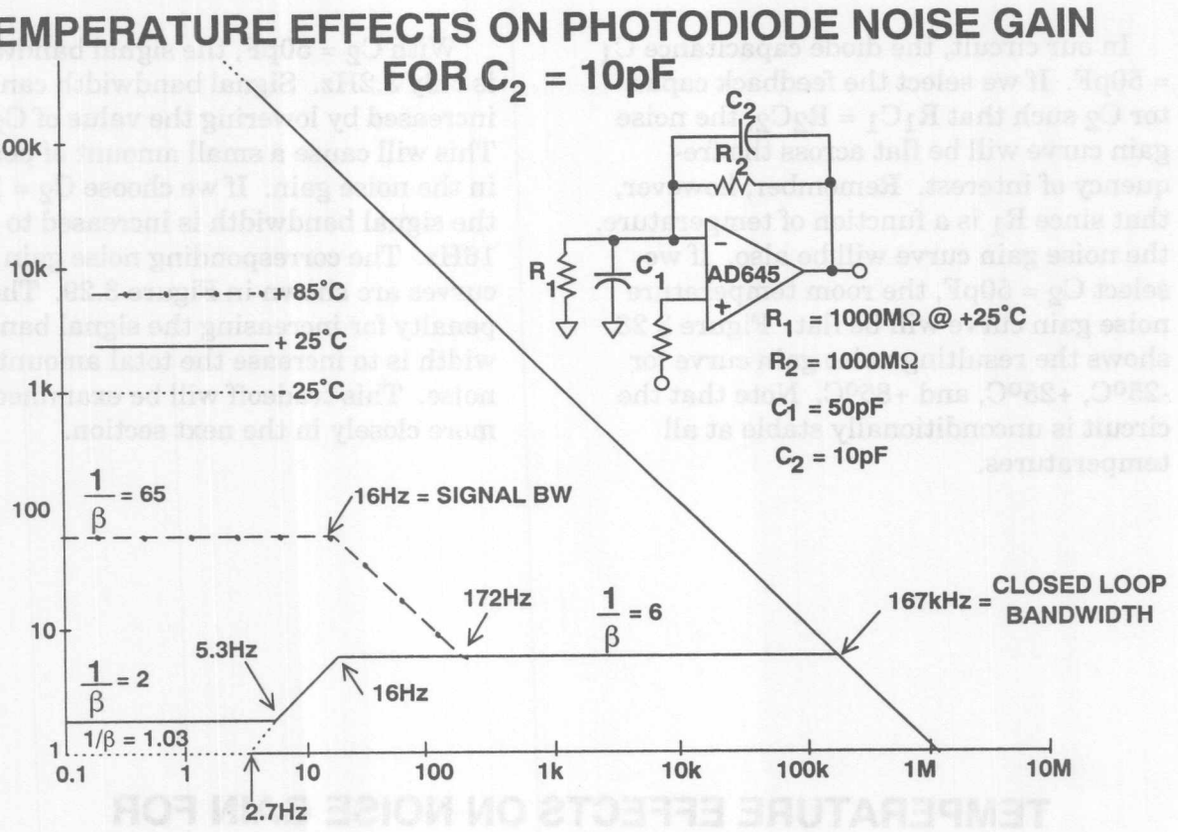


Figure 3.29

PHOTODIODE PREAMPLIFIER CIRCUIT NOISE ANALYSIS

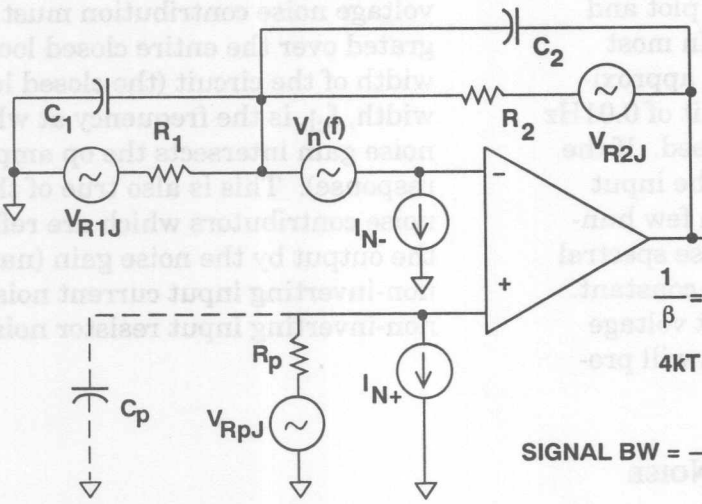
All noise sources associated with an op amp circuit are shown in Figure 3.30. The op amp itself generates both voltage noise and current noise. There is also Johnson (or thermal) noise generated by the external resistors. The total op amp output noise is obtained by first calculating the individual contributions of each of the sources, reflecting them to the output, and then taking the square root of the sum of their squares.

Johnson noise is broadband, and its spectral density is constant with frequency. Op amp voltage and current noise are usually specified as a function of frequency in terms of noise spectral density plot. These noise spectral density curves for the AD645 are shown in Figure 3.31 and are given in the units of $nV/\sqrt{Hz}$ and $fA/\sqrt{Hz}$. Each noise component must be multiplied by an appropriate factor to reflect it to the output. The output spectral densities of the individual components are then integrated over the appropriate bandwidth to obtain the rms contribution. The total output noise is then calculated by taking the square root of the sum of the squares of the individual components. We will now discuss each source which contributes to the output noise.

INPUT VOLTAGE NOISE

In order to obtain the output voltage noise spectral density plot due to the input voltage noise, the input voltage noise spectral density plot is multiplied by noise gain plot. This is easily accomplished using Bode plots on a log-log scale. The total rms output voltage noise due to the input voltage noise is then obtained

OP AMP NOISE MODEL



$$\frac{1}{\beta} = 1 + \frac{Z_2}{Z_1}$$

$$4kT = 0.01656(nV)^2 \frac{}{Hz \cdot \Omega} \ @+25°C$$

$$\text{SIGNAL BW} = \frac{1}{2\pi R_2 C_2}$$

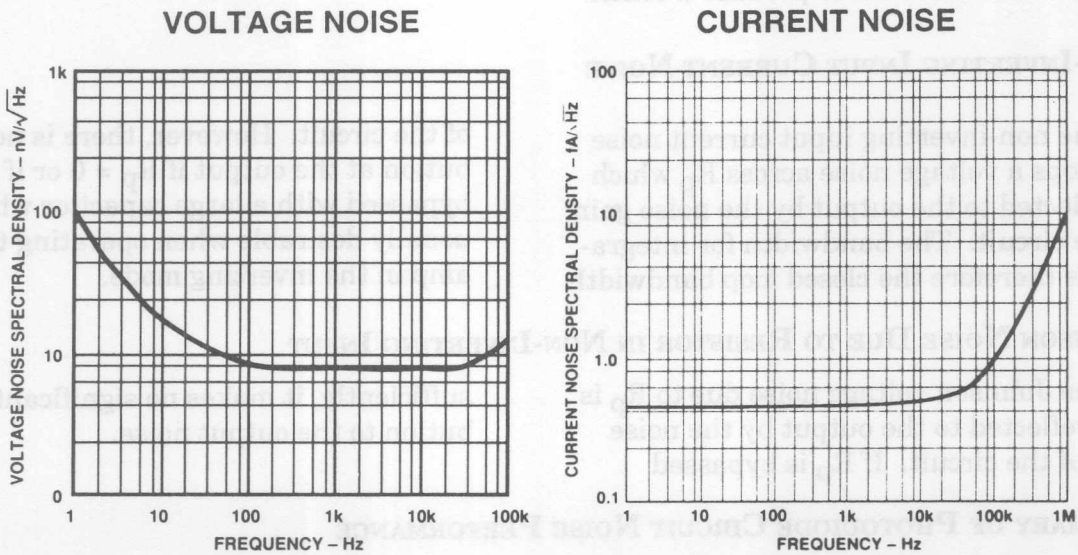
$$V_{on} = \left\{ \int_{f_1}^{f_2} V_n^2(f) \left(1 + \frac{Z_2}{Z_1}\right)^2 df + I_{n+} R_p^2 \int_{f_1}^{f_2} \left(1 + \frac{Z_2}{Z_1}\right)^2 df + 4kTR_p \int_{f_1}^{f_2} \left(1 + \frac{Z_2}{Z_1}\right)^2 df \right.$$

$$\left. + I_{n-}^2 R_2^2 BW + 4kTR_2 BW + 4kTR_1 \left(\frac{R_2}{R_1}\right)^2 BW \right\}^{\frac{1}{2}}$$

f_1 = 0.01Hz, f_2 = CLOSED LOOP BW•1.57, BW = SIGNAL BW•1.57

Figure 3.30

AD645 INPUT NOISE SPECTRAL DENSITIES



$\frac{1}{f}$ CORNER FREQUENCY = 12Hz

Figure 3.31

by integrating the square of the output voltage noise spectral density plot and then taking the square root. In most cases, this integration may be approximated. A lower frequency limit of 0.01Hz in the 1/f region is normally used. If the bandwidth of integration for the input voltage noise is greater than a few hundred Hz, the input voltage noise spectral density may be assumed to be constant. Usually, the value of the input voltage noise spectral density at 1kHz will provide sufficient accuracy.

It is important to note that the input voltage noise contribution must be integrated over the entire closed loop bandwidth of the circuit (the closed loop bandwidth, f_{cl}, is the frequency at which the noise gain intersects the op amp open loop response). This is also true of the other noise contributors which are reflected to the output by the noise gain (namely, the non-inverting input current noise and the non-inverting input resistor noise).

INVERTING INPUT CURRENT NOISE

The inverting input noise current flows through the feedback network to produce a noise voltage contribution at the output The input noise current is approximately constant with frequency, therefore, the integration is accomplished by multiplying the noise current spectral density (measured at 1kHz) by the noise bandwidth which is 1.57 times the signal bandwidth ($1/2\pi R_2C_2$). The factor of 1.57 arises when single-pole 3dB bandwidth is converted to equivalent noise bandwidth (See Reference 4, p. 137).

JOHNSON NOISE DUE TO FEEDFORWARD RESISTOR R_1

The noise current produced by the feedforward resistor R_1 also flows through the feedback network to produce a contribution at the output. The noise bandwidth for integration is also 1.57 times the signal bandwidth.

NON-INVERTING INPUT CURRENT NOISE

The non-inverting input current noise develops a voltage noise across R_p which is reflected to the output by the noise gain of the circuit. The bandwidth for integration is therefore the closed loop bandwidth of the circuit. However, there is no contribution at the output if $R_p = 0$ or if R_p is bypassed with a large capacitor which is usually desirable when operating the op amp in the inverting mode.

JOHNSON NOISE DUE TO RESISTOR IN NON-INVERTING INPUT

The Johnson voltage noise due to R_p is also reflected to the output by the noise gain of the circuit. If R_p is bypassed sufficiently, it makes no significant contribution to the output noise.

SUMMARY OF PHOTODIODE CIRCUIT NOISE PERFORMANCE

Figure 3.32 shows the output noise spectral densities for each of the contributors at +25°C. The various contributors to the output noise along with appropriate multiplying factors and integration bandwidths are summarized in Figure 3.33. The specific results for the photodiode circuit at +25°C are summarized in Figure 3.34.

OUTPUT VOLTAGE NOISE COMPONENTS SPECTRAL DENSITIES AT +25°C

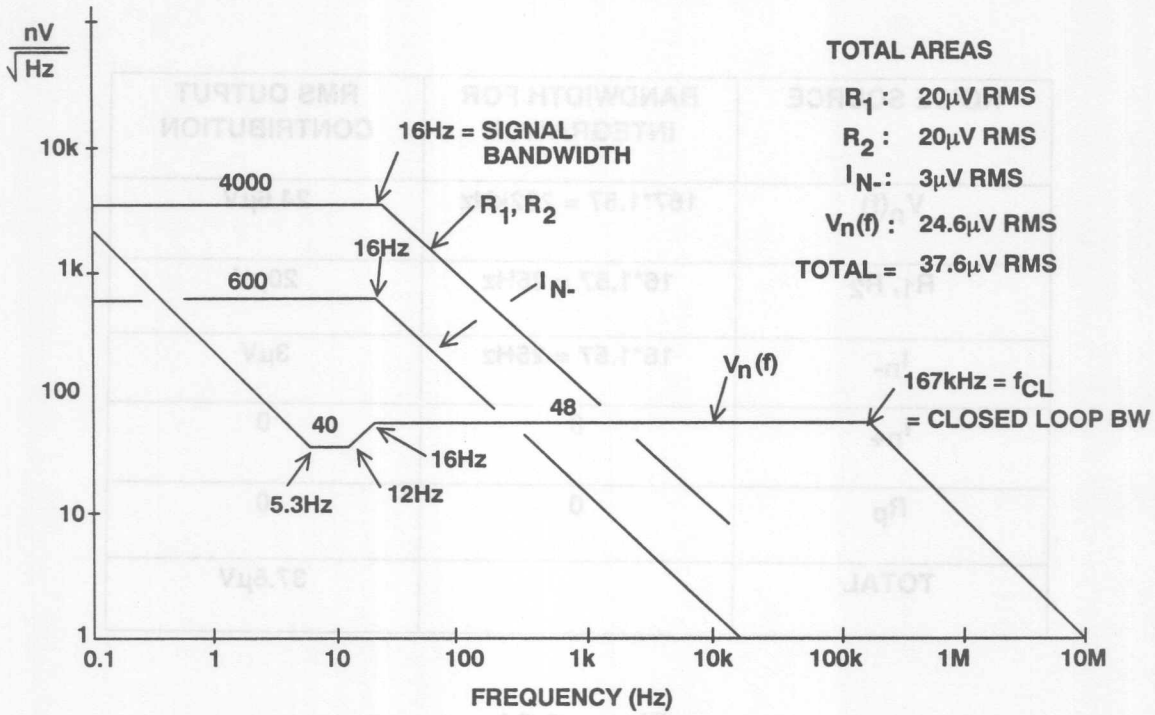


Figure 3.32

SUMMARY OF CONTRIBUTORS TO OUTPUT NOISE

NOISE SOURCE	SPECTRAL DENSITY OF VOLTAGE NOISE	REFLECTED TO OUTPUT	BANDWIDTH FOR INTEGRATION
$V_n(f)$	Frequency Dependent	$V_n(f)$*Noise Gain	1.57*Closed Loop BW
I_{n+}	Constant	$I_{n+}R_p$*Noise Gain	1.57*Closed Loop BW
I_{n-}	Constant	$I_{n-}R_2$	1.57*Signal BW
R_1	Constant	$V_{nR1}(R_2/R_1)$	1.57*Signal BW
R_2	Constant	V_{nR2}	1.57*Signal BW
R_p	Constant	V_{nRp}*Noise Gain	1.57*Closed Loop BW

Figure 3.33

SUMMARY OF NOISE CONTRIBUTORS FOR PHOTODIODE CIRCUIT AT +25°C

NOISE SOURCE	BANDWIDTH FOR INTEGRATION	RMS OUTPUT CONTRIBUTION
$V_n(f)$	167*1.57 = 262kHz	24.6μV
R_1, R_2	16*1.57 = 25Hz	20μV
I_{n-}	16*1.57 = 25Hz	3μV
I_{n+}	0	0
R_p	0	0
TOTAL		37.6μV

Figure 3.34

The effects of high temperature on the noise performance of the circuit are shown in Figure 3.35. There are three factors which cause an overall increase in the output noise. First, the overall noise gain increases considerably at frequencies less than 172Hz. This is due to the temperature dependence of R_1 which has been previously discussed. The second factor is that the output noise contribution due to the current noise of the op amp increases from 600nV/$\sqrt{Hz}$ to 4000nV/$\sqrt{Hz}$. This information comes from the AD645 data sheet. Lastly, the Johnson resistor noise spectral density increases from 4000nV/$\sqrt{Hz}$ to 4500nV/$\sqrt{Hz}$ due to the increase in temperature. Total output noise at +85°C is 50.5μV rms compared to 37.6μV rms at +25°C.

OUTPUT VOLTAGE NOISE COMPONENTS SPECTRAL DENSITIES AT +85°C

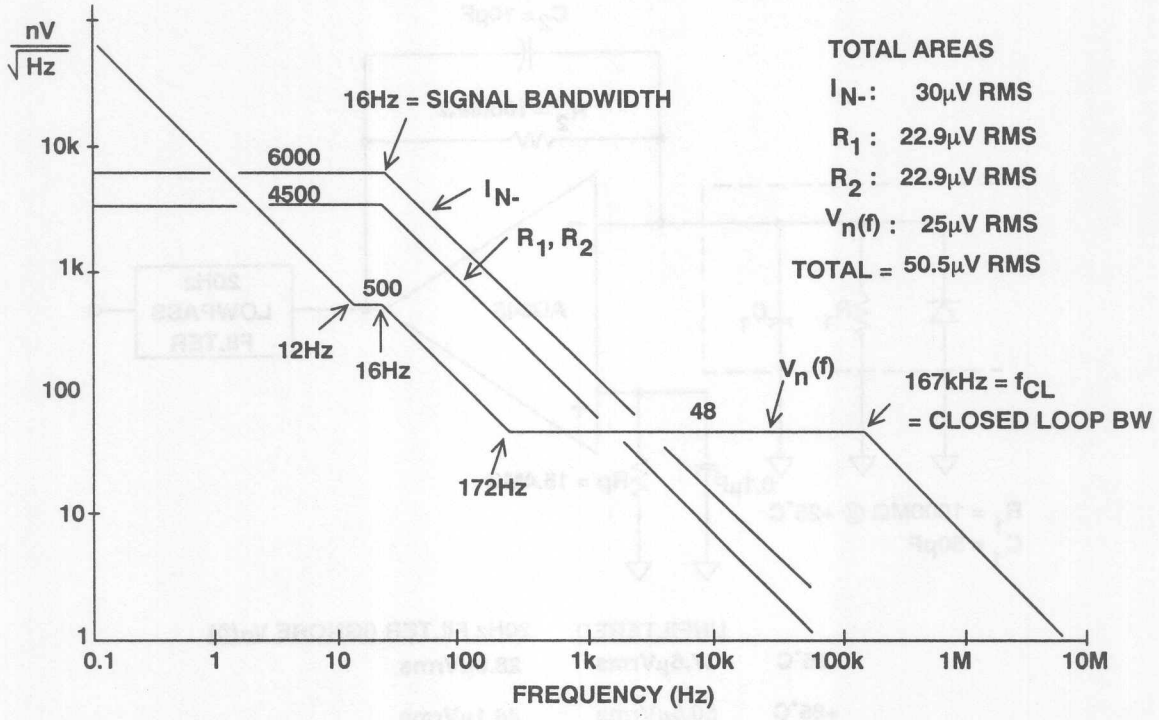
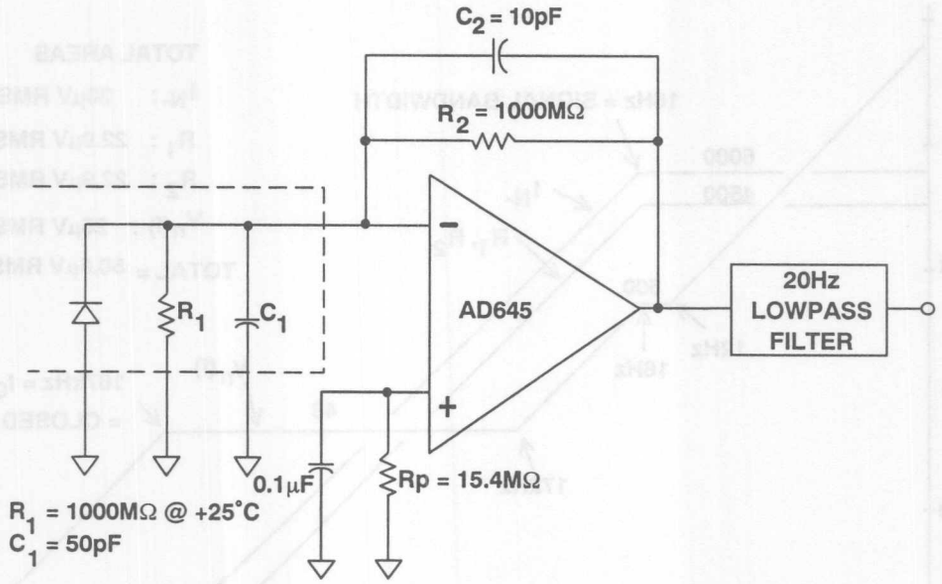


Figure 3.35

NOISE REDUCTION USING OUTPUT FILTERING

From the above analysis, the largest contributor to the output noise voltage at +25°C is the input voltage noise of the op amp reflected to the output by the noise gain. This contributor is large primarily because the noise gain over which the integration is performed extends to a bandwidth of 167kHz (the intersection of the noise gain curve with the open-loop response of the op amp). If the op amp output is filtered by a single pole filter (as shown in Figure 3.36) with a 20Hz cutoff frequency (R = 80MΩ, C = 0.1μF), this contribution is reduced to less than 1μV rms. Notice that the same results would not be achieved simply by increasing the feedback capacitor, C_2. Increasing C_2 lowers the high frequency noise gain, but the integration bandwidth becomes proportionally higher. Larger values of C_2 may also decrease the signal bandwidth to unacceptable levels. The addition of the simple filter reduces the output noise to 28.5μV rms; approximately 75% of its former value. After inserting the filter, the resistor noise and current noise are now the largest contributors to the output noise.

OUTPUT FILTER REDUCES INPUT VOLTAGE NOISE CONTRIBUTION TO OUTPUT NOISE



	UNFILTERED	20Hz FILTER (IGNORE Vn(f))
+25°C	37.6μVrms	28.5μVrms
+85°C	50.5μVrms	44.1μVrms

Figure 3.36

SUMMARY OF CIRCUIT PERFORMANCE

The diagram for the final optimized design of the photodiode circuit is shown in Figure 3.37. Performance characteristics are summarized in Figure 3.38. The total output voltage drift over -25 to +85°C is 25mV. This corresponds to 25pA of diode current, or approximately 0.001 foot-candles. (The level of illumination on a clear moonless night). Limiting the upper operating temperature to +50°C reduces the output voltage drift to only 10mV.

The input sensitivity based on a total output voltage noise of 44μV is obtained by dividing the output voltage noise by the value of the feedback resistor R_2. This yields a minimum detectable diode current of 44fA. If a 12 bit ADC is used to digitize the 10V fullscale output, the weight of the least significant bit (LSB) is 2.5mV. The output noise level is much less than this.

OPTIMIZED PHOTODIODE PREAMP

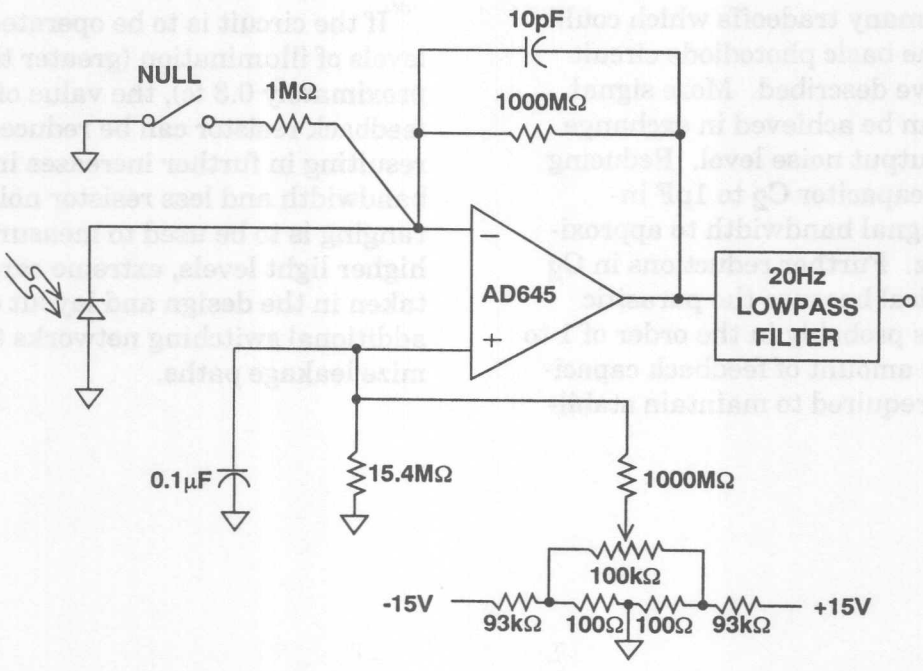


Figure 3.37

PHOTODIODE CIRCUIT PERFORMANCE

- Output Voltage Drift (-25 to +85°C) : 25mV
- Photosensitivity Drift (-25 to +85°C) : 0.001fc
- Output Photosensitivity: 30V/foot-candle
- Total Output Noise: 44μV rms at +85°C
- Output Noise Referred to Input Current: 44fA rms
- Range with R_2 = 1000MΩ: 0.001 to 0.33fc
- Bandwidth: 16Hz

Figure 3.38

PHOTODIODE CIRCUIT TRADEOFFS

There are many tradeoffs which could be made in the basic photodiode circuit design we have described. More signal bandwidth can be achieved in exchange for a larger output noise level. Reducing the feedback capacitor C_2 to 1pF increases the signal bandwidth to approximately 160Hz. Further reductions in C_2 are not practical because the parasitic capacitance is probably in the order of 1 to 2pF. A small amount of feedback capacitance is also required to maintain stability.

If the circuit is to be operated at higher levels of illumination (greater than approximately 0.3 fc), the value of the feedback resistor can be reduced thereby resulting in further increases in circuit bandwidth and less resistor noise. If gain-ranging is to be used to measure the higher light levels, extreme care must be taken in the design and layout of the additional switching networks to minimize leakage paths.

PHOTODIODE CIRCUIT TRADEOFFS

- **Signal Gain / Signal Bandwidth**
- **Bandwidth / Noise**
- **Sensitivity / Gain Ranging**

Figure 3.39

T NETWORK ANALYSIS

A popular circuit using "T" feedback for converting small currents into voltages is shown in Figure 3.40. The equations relating the input current to the output voltage as well as the equations for the noise gain, $1/\beta$, are given. Notice that R_3 and R_4 constitute an attenuator which attenuates the output voltage by an amount equal to approximately $R_3/(R_3 + R_4)$. The attenuated voltage is then applied to the op amp summing junction through R_2. The effect of the attenuator is to increase the signal gain by an amount equal to approximately $1 + R_4/R_3$ (assuming that $R_2 >> R_3$). The transimpedance "gain" of the circuit is increased from R_2 to approximately $R_2(1+R_4/R_3)$.

This circuit may be useful especially when amplifying very low input currents such as in the photodiode preamp. In Figure 3.41, the 1000MΩ feedback resistor is replaced with a 100MΩ resistor and a 10X attenuator. The overall transimpedance gain remains approximately 1000MΩ, but the need for the extremely large resistor is eliminated. Notice, however, that the noise gain of the circuit is increased by a factor of 6. The T-network circuit will therefore be 6 times as sensitive to input offset voltage drift and also input noise voltage.

The effect on output noise due to the feedback resistor is even more interesting. Reducing the 1000MΩ resistor to 100MΩ reduces the resistor Johnson noise by a factor of $\sqrt{2}$. However, this noise is gained up by a factor of 10 due to the T network attenuator. The net effect is to *increase* the overall output noise due to the feedback resistor by a factor of $\sqrt{10}$.

In the photodiode design example just completed, we could probably tolerate an increase in output noise due to the increase in noise gain, but the increase in sensitivity to input offset voltage would be undesirable.

T NETWORK

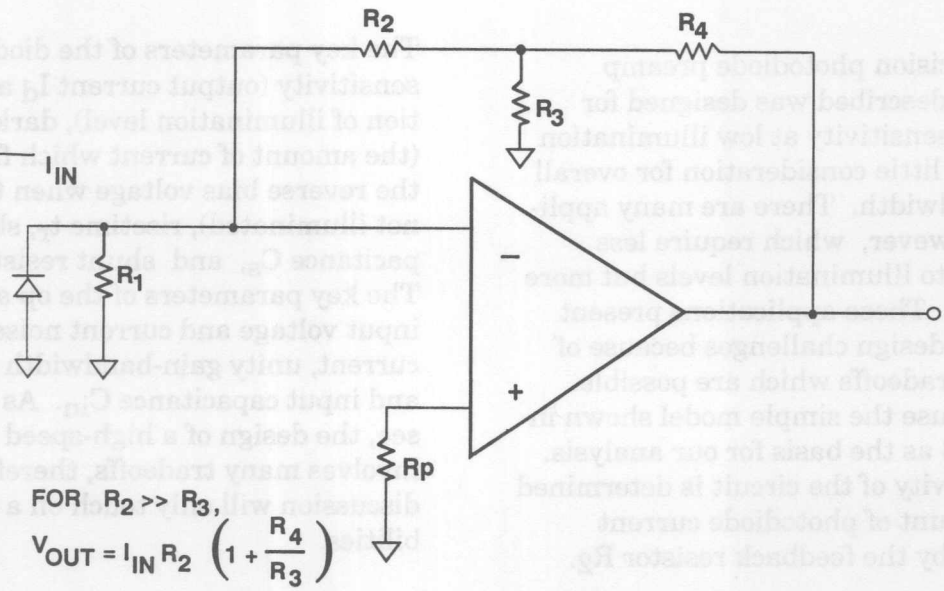


Figure 3.40

T NETWORK INCREASES RESISTOR NOISE AND NOISE GAIN

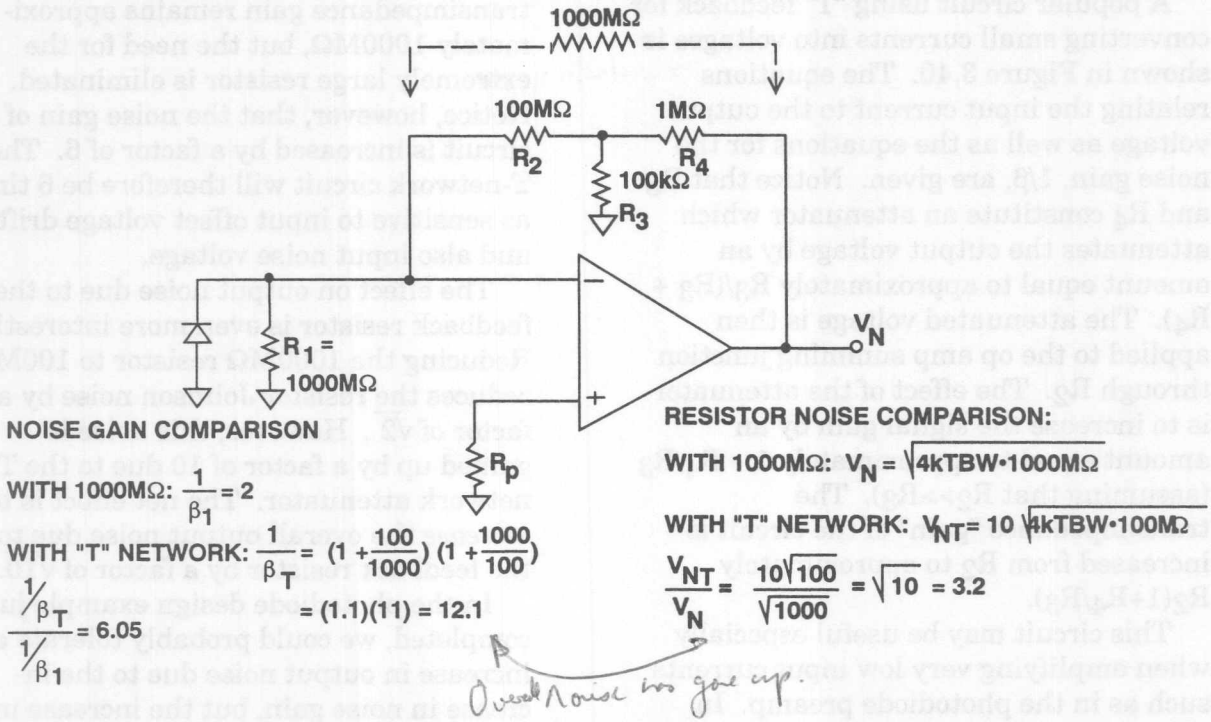


Figure 3.41

HIGH SPEED PHOTODIODE PREAMPLIFIERS

WALT KESTER, SCOTT WURCER

The precision photodiode preamp previously described was designed for maximum sensitivity at low illumination levels with little consideration for overall signal bandwidth. There are many applications, however, which require less sensitivity to illumination levels but more bandwidth. These applications present significant design challenges because of the many tradeoffs which are possible.

We will use the simple model shown in Figure 3.43 as the basis for our analysis. The sensitivity of the circuit is determined by the amount of photodiode current multiplied by the feedback resistor R_2.

The key parameters of the diode are its sensitivity (output current I_d as a function of illumination level), dark current (the amount of current which flows due to the reverse bias voltage when the diode is not illuminated), risetime t_r, shunt capacitance C_S, and shunt resistance R_{sh}. The key parameters of the op amp are its input voltage and current noise, bias current, unity gain-bandwidth product, f_u, and input capacitance C_{in}. As we shall see, the design of a high-speed preamp involves many tradeoffs, therefore this discussion will only touch on a few possibilities.

APPLICATIONS OF WIDE BANDWIDTH PHOTODIODE CIRCUITS

- Ring Laser Gyro Systems
- Bar Code Readers
- Fast Scanners
- Document Scanners
- Fax Machines
- Fiber Optic Receivers

Figure 3.42

HIGH BANDWIDTH PHOTODIODE PREAMP EQUIVALENT CIRCUIT

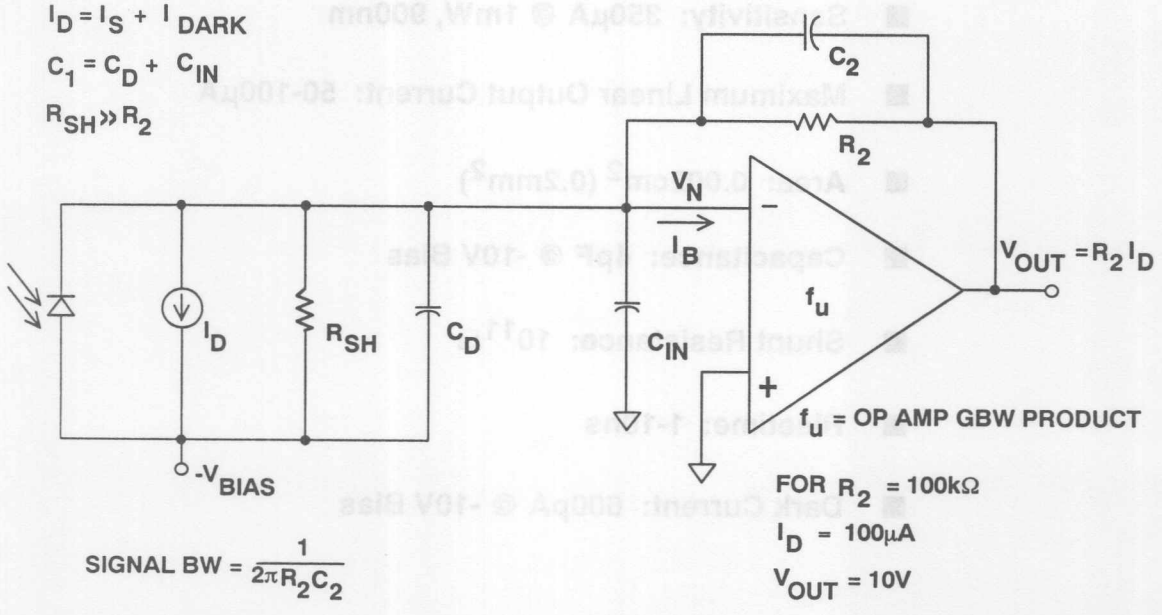


Figure 3.43

CHARACTERISTICS OF HIGH SPEED PHOTODIODES

The Motorola 5082-4204 PIN Photodiode will be used as an example for our discussion. Its characteristics are given in Figure 3.44. It is typical of many commercially available PIN photodiodes. As in most high speed photodiode applications, the diode is operated in the reverse-biased or *photoconductive* mode. This greatly lowers the junction capacitance, but causes a small amount of *dark current* to flow even when the diode is not illuminated.

It is, therefore, the combination of dark current and noise which usually determines the lowest level of detectable light. Photodiodes are linear with illumination level up to approximately 50 to 100μA of output current. With a dark current of 600pA, this give a possible dynamic range of approximately 100,000, or 100dB, neglecting the effects of noise.

Using the simple circuit shown in Figure 3.43, assume that we wish to have a fullscale output of 10V for a diode current of 100μA. The value of the feedback resistor R_2 must therefore be:

$$R_2 = 10V/100\mu A = 100k\Omega.$$

CHARACTERISTICS OF TYPICAL HIGH SPEED PIN PHOTODIODE OPERATED IN PHOTOCONDUCTIVE MODE

- **Sensitivity: 350μA @ 1mW, 900nm**
- **Maximum Linear Output Current: 50-100μA**
- **Area: 0.002cm^2 (0.2mm^2)**
- **Capacitance: 4pF @ -10V Bias**
- **Shunt Resistance: $10^{11}\Omega$**
- **Risetime: 1-10ns**
- **Dark Current: 600pA @ -10V Bias**

Figure 3.44

DETERMINING CIRCUIT FREQUENCY RESPONSE

The simple model shown in Figure 3.43 may also be used to determine the overall frequency response of the photodiode circuit. The total input capacitance C_1 is the sum of the diode capacitance C_d and the op amp input capacitance C_{in}. This capacitance creates a feedback pole in the frequency response. Noise gain plots for the circuit are shown in Figure 3.45, and Bode gain and phase plots in Figure 3.46.

With no compensation capacitor (C_2 = 0), the circuit is unstable because the phase shift at unity loop gain (see Figure 3.45) is 180°, corresponding to zero phase margin. The effects of adding the compensation capacitor C_2 are also shown in the Figure 3.45 and 3.46.

At this point, we should distinguish between the *signal bandwidth* and the *closed loop bandwidth*. The signal bandwidth is the frequency at which the output voltage divided by the diode current is attenuated by 3dB. The closed loop bandwidth, on the other hand, is the frequency at which the noise gain curve intersects the open loop gain curve.

The absolute maximum signal bandwidth achievable in this circuit f_{max} is the geometric mean of $1/2\pi R_2C_1$ and the unity gain-bandwidth frequency of the op amp f_u:

$$f_{max} = \sqrt{\frac{f_u}{2\pi R_2 C_1}}$$

The circuit may be stabilized by adding a feedback capacitor C_2 which creates a zero in the transfer function as shown in the noise gain plot of Figure 3.45. If we desire the maximum signal bandwidth, select C_2 such that the signal bandwidth, $1/2\pi R_2C_2$ is equal to f_{max}, or

$$\frac{1}{2\pi R_2 C_2} = \sqrt{\frac{f_u}{2\pi R_2 C_1}} \quad ,$$

EFFECT OF COMPENSATION ON PREAMP NOISE GAIN AND SIGNAL BANDWIDTH

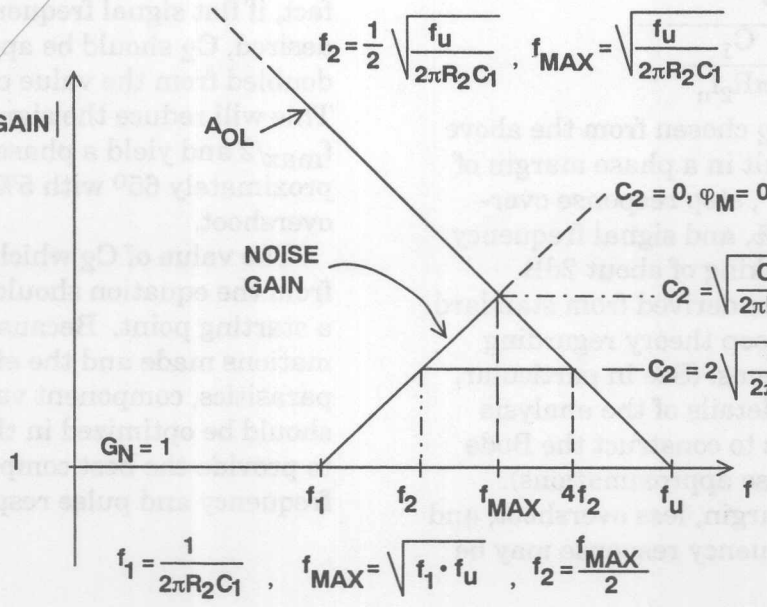


Figure 3.45

BODE PLOTS SHOW EFFECTS OF COMPENSATION ON PHASE MARGIN

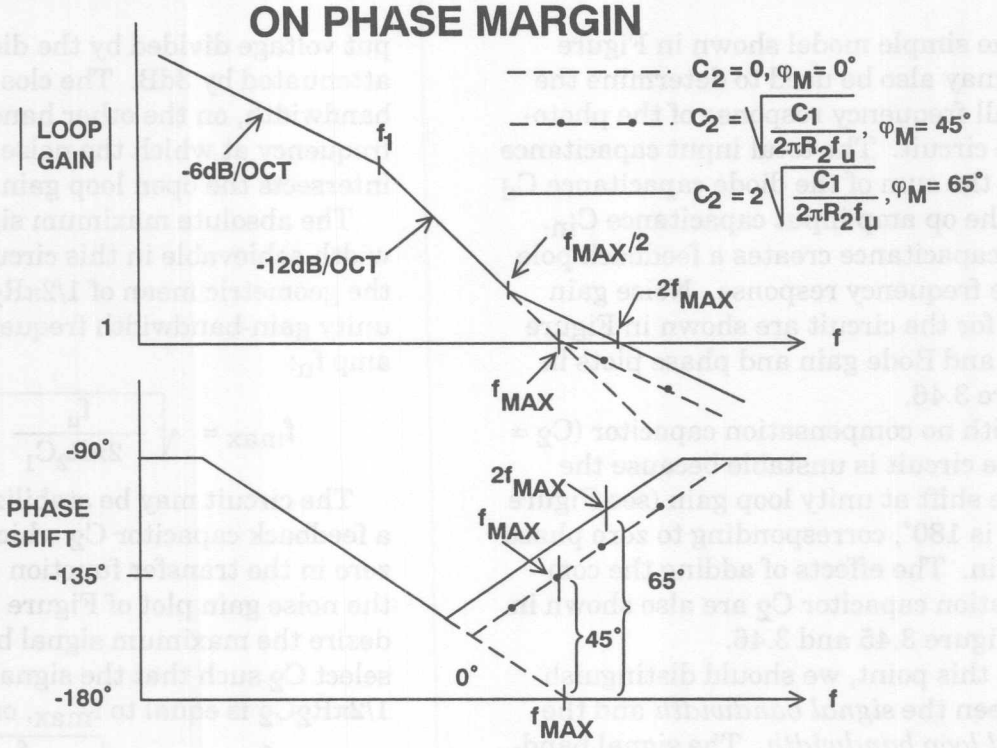


Figure 3.46

and solving for C_2 :

$$C_2 = \sqrt{\frac{C_1}{2\pi R_2 f_u}}$$

The value of C_2 chosen from the above equation will result in a phase margin of approximately 45°, step response overshoot of about 16%, and signal frequency response gain peaking of about 2dB. These numbers are derived from standard feedback control loop theory regarding second-order systems. (See in particular, Reference 11 for details of the analysis and easy methods to construct the Bode plot gain and phase approximations).

More phase margin, less overshoot, and flatter signal frequency response may be obtained by increasing the value of C_2. In fact, if flat signal frequency response is desired, C_2 should be approximately doubled from the value calculated above. This will reduce the signal bandwidth to $f_{max}/2$ and yield a phase margin of approximately 65° with 5% step response overshoot.

The value of C_2 which is computed from the equation should only be used as a starting point. Because of the approximations made and the effects of circuit parasitics, component variations, etc., C_2 should be optimized in the actual circuit to provide the best compromise between frequency and pulse response.

CONDITIONS FOR MAXIMALLY FLAT SIGNAL FREQUENCY RESPONSE WITH APPROXIMATELY 65° PHASE MARGIN AND 5% STEP FUNCTION OVERSHOOT

- $C_2 \approx 2\sqrt{\frac{C_1}{2\pi R_2 f_u}}$, and
- Signal Bandwidth $\approx \frac{1}{2}\sqrt{\frac{f_u}{2\pi R_2 C_1}}$.

Figure 3.47

SELECTING THE PROPER OP AMP

The relationship between the various circuit parameters and the signal bandwidth it given by the following approximate equations:

$$C_2 \approx 2\sqrt{\frac{C_1}{2\pi R_2 f_u}} \text{ , and}$$

Signal Bandwidth =

$$\frac{1}{2\pi R_2 C_2} = \frac{1}{2}\sqrt{\frac{f_u}{2\pi R_2 C_1}}$$

The equation for signal bandwidth can be simplified to show proportionality only, as shown in the general selection process given in Figure 3.48.

Since R_2 has already been determined by sensitivity requirements, the ratio f_u/C_1 may be used along with bias current and voltage noise to evaluate various op amps for maximum signal bandwidth in this application. Note that $C_1 = C_d + C_{in}$, where C_{in} is the op amp's input capacitance. In any event, making $C_{in} < C_d$, and maximizing the ratio f_u/C_1 provides the greatest signal bandwidth in the circuit, assuming the other parameters of the op amp are acceptable. If you plug in some typical numbers, you will quickly find that the op amp and not the diode is the chief element limiting the frequency response of the circuit. A comparison table between various low bias current FET-input op amps is given in Figure 3.49 to assist in the selection process.

Because the feedback resistor R_2 is normally between 100 and 300kΩ, the effects of the amplifier input current noise may usually be neglected, especially when using FET-input op amps which have inherently low input current noise specifications.

GENERALIZED OP AMP SELECTION FLOW CHART FOR HIGH SPEED PHOTODIODE PREAMP

- SIGNAL BW ~ $\sqrt{\frac{f_u}{R_2C_1}}$, f_u = Op Amp Unity Gain Bandwidth
  C_1 = Input Capacitance = $C_d + C_{in}$.
- Minimize Value of R_2 Based on Gain Requirements
- Try and make op amp input capacitance, $C_{in} \leq C_d$
- Maximize f_u/C_{in}, Minimize Voltage and Current Noise
- Calculate C_2 and Signal Bandwidth
- Examine Bias Current and Noise Effects on Circuit

Figure 3.48

OP AMP COMPARISON TABLE FOR WIDE BANDWIDTH PHOTODIODE PREAMP APPLICATIONS

	Unity GBW Product, f_u (MHz)	Input Capacitance C_{in} (pF)	f_u/C_{in} (MHz/pF)	Input Bias Current I_b (pA)	Voltage Noise @10kHz (nV/$\sqrt{Hz}$)
AD645	1	1	1	1.5	8
AD743	4.5	20	0.2	250	2.9
AD745*	20	20	1	250	2.9
AD744	13	5.5	2.4	100	16
AD845	16	8	2	500	18
AD843	34	6	5.7	600	19
AD829	500	5	100	7000	2

* Stable for Noise Gains $\geq$ 5. Usually the Case, Since High Frequency Noise Gain = $1 + C_1/C_2$, and C_1 Usually $\geq 4C_2$.

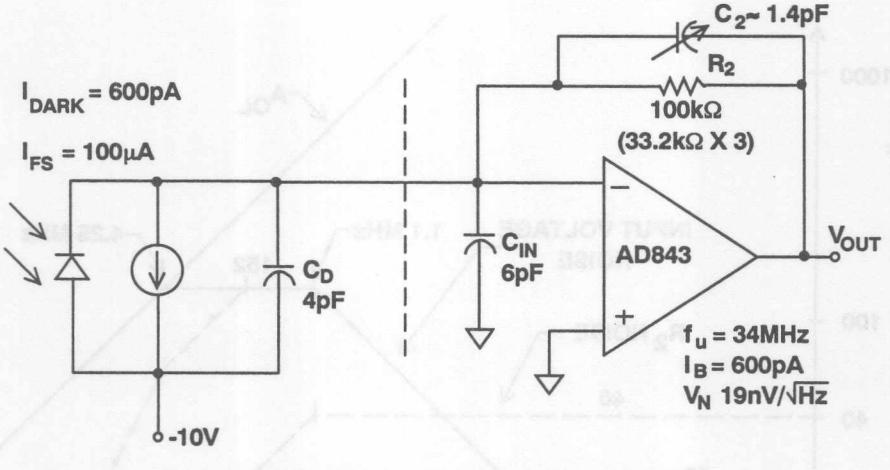
Figure 3.49

For the example under consideration, we will choose the FET-input AD843 op amp which has a unity gain-bandwidth product of 34MHz and an input capacitance of 6pF. Using the circuit parameters: $C_1 = C_d + C_{in} = 4 + 6 = 10pF$, $f_u = 34MHz$, $R_2 = 100k\Omega$, we find that $C_2 \approx 1.4pF$. This yields a signal bandwidth of 1.14MHz. In actual practice, C_2 should be a 2pF low leakage variable capacitor so that the circuit may be optimized for best compromise between frequency and transient performance. The 100kΩ resistor should be made up of three 33.2kΩ film resistors to minimize the associated stray capacitance. The circuit is shown in Figure 3.50.

ESTIMATING CIRCUIT NOISE PERFORMANCE

Performing exact noise calculations for op amp circuits can become a very tedious matter. It is much more productive to make intelligent approximations and simplify the process by identifying the chief noise contributors and neglecting the others.

1 MHz PHOTODIODE PREAMP USING AD843 OP AMP



SIGNAL BW ≈ 1.14 MHz
PHASE MARGIN ≈ 65°

Figure 3.50

STEPS IN ESTIMATING TOTAL AMPLIFIER OUTPUT NOISE

- Approximate the Noise Gain Curve for the Circuit
- Multiply the Noise Gain Curve by the Input Voltage Noise Spectral Density (Use Value at 1 or 10kHz) to Obtain the Output Noise Voltage Spectral Density
- Use Approximation Techniques to Integrate the Output Noise Voltage Spectral Density
- Calculate the Output Voltage Noise Due to the Feedback Resistor
- Calculate the Output Voltage Noise Due to the Amplifier Input Current Noise (May be Neglected in This Example)
- Calculate the Total Output Voltage Noise by Taking the Square Root of the Sum of the Squares of the Individual Components

Figure 3.51

1.1 MHz PREAMP OUTPUT VOLTAGE NOISE COMPONENTS SPECTRAL DENSITIES

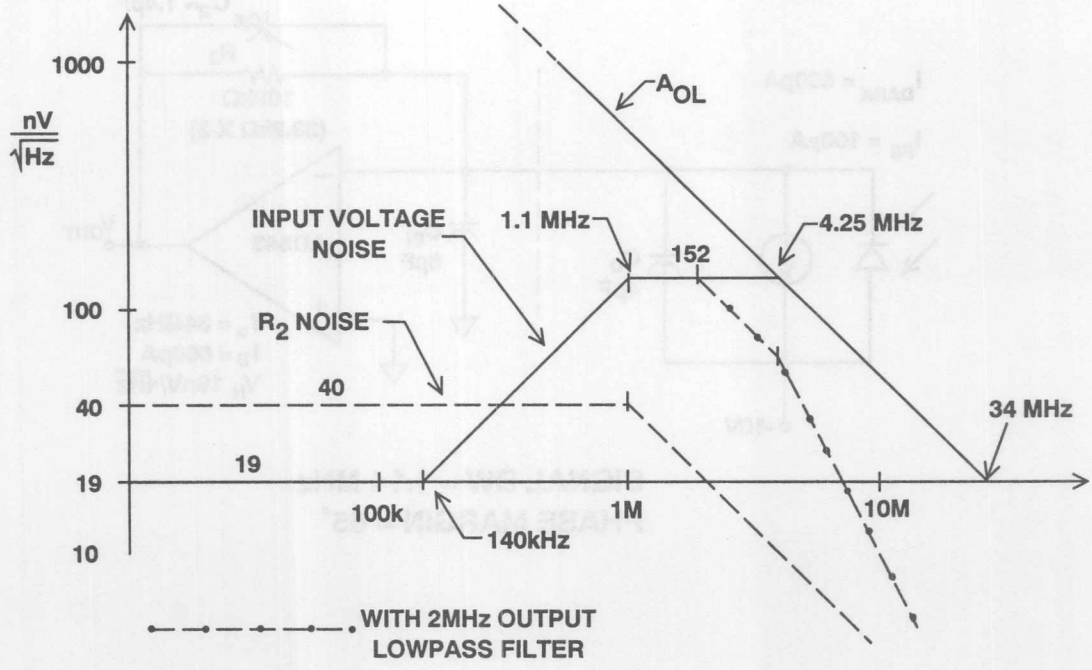


Figure 3.52

The steps used in calculating the total output noise are summarized in Figure 3.51. The total output voltage noise spectral density for the circuit using the AD843 op amp is shown in Figure 3.52. The most significant contributor to the total output noise is the input voltage noise of the op amp. The voltage noise of the 100kΩ feedback resistor should also be considered, but the contribution due to the op amp's input current noise may be neglected. The input voltage noise contribution must be integrated over the output voltage noise spectral density plot shown in Figure 3.52.

For simplicity, we will use the input voltage noise spectral density at 10kHz ($19nV/\sqrt{Hz}$) for all frequencies in the calculations. The output voltage noise over the three regions of interest are given in Figure 3.53. The noise gain is assumed to be unity in Region 1 between dc and 140kHz. In Region 2, between 140kHz and 1.1MHz, the noise gain is approximated by the geometric mean of the two noise gains: 1 and 8, or = 2.8. This yields an output noise spectral density of $54nV/\sqrt{Hz}$. This point was somewhat arbitrarily chosen to simplify the mathematics, but the approximation contributes negligible error. The noise gain is 8 between 1.1MHz and 4.25MHz yielding an output noise spectral density of $152nV/\sqrt{Hz}$. The correction factor of 1.57 is needed to convert the single-pole closed loop bandwidth into its equivalent noise bandwidth.

Now, we must calculate the output noise due to the 100kΩ resistor. Since a 1000Ω resistor has a noise spectral density of $4nV/\sqrt{Hz}$, the noise of the 100kΩ resistor integrated over the signal bandwidth of 1.1MHz is given by:

$$R_2 \text{ Output Noise} = \frac{4nV}{\sqrt{Hz}}\sqrt{\frac{100000}{1000}}\sqrt{1.1x10^6x1.57Hz} = 53\mu V \text{ rms.}$$

Total output voltage noise is the root-sum of the squares of the three contributing voltage noise regions plus the feedback resistor noise, or approximately 346μV rms.

Notice that the largest contributor to the total output voltage noise is due to the noise within the gain-peaking region between 1.1MHz and 4.25MHz. In fact, this contribution itself is 338μV rms, making the other contributors negligible.

This calculation illustrates another important principle in making approximate noise calculations which essentially says that if there is a significant amount of noise at the higher frequencies of interest, the error caused by neglecting lower frequency contributors is small.

The total output voltage noise is now reflected to the input as an equivalent input noise current by dividing by the feedback resistor R_2.

This value should now be compared with the op amp input bias current of 600nA and the diode dark current of 600nA. For this example, the noise becomes the chief factor limiting the resolution of the system and not the bias current or the dark current.

A single pole external lowpass filter may be used to reduce the total high frequency output noise contribution as shown in Figure 3.55. The total output noise is reduced to 196μV rms using a single pole external 2Mhz filter, and the equivalent input current noise becomes 1960pA rms.

SUMMARY OF OUTPUT VOLTAGE NOISE CONTRIBUTIONS

Noise Source	Output Spectral Density, $nV/\sqrt{Hz}$	Bandwidth for Integration, MHz	Output Voltage Noise μV rms
V_n, dc to 140kHz	19×1 = 19	0.140	7.1
V_n, 140kHz to 1.1MHz	19×2.8 = 54	0.996	54
V_n, 1.1MHz to 4.25MHz	19×8 = 152	3.15×1.57	338
Resistor, R_2	40	1.1×1.57	53
TOTAL			346

Figure 3.53

REFLECTING OUTPUT VOLTAGE NOISE TO AN EQUIVALENT INPUT NOISE CURRENT

- Equivalent Input Current Noise = 346μV rms/100,000Ω = 3460pA rms.
- Op Amp Input Bias Current = 600pA
- Photodiode Dark Current = 600pA
- Dynamic Range $= 20\log_{10}\left(\frac{100\mu A}{3460pA}\right) = 89dB.$

Figure 3.54

EFFECT OF OUTPUT FILTER ON NOISE

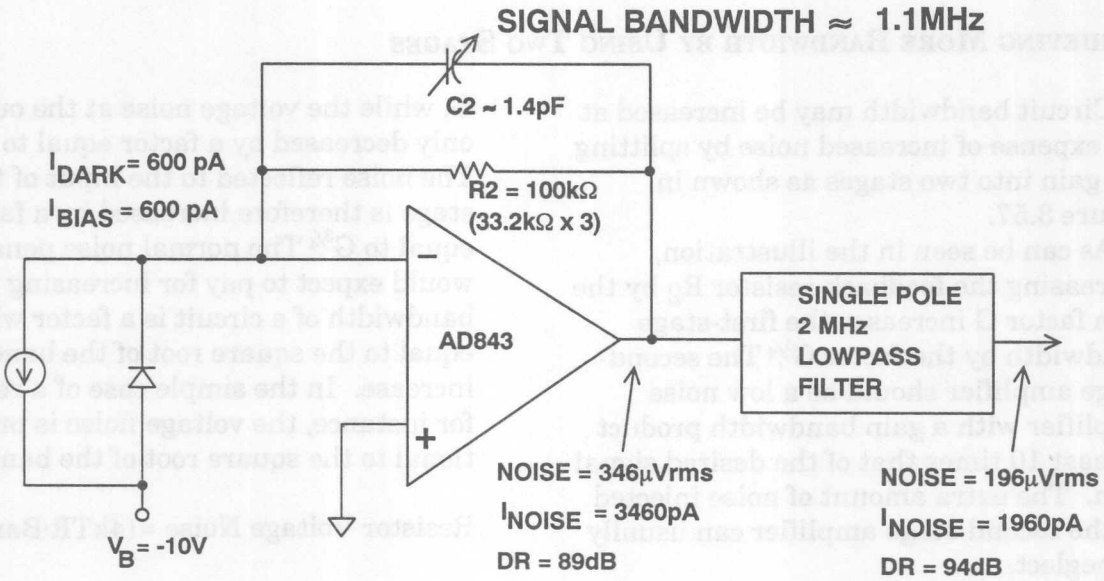


Figure 3.55

EFFECTS OF 2MHz OUTPUT FILTER ON OUTPUT VOLTAGE NOISE

- Equivalent Input Current Noise = 196μVrms/100,000Ω = 1960pA rms.
- Op Amp Input Bias Current = 600pA
- Photodiode Dark Current = 600pA
- Dynamic Range $= 20\log_{10}\left(\frac{100\mu A}{1960pA}\right) = 94dB.$

Figure 3.56

The external 2MHz lowpass filter will not have a significant effect on the signal bandwidth, but reduces the effective output rms noise by a factor of almost two. If the filter is to be used, its effects on the circuit's pulse response must be evaluated during the optimization process.

ACHIEVING MORE BANDWIDTH BY USING TWO STAGES

Circuit bandwidth may be increased at the expense of increased noise by splitting the gain into two stages as shown in Figure 3.57.

As can be seen in the illustration, decreasing the feedback resistor R_2 by the gain factor G increases the first-stage bandwidth by the factor $G^{1/2}$ The second-stage amplifier should be a low noise amplifier with a gain bandwidth product at least 10 times that of the desired signal gain. The extra amount of noise injected by the second-stage amplifier can usually be neglect.

The noise penalty due to this approach may be explained as follows. The gain of the first stage is decreased by the factor G, while the voltage noise at the output is only decreased by a factor equal to $G^{1/4}$ The noise reflected to the input of the first stage is therefore increased by a factor equal to $G^{3/4}$ The normal noise penalty one would expect to pay for increasing the bandwidth of a circuit is a factor which is equal to the square root of the bandwidth increase. In the simple case of a resistor, for instance, the voltage noise is proportional to the square root of the bandwidth:

Resistor Voltage Noise $= (4kTR \cdot \text{Bandwidth})^{1/2}$.

USING TWO GAIN STAGES INCREASES BANDWIDTH BUT INCURS NOISE PENALTY WHEN REFLECTED TO INPUT

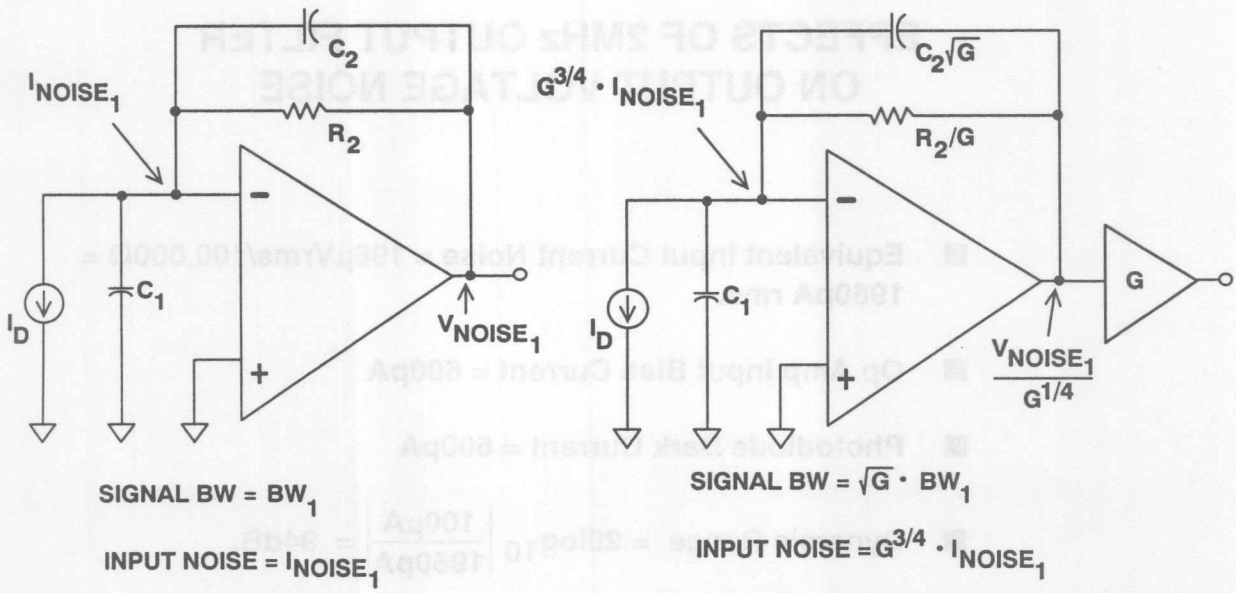


Figure 3.57

If the bandwidth increases by a factor of $G^{1/2}$, then one would expect the noise voltage to increase by a factor equal to $(G^{1/2})^{1/2} = G^{1/4}$. The noise "penalty" paid in the above photodiode is therefore proportional to $G^{1/2}$, since the actual increase is $G^{3/4}$.

USING A COMPOSITE AMPLIFIER CONFIGURATION TO INCREASE THE EFFECTIVE GAIN-BANDWIDTH PRODUCT

Figure 3.58 shows a circuit configuration which takes advantage of the low bias current of a FET input amplifier such as the AD843 and the high gain-bandwidth product (600MHz) of a bipolar op amp such as the AD829. The AD829 is configured and compensated for a gain of 2. The signal bandwidth of the AD829 in this configuration is approximately 71MHz, which is much greater than the unity gain bandwidth product of the AD843 of 34MHz. The net result is that the unity gain bandwidth product f_u of the composite amplifier is increased by approximately a factor of 2. The equations developed previously indicate that if f_u is doubled, the signal bandwidth increases by a factor equal to $\sqrt{2}$.

The composite circuit may be best optimized initially by using ADSpice models of the amplifiers, and final optimization done on the actual circuit.

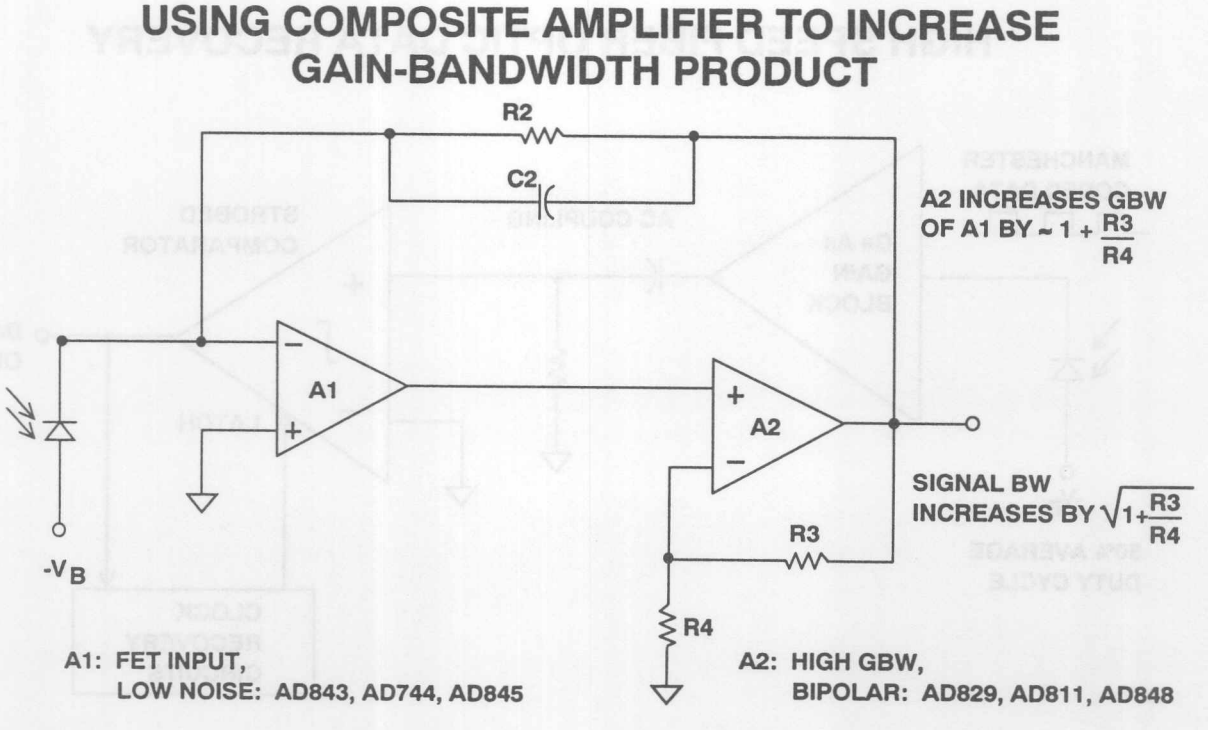


Figure 3.58

HIGH SPEED FIBER OPTIC RECEIVERS

When the primary function of the photodiode preamp is to amplify digital data from a fiber optic link, even more tradeoffs become possible in achieving higher speeds. In a fiber optic data transmission system such as the one shown in Figure 3.59, the primary purpose of the preamp is to amplify the photodiode current to a voltage level which is sufficient to drive the input of threshold comparator. In these applications, the data is coded in such a manner that the average duty cycle of the data is always 50% regardless of the actual bit pattern. A Manchester coding scheme is one way to accomplish this. Since the average duty cycle of the data stream is always 50%, ac coupling is possible, and the need for wideband precision op amps is eliminated. The preamp does not have to be a traditional dc-coupled op amp with feedback, and may be a low noise open loop GaAs "gain block". The photodiode, preamp, and the comparator are often fabricated on the same substrate in a hybrid package in order to minimize parasitics. Data transmission rates of greater than 100MHz are possible using this approach.

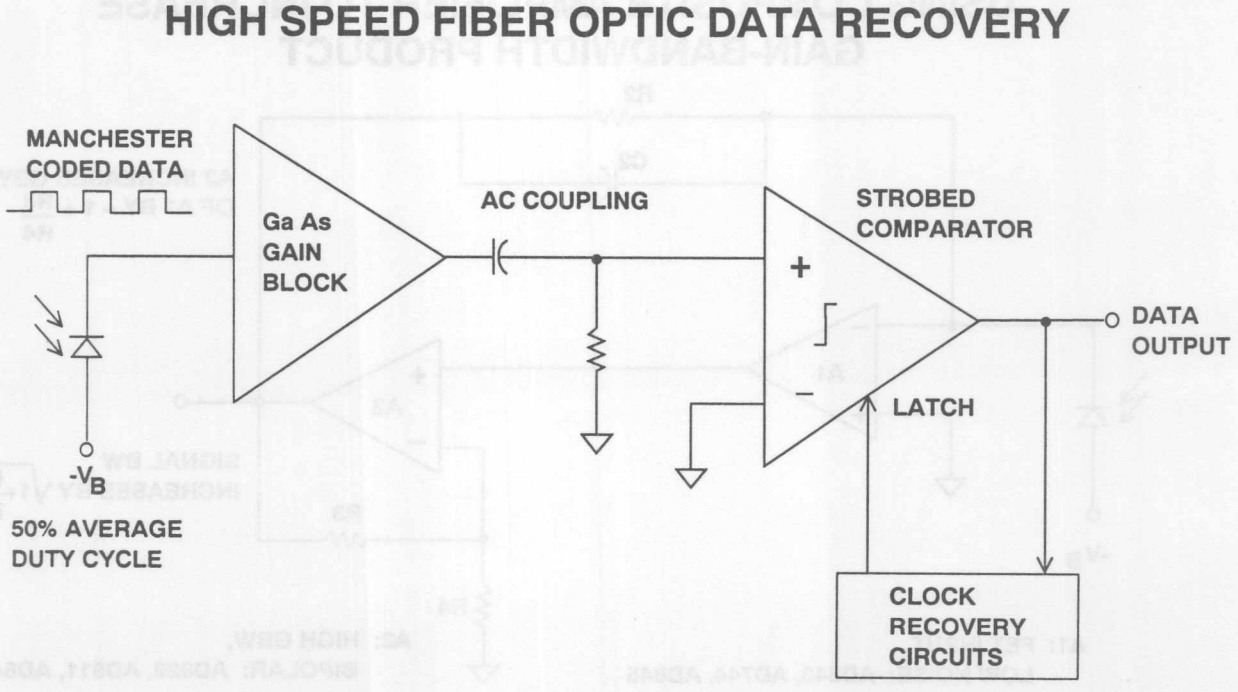


Figure 3.59

OTHER HIGH IMPEDANCE TRANSDUCER APPLICATIONS

SCOTT WURCER, CHUCK KITCHEN

A pH PROBE BUFFER AMPLIFIER

A typical pH probe requires a buffer amplifier to isolate its 10^6 to 10^9 Ω source resistance from external circuitry. Such an amplifier is shown in Figure 3.60. The low input current of the AD645 allows the voltage error produced by the bias current and electrode resistance to be minimal. The use of guarding, shielding, high insulation resistance standoffs, and other such standard picoamp methods used to minimize leakage are all needed to maintain the accuracy of this circuit.

The slope of the pH probe transfer function, 50mV per pH unit at room temperature, has a +3300ppm/°C temperature coefficient. The buffer shown in Figure 3.60. provides a gain of 20 and yields an output voltage equal to 1 volt/pH unit. Temperature compensation is provided by resistor RT which is a special temperature compensation resistor, part number Q81, 1kΩ, 1%, +3500ppm/°C, available from Tel Labs Inc.

A pH PROBE BUFFER AMPLIFIER WITH A GAIN OF 20 USING THE AD645 PRECISION OP AMP

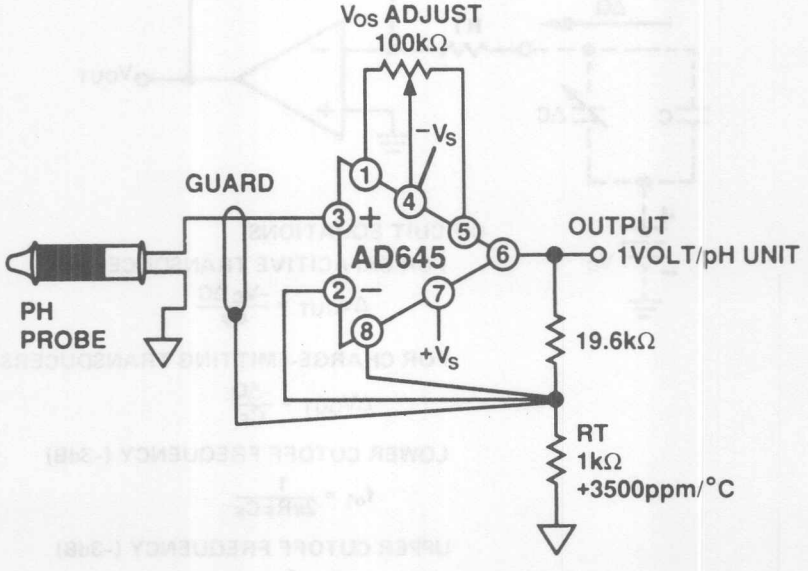


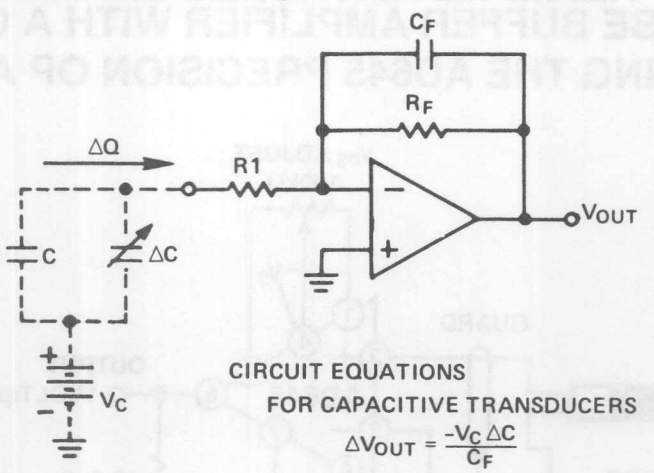
Figure 3.60

HIGH-IMPEDANCE CHARGE OUTPUT TRANSDUCERS

High impedance transducers such as hydrophones and some accelerometers require an amplifier which converts a transfer of charge into a change of voltage. Because of the high dc output impedance of these devices, appropriate buffers are required. The basic circuit for an inverting charge sensitive amplifier is shown in Figure 3.61. There are basically two types of charge transducers: capacitive and charge-emitting. In a capacitive transducer, the voltage across the capacitor (V_C) is held constant. The change in capacitance ,ΔC, produces a change in charge, $\Delta Q = \Delta CV_C$. This charge is transferred to the op amp output as a voltage, $\Delta V_{out} = -\Delta Q/C_f = \Delta CV_c/C_f$.

Charge-emitting transducers produce an output charge, ΔQ, and their output capacitance remains constant. This charge would normally produce an open-circuit output voltage at the transducer output equal to $\Delta Q/C$. However, since the voltage across the transducer is held constant by the virtual ground of the op amp (R1 is usually small), the charge is transferred to capacitor C_f producing an output voltage $\Delta V_{out} = -\Delta Q/C_f$.

CHARGE-SENSITIVE AMPLIFIER



CIRCUIT EQUATIONS

FOR CAPACITIVE TRANSDUCERS

$$\Delta V_{OUT} = \frac{-V_C \Delta C}{C_F}$$

FOR CHARGE-EMITTING TRANSDUCERS

$$\Delta V_{OUT} = \frac{-\Delta Q}{C_F}$$

LOWER CUTOFF FREQUENCY (-3dB)

$$f_{o1} = \frac{1}{2\pi R_F C_F}$$

UPPER CUTOFF FREQUENCY (-3dB)

$$f_{o2} = \frac{1}{2\pi R_1 C}$$

Figure 3.61

LOW NOISE CHARGE AMPLIFIER CIRCUIT CONFIGURATIONS

Figure 3.62 shows two ways to buffer and amplify the output of a charge output transducer. Both require using an amplifier which has a very high input impedance, such as the AD745. The AD745 provides both low voltage and low current noise. This combination makes this device particularly suitable in applications requiring very high charge sensitivity, such as capacitive accelerometers and hydrophones.

The first circuit in Figure 3.62 uses the op amp in the inverting mode. Amplification depends on the principle of conservation of charge at the inverting input of amplifier A1. The charge on capacitor C_S is transferred to capacitor C_F, thus yielding an output voltage of $\Delta Q/C_f$. The amplifier's input voltage noise will appear at the output amplified by the ac noise gain of the circuit, $1 + C_S/C_f$.

The second circuit shown in Figure 3.62 is simply a high impedance follower with gain. Here the noise gain (1 + R1/R2) is the same as the gain from the transducer to the output. Resistor R_B, in both circuits, is required as a dc bias current return.

To maximize dc performance over temperature, the source resistances should be balanced on each input of the amplifier. This is represented by the optional resistor R_B shown in Figure 3.62. For best noise performance, the source capacitance should also be balanced with the capacitor C_B. In general, it is good practice to balance the source impedances (both resistive and reactive) as seen by the inputs of a precision low noise BIFET amplifiers such as the AD743/AD745. Balancing the resistive components will

CHARGE AMPLIFIER CONFIGURATIONS

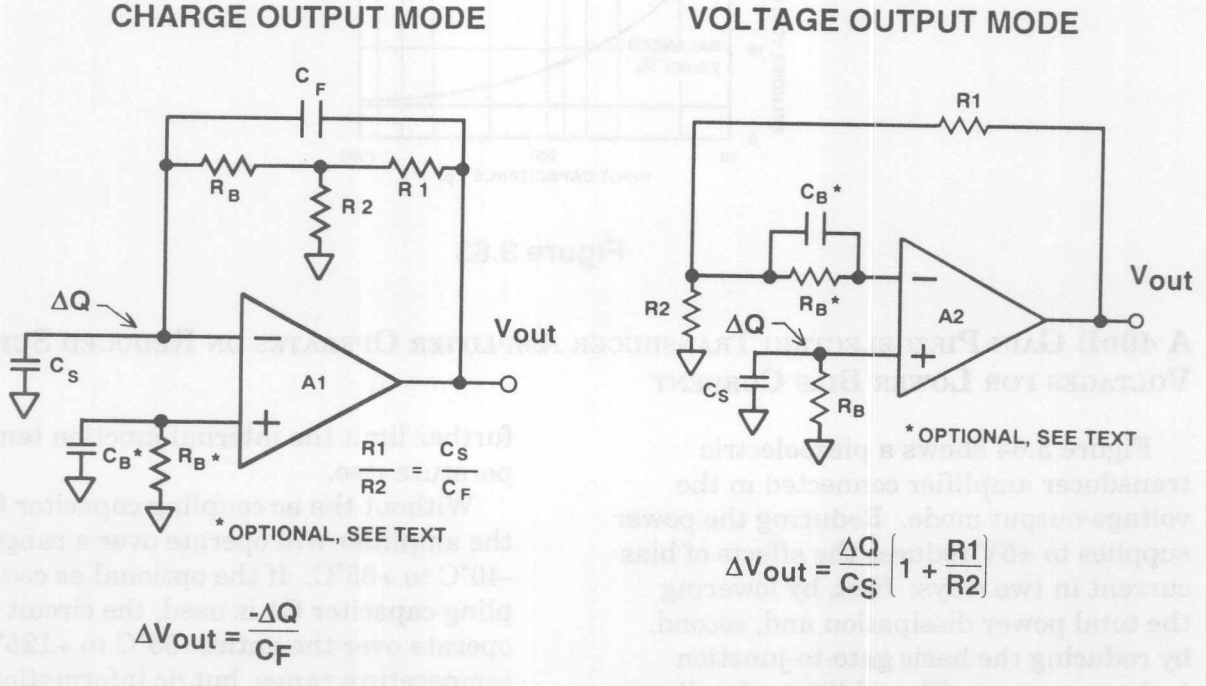


Figure 3.62

optimize dc performance over temperature because balancing will mitigate the effects of any bias current errors. Balancing the input capacitance will minimize ac response errors due to the amplifier's nonlinear common mode input capacitance, and as shown in Figure 3.63, noise performance will be optimized. Figure 3.63 shows the required external components for both inverting and noninverting configurations. For values of C_B greater than 300pF, there is a diminishing impact on noise, and C_B can then be simply a large mylar bypass capacitor of 0.01μF or greater.

BALANCING SOURCE IMPEDANCES MINIMIZES EFFECTS OF BIAS CURRENTS AND REDUCES INPUT NOISE

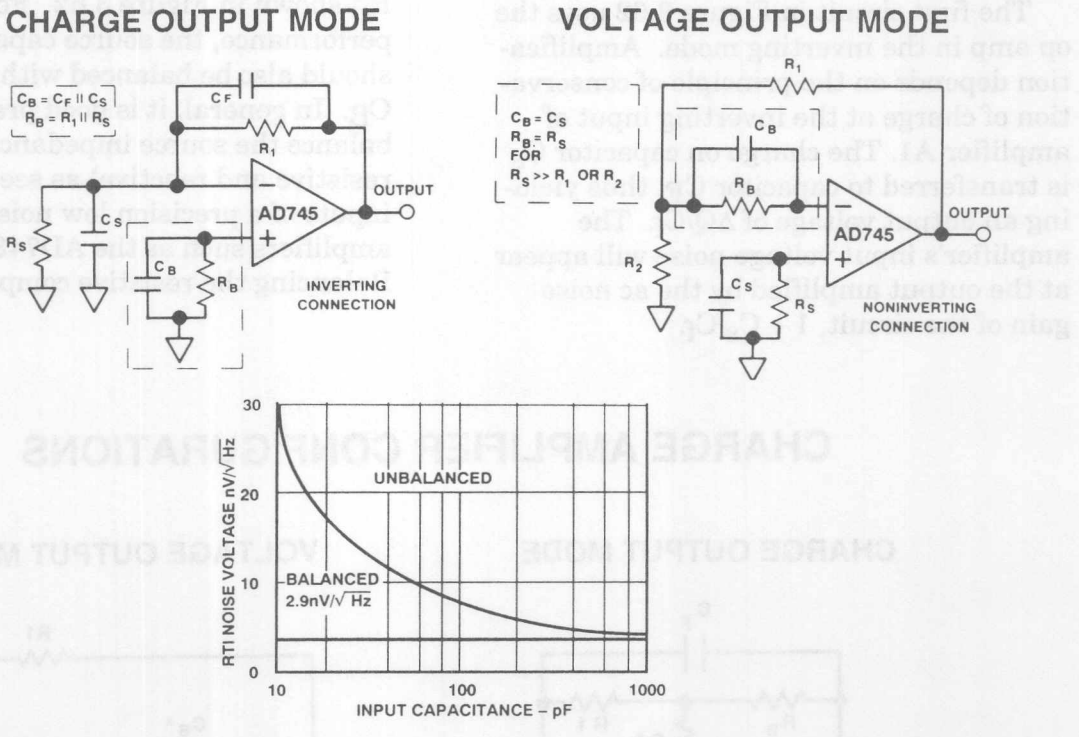


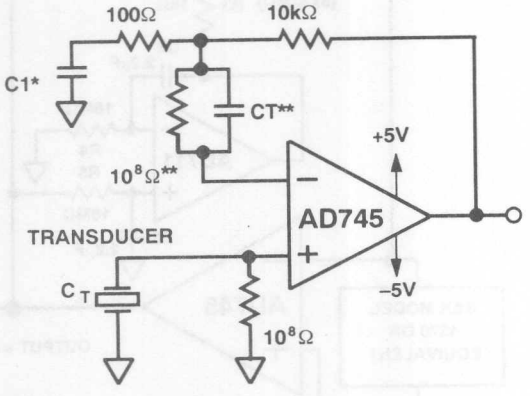
Figure 3.63

A 40dB Gain Piezoelectric Transducer Amplifier Operates on Reduced Supply Voltages for Lower Bias Current

Figure 3.64 shows a piezoelectric transducer amplifier connected in the voltage-output mode. Reducing the power supplies to ±5V reduces the effects of bias current in two ways: first, by lowering the total power dissipation and, second, by reducing the basic gate-to-junction leakage current. The addition of a clip-on heat sink such as the Aavid #5801will further limit the internal junction temperature rise.

Without the ac coupling capacitor C1, the amplifier will operate over a range of -40°C to +85°C. If the optional ac coupling capacitor C1 is used, the circuit will operate over the entire -55°C to +125°C temperature range, but dc information is lost.

A GAIN OF 100 PIEZOELECTRIC TRANSDUCER AMPLIFIER



*OPTIONAL DC BLOCKING CAPACITOR
**OPTIONAL, SEE TEXT

- ±5V Power Supplies Reduce I_b for 0°C to +85°C Operation
- C1 Allows -55°C to +125°C Operation

3

Figure 3.64

HIGH PERFORMANCE ACCELEROMETER AMPLIFIERS

Two of the most popular charge-out transducers are hydrophones and accelerometers. Precision accelerometers are typically calibrated for a charge output measured in picocoulombs (pC) per g, where g is the Earth's gravitational constant. Figure 3.65 shows two ways to configure the AD745 as a low noise charge amplifier for use with a wide variety of piezoelectric accelerometers. The output voltage, ΔV_{out} ,of these circuits will be determined by the value of capacitor, C1, and the transducer charge output ,ΔQ, or

$$\Delta V_{out} = \frac{\Delta Q}{C1}$$

HIGH PERFORMANCE ACCELEROMETER AMPLIFIERS

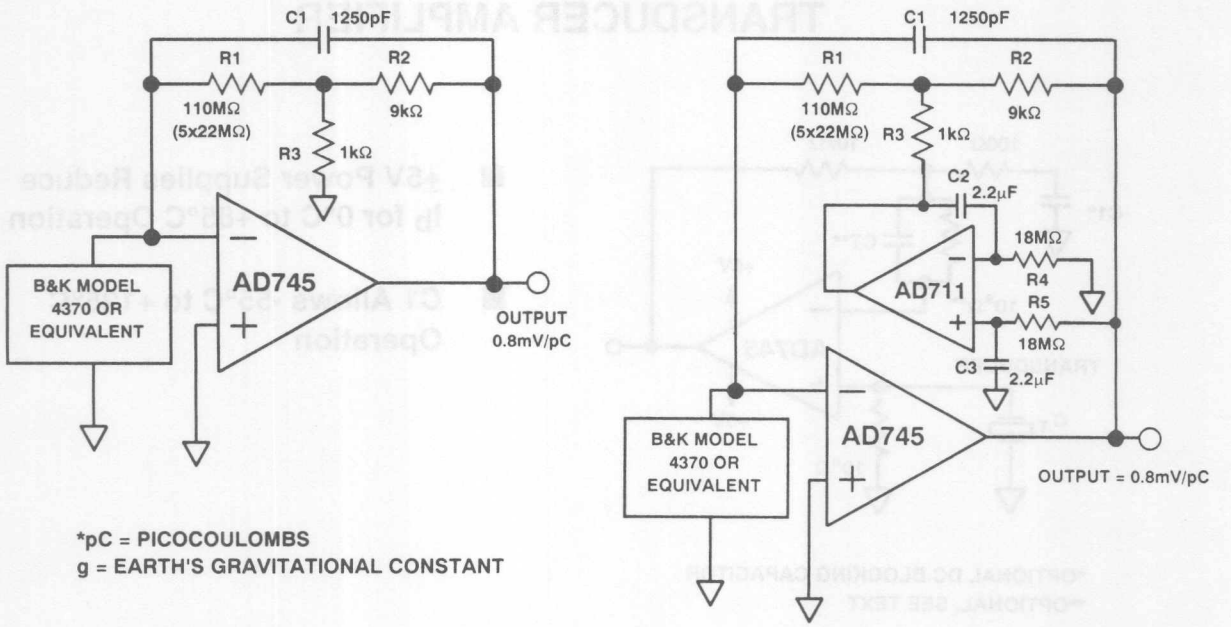


Figure 3.65

The ratio of capacitor C1 to the internal capacitance C_T of the transducer determines the ac noise gain of the circuit, $1 + C_T/C1$. The amplifier's voltage noise will appear at its output amplified by this amount. The low frequency bandwidth of these circuits will be dependent on the value of resistor R1. If a "T" network is used, the effective value is R1(1+R2/R3).

The addition of a dc servo loop as shown in Figure 3.65 can be used to assure a dc output less than 10mV without the need for a large compensating resistor when dealing with bias currents as large as 100nA. For optimal low frequency performance, the time constant of the servo loop (R4C2 = R5C3) should be:

Time Constant = R4C2 =

$$R5C3 \geq 10R1\left(1 + \frac{R2}{R3}\right)C1 .$$

HYDROPHONES

Interfacing the outputs of highly capacitive transducers such as hydrophones, some accelerometers, and condenser microphones to the outside world presents many problems. Previously designers had to use costly hybrid amplifiers consisting of discrete low-noise JFETs in front of conventional op amps to achieve the low levels of voltage and current noise required by these applications. Now, using the AD743 and AD745, designers can achieve new levels of system integration and performance.

In sonar applications, a piezo-ceramic cylinder is commonly used as the active element in the hydrophone as shown in Figure 3.66. A typical cylinder has a nominal capacitance of around 6,000pF with a series resistance of 10Ω. The output impedance is typically $10^8\Omega$ or 100MΩ

Since the hydrophone signals of interest are inherently ac in nature, noise is the overriding concern among sonar system designers. The noise floor of the hydrophone and the hydrophone preamplifier together limit the sensitivity of the system and therefore the overall usefulness of the hydrophone. Typical hydrophone bandwidths are in the 1kHz to 10kHz range. The AD743 and AD745 op amps, with their low noise figures of $2.9nV/\sqrt{Hz}$ and high input impedance of $10^{10}\Omega$ (or 10GΩ) are ideal for use as hydrophone amplifiers.

The AD743 and AD745 are companion amplifiers with different levels of internal compensation. The AD743 is internally compensated for unity gain stability. The AD745, stable for noise gains of 5 or greater, has a much higher bandwidth and slew rate. This makes the AD745 especially useful as a high-gain preamplifier where it provides both high gain and wide bandwidth. The AD743 and AD745 also operate with extremely low levels of distortion: less than 0.0003% and 0.0002% (at 1kHz), respectively.

HYDROPHONE AMPLIFIERS

Hydrophone amplifiers are usually connected in the voltage-out mode rather than charge-out mode shown in Figure 3.66. The circuits shown in Figure 3.67 can be used to amplify the output of a typical hydrophone connected in the voltage-out mode.

If the optional ac coupling capacitor, C_C, is used, the circuit on the left-hand side of Figure 3.8 will have a low frequency cutoff (F_L) :

$$F_L = \frac{1}{2\pi C_C 100\Omega} ,$$

which is determined by the time constant R_3C_C. With the ac coupling capacitor, the gain at dc is 1, and the gain above the low frequency cutoff will be a maximum of (1 + R2/R3) or 26dB.

A second type of hydrophone amplifier circuit is shown in the right-hand diagram in Figure 3.67. It uses a DC servo loop to force the dc output to 0V, within the input offset limits of the op amp, thereby maintaining full dynamic range. Power supply voltages should be reduced and heatsinking used to keep the input bias current of the AD745 below 100nA over the full military temperature range. For a smooth, low frequency response, the time constant of R7 and C1 should be at least 10x larger than that of R1 and C_T.

The transducer shown has a source capacitance of 7500pF. For smaller transducer capacitances (≤300pF), the lowest noise can be achieved by adding a parallel RC network (R4 = R1, C_T = C1) in series with the inverting input of the AD745. Balancing the source impedances (both resistive and reactive) is good practice as has been previously described.

HYDROPHONE AMPLIFIERS

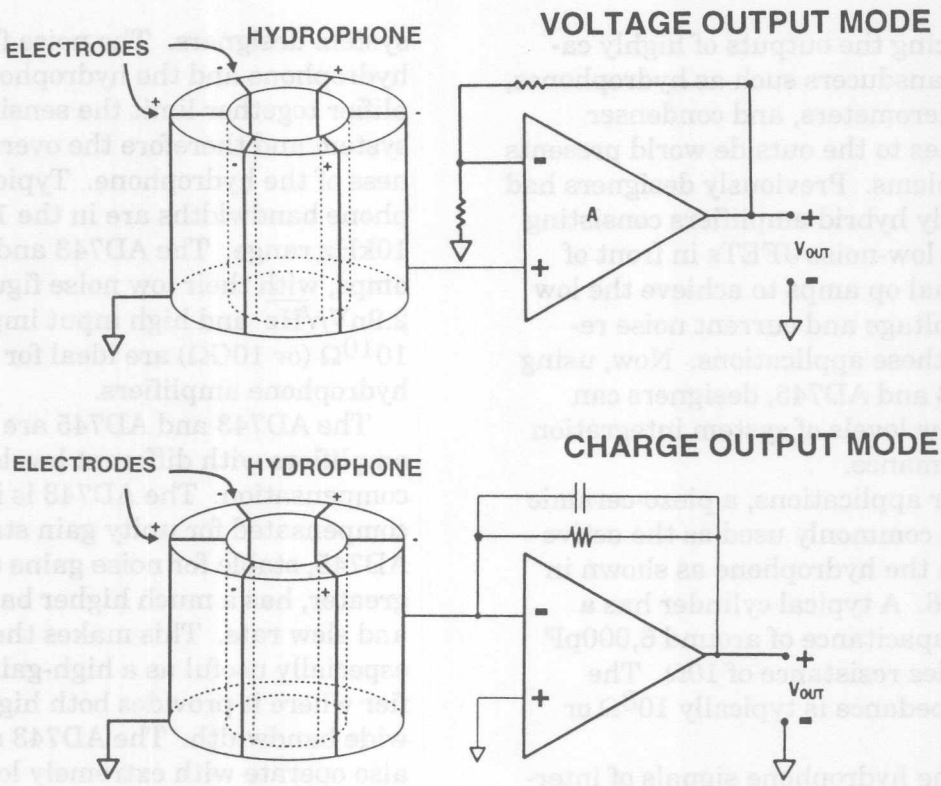


Figure 3.66

HYDROPHONE AMPLIFIER CONFIGURATIONS

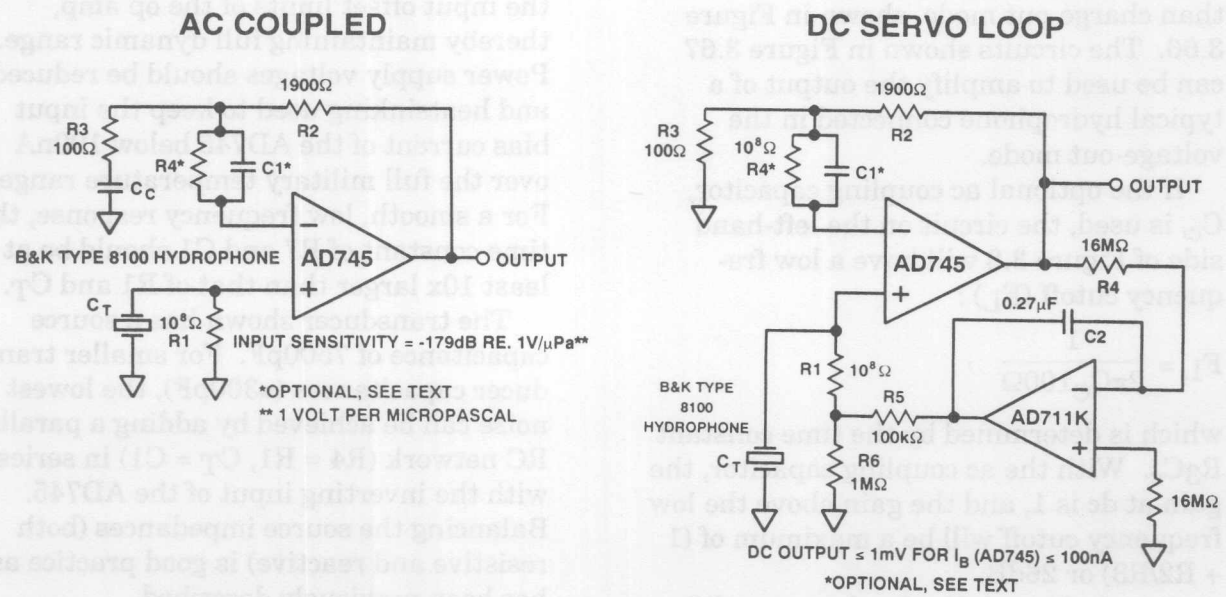


Figure 3.67

OP AMP PERFORMANCE: JFET VERSUS BIPOLAR

The AD743 and AD745 op amps are the first monolithic JFET devices to offer the low input voltage noise of an industry standard bipolar op amp without the high input bias currents typically associated with bipolar op amps. Figure 3.68 shows input voltage noise versus input source resistance of the OP-37 and the AD745 op amps. Note that the noise levels of the AD743 and the AD745 are identical. From this figure, it is clear that at high source impedances, the low current noise of the AD745 also provides total lower noise than the typical bipolar op amp. It is also important to note that, with the AD745, this noise reduction extends all the way down to low source impedances. At high source impedances, the lower dc current errors of the AD745 also reduce errors due to offset and drift as shown in Figure 3.68.

EFFECTS OF SOURCE RESISTANCE ON OUTPUT NOISE AND EFFECTIVE INPUT OFFSET VOLTAGE FOR OP-37 (BIPOLAR) AND AD745 (BiFET) OP AMPS

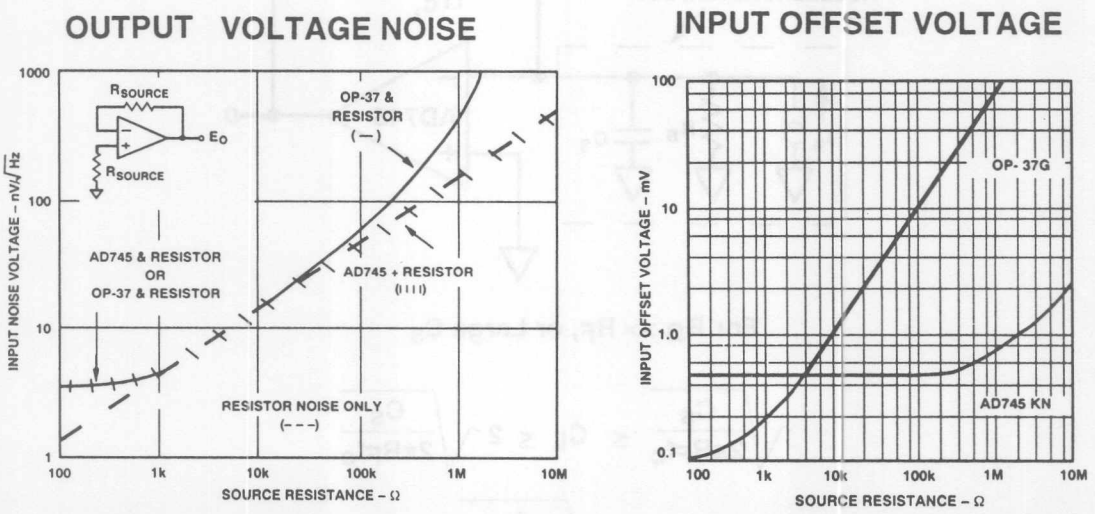


Figure 3.68

USING DECOMPENSATED AMPLIFIERS AS I/V CONVERTERS: DESIGN CONSIDERATION SUMMARY

As we have seen in the previous discussions regarding high speed photodiode preamps, there are some simple rules of thumb when designing an I/V converter where there is significant source capacitance and the bandwidth needs to be optimized. The basic circuit is shown in Figure 3.69. The high frequency noise gain ($1 + C_S/C_L$) is usually greater than 5, so a decompensated amplifier such as the AD745 with its higher slew rate and bandwidth is ideally suited to this application.

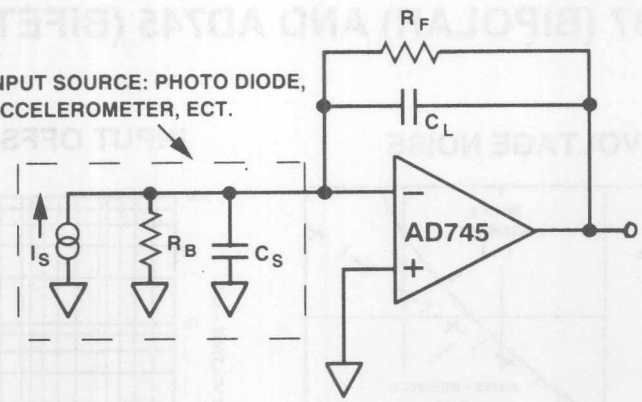
Here both the low current and low voltage noise of the AD745 can be taken advantage of, since it is desirable in some instances to have a large R_F (which increases sensitivity to input current noise) and , at the same time, operate the amplifier at high noise gain.

In Figure 3.69, the time constant $R_F C_S$ limits the practical bandwidth over which flat response can be obtained. The maximum signal bandwidth obtainable is given by the geometric mean of $1/2\pi R_F C_S$ and the op amp unity gain bandwidth produce f_C:

$$f_{max} = \sqrt{\frac{f_c}{2\pi R_F C_S}}.$$

The proper selection of the value of the stabilization capacitor, C_L, is critical to the performance of the circuit. If R_B and R_F are of the same order of magnitude, C_L is chosen such that $R_F C_L = R_B C_S$. If, however, the source is largely capacitive, and $R_B >> R_F$, then the optimum value of C_L is chosen in a different manner.

GENERALIZED CURRENT-TO-VOLTAGE CONVERTER



For $R_B >> R_F$, or Large C_S

$$\sqrt{\frac{C_S}{2\pi R_F f_C}} \leq C_L \leq 2\sqrt{\frac{C_S}{2\pi R_F f_C}}$$

$$f_{max} = \sqrt{\frac{f_C}{2\pi R_F C_S}}$$

$$\frac{f_{max}}{2} \leq f_{3dB} \leq f_{max}$$

Figure 3.69

For the case of a high impedance source, C_L should be chosen such that the phase margin of the two-pole circuit is between is between 45° and 65°, or

$$\sqrt{\frac{C_S}{2\pi R_F f_c}} \leq C_L \leq 2\sqrt{\frac{C_S}{2\pi R_F f_c}} .$$

Optimizing the value of C_L within this range will result in a signal bandwidth between f_{max} and $f_{max}/2$ for the two-pole system. The actual value should be chosen in the circuit by adjusting C_L to provide the best tradeoff between frequency and pulse response.

A HIGH PERFORMANCE AUDIO I/V CONVERTER USING THE AD745

This principle can also be used to apply the AD745 in a high performance audio application. Figure 3.70 shows that an I/V converter of a high performance DAC, here the AD1862, can be designed to take advantage of the low voltage noise of the AD745 (2.9nV/ as well as the high slew rate and bandwidth provided by decompensation. This circuit, with component values shown, has a 3dB bandwidth of 531kHz, with a passband ripple of less than 0.001dB and a phase deviation of less than 2 degrees at 20kHz. The feedback capacitor value is initially chosen using the formulas in Figure 3.69, which indicate a value between 72pF and 144pF. The final circuit value of 100pF was selected by optimizing the actual circuit performance. An important feature of this circuit is that high frequency energy, such as clock feedthrough, is shunted to ground via a high quality 2000pF capacitor and not the output stage of the amplifier, thereby greatly reducing the error signal at the input of the amplifier and subsequent opportunities for intermodulation distortion.

HIGH PERFORMANCE AUDIO DAC CURRENT-TO-VOLTAGE CONVERTER USING AD745

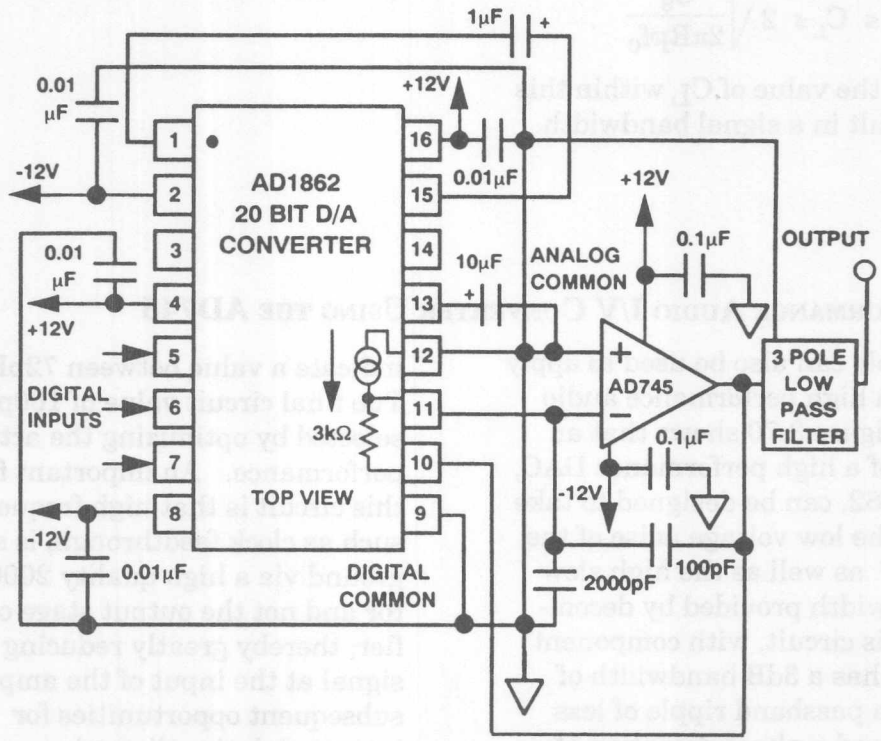


Figure 3.70

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SECTION IV

SINGLE SUPPLY, LOW POWER APPLICATIONS

- Single Supply Design Considerations:
  Reduced SNR, Determining the Ground Reference, Zero-Volt Input Signals, Zero-Volt Output Signals
- Application Example: Designing a True Single Supply Instrumentation Amplifier
- Other Limitations of Zero-Volt Output Amplifiers
- Rail-to Rail Output Swing Op Amp
- Choosing Single Supply Op Amps
- Using Precision Op Amps in Single-Supply, Low Voltage Applications
- Noise Pickup and Logic Supplies

SECTION IV

SINGLE SUPPLY, LOW POWER APPLICATIONS

JAMES WONG

SINGLE SUPPLY DESIGN CONSIDERATIONS

Single supply operation is becoming an increasingly important requirement as systems get smaller, cheaper, and more portable. Portable systems rely on a battery as the primary power source. Consequently power consumption and therefore operating time per battery charge are high on the designers' priority list. This makes low voltage operation and low power consumption critical.

However, most op amps are designed to operate with ±15V supplies. Trying to make them work at low voltages may require special attention because few are specified to operate at lower voltages. Many will not even function at 5V or less. Thus the choice of devices narrows rapidly as the supply voltage is reduced.

The +12V supply is popular because of the ubiquitous automobile battery and its wide range of size and capacity. Even more popular is the +5V supply voltage that powers virtually all TTL or CMOS logic based systems. There are also special applications that run on one or two 1.5V cells. The lower the supply voltage, the more difficult the circuit design task becomes: the signal range gets compressed, and fewer components are able to operate.

SINGLE SUPPLY DESIGN CONSIDERATIONS

- Low Signal Swing Compresses Signal-To-Noise Performance
- Noise Floor Tends To Rise at Low Currents
- Choosing "Ground Reference" Important
- Fewer Precision Op Amp Choices Available
- Bandwidth Suffers As Supply Current Drops
- Limitations of Zero-Volt Output Amplifiers
- Noise Pickup from Logic Supplies
- Tradeoffs to Achieve Desired Performance May Be Necessary

Figure 4.1

Besides these limitations, many design considerations that otherwise are minor issues suddenly become important. For example, signal-to-noise (SNR) performance degrades as a result of swing limitation. "Ground reference" is no longer a simple choice, as one reference voltage may work for some devices, but not others. System noise usually increases dramatically as operating current drops and bandwidth decreases. Therefore, achieving adequate bandwidth and required precision with a somewhat limited selection of amplifiers presents significant design challenges in single-supply, low power applications. The following sections discuss each of these issues.

REDUCED SIGNAL-TO-NOISE PERFORMANCE

The most immediate effect on an amplifier circuit when operating with a single supply at a reduced voltage is the reduction in signal swing. Even if the noise floor remains constant (highly unlikely), the signal-to-noise performance will drop as the signal amplitude decreases.

Most op amps that are designed to operate from ±15V usually do not have problems with output headroom: 3V to 4V is sufficient for most applications. However, if the supply voltages drop to, say +12V, a 3V headroom requirement (at each rail) would limit the signal swing to 6Vp-p (from +3V to +9V). Dropping the voltage further to +5V will render these op amps inoperable, as there is no output swing capability left.

For this reason and others, low voltage single supply op amps are designed so that their output stage is designed to swing as close to both rails as possible. This helps to restore some of the lost SNR performance. It is useful if the output can swing to the negative rail. Many op amps do have this capability. More on this subject in the next sections. On the positive rail side, most single supply op amps still require 1V to 2V of headroom because of junction voltages and biasing circuits. Others require even less by designing the output stage such that there are no junction voltages to limit headroom. Thus a 3V to 4V or more swing is possible for a 5V supply. The drawback is that most of these op amps are not designed to source much output current, usually 5mA maximum.

Besides being compressed at high levels end by signal reduction, SNR performance is generally squeezed from the bottom end as well as noise floor tends to rise. This is because single supply usually accompanies an inevitable drive toward lower supply current consumption, which tends to increase noise up.

The designer must decide how these issues affect the final performance target of the system and make the necessary tradeoffs.

WHERE IS "GROUND"?

Most of us take "ground" reference for granted. Most analog circuits scale their input and output ranges about a ground reference. For ±15V supply operation, a reference that splits the supplies is very convenient, as there is ample supply headroom to work with. Indeed, being a de facto standard also helps ease the choice.

Such is not the case for single supply circuits. Ground reference can be chosen anywhere within the supply range of the circuit. There is no standard to follow. Indeed, the choice of ground reference depends on the type of signals used. To illustrate the point, choosing the negative rail as the ground reference may optimize the signal dynamic range of an op amp

that is designed to swing to zero volts. On the other hand, the signal may have to be level shifted in order to be compatible with another device that is not designed to operate at 0V input because the signal can no longer be inverted. These limitations can force an inefficient design, thus increasing the cost of the system.

It is prudent to sit back and think through the design requirements, roughly sketch out the circuit configurations of various stages that fit together, and get an idea of what devices might be used before deciding on the ground reference.

CHOOSING THE NEGATIVE RAIL AS THE GROUND REFERENCE

This is the simplest and the most natural choice for setting the ground reference. Since the negative rail is the return of the supply, its impedance is very low and it makes an ideal ground reference. All signals can be returned to this point without the concern about its ability to sink the current - assuming the current is within the rated capability of the supply. Nevertheless the voltage drop in negative rail ground returns can be a problem, and their resistance must be kept low.

Setting ground reference at the negative rail usually allows the maximum signal dynamic range, as it establishes the limit of one end of the signal range. However, this may present a problem interfacing with other devices as their inputs or outputs are not designed to operate near the negative rail. Therefore it is important to know what type of devices are needed for the application, knowing that the signal will swing to the negative rail.

AN ISOLATED DIGITALLY PROGRAMMABLE, LOOP-POWERED 4-TO-20mA PROCESS CONTROLLER

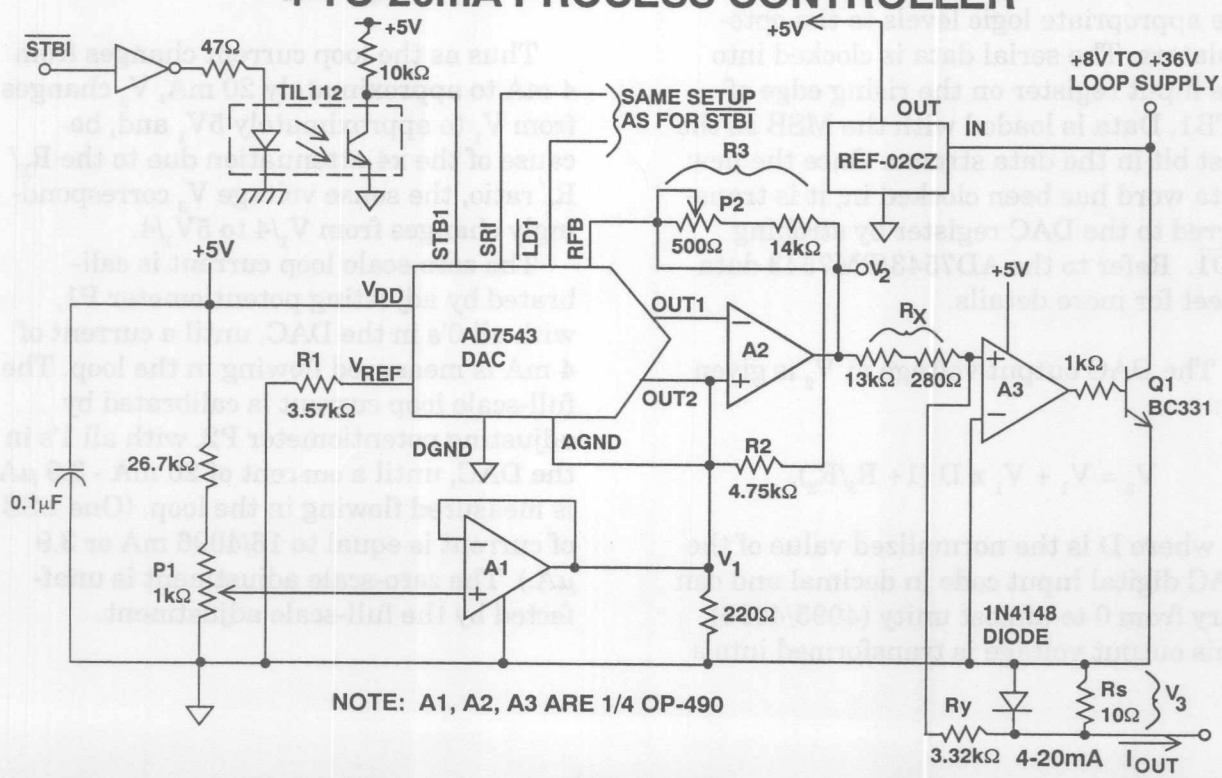


Figure 4.2

Quite often a non-single supply device can be made to operate in a single supply environment. For example, Figure 4.2 shows a CMOS DAC operating with a single supply in a loop-powered 4-to-20mA process control application. Note that while the op amp uses the negative rail as the reference voltage, the DAC is biased up from the negative rail with a separate reference voltage V_1. This allows a non-single supply device to interface properly with a single supply op amp.

Power for the controller circuit is derived from the loop supply, which can range from +8V to +36V. Since the controller is intended to be isolated, all control signals must be opto-isolated before being applied to the DAC. To limit the power and the number of isolators and components, a serial input loading DAC is preferable.

The AD7543/PM7543 is a 12-bit DAC that can be loaded and controlled with only three lines, STB1, SRI and $\overline{\text{LD1}}$. Since the opto-isolators act as signal inverters, the microcontroller, PC, or whatever is supplying the control signals must take this into account and generate the appropriate logic levels to the opto-isolators. The serial data is clocked into the input register on the rising edge of STB1. Data is loaded with the MSB as the first bit in the data stream. Once the new data word has been clocked in, it is transferred to the DAC register by strobing $\overline{\text{LD1}}$. Refer to the AD7543/PM7543 data sheet for more details.

The DAC output voltage at V_2 is given by:

$$V_2 = V_1 + V_1 \times D\ (1 + R_3/R_2).$$

where D is the normalized value of the DAC digital input code in decimal and can vary from 0 to almost unity (4095/4096). This output voltage is transformed into a loop current by means of A3 and Q1. Amplifier A3 drives the NPN transistor Q1, configured as an emitter follower in the feedback loop, to maintain a current necessary to keep the voltage V_3 across R_S, the sense resistor, equal to the voltage across R_Y, the feedback resistor. Since the ratio of R_X to R_Y is 4 so the ratio of voltages across R_X and R_Y must be the same, i.e. $V_3 = V_2/4$.

Thus V_3, and ultimately the loop current, follows the DAC output voltage V_2. In order to operate from low loop voltages, the voltage V_3 should be as small as practical. With the 10 Ω used for R_S in Figure 4.2, V_3 varies from approximately 40 mV (at 4 mA loop current) to approximately 200 mV (at 20 mA loop current).

From the above equation, with all 0's in the DAC,

$$V_2 = V_1,$$

and with all 1's in the DAC and $(1 + R_3/R_2) = 4$,

$$V_2 \sim 5V_1.$$

Thus as the loop current changes from 4 mA to approximately 20 mA, V_2 changes from V_1 to approximately $5V_1$ and, because of the x4 attenuation due to the R_X/R_Y ratio, the sense voltage V_3 correspondingly changes from $V_1/4$ to $5V_1/4$.

The zero-scale loop current is calibrated by adjusting potentiometer P1, with all 0's in the DAC, until a current of 4 mA is measured flowing in the loop. The full-scale loop current is calibrated by adjusting potentiometer P2, with all 1's in the DAC, until a current of 20 mA - 3.9 μA is measured flowing in the loop. (One LSB of current is equal to 16/4096 mA or 3.9 μA.) The zero-scale adjustment is unaffected by the full-scale adjustment.

Resistor R_1 is chosen to be equal to the parallel combination of resistors R_2 and R_3. This avoids the absolute value of the DAC ladder resistance, which may vary from device to device, from appearing in the output expression for V_2 (assuming $R_{FB} = R_{ladder}$, i.e. , no DAC gain error). Ideally resistors R_1, R_2, and R_3 should be the same type and from the same manufacturer to ensure that their TCs match and track each other. However since it is necessary to provide full-scale adjustment, R_3 consists of a fixed 14 kΩ metal film resistor and a 500 Ω 10-turn potentiometer P2. Although the TCs of the potentiometer and the metal film resistor will almost certainly not match, the additional drift will not be significant since the TC of the much larger fixed resistor will dominate.

The 220 Ω resistor on the output of A1 acts as a pull-down resistor and helps to keep the voltage V_1 constant as the DAC's digital input code changes.

The actual loop current that flows is given by:

$$I_{OUT} = V_3 (1/R_S + 1/R_Y)$$

R_S is set at 10 Ω and R_Y is set at 3 kΩ. With 4 mA flowing (I_{OUT} = 4 mA), using the above equation we see that V_3 = 39.867 mV (V_2 = 159.468mV). Similarly, $V_2 = V_1$ at the all-0's code. This voltage, as mentioned above, is set by P1.

At full-scale (I_{OUT} = 30 mA - 3.9 μA), using the above output current equation, we see that V_3 = 199.336 mV (V_2 = 797.344 mV). This voltage is set by P2.

The diode across R_S serves to clamp the voltage to 0.6V such that it limits the loop current to no more than 60 mA during power-on, where transient voltages may be present on the base of Q1. When this condition occurs, Q1 can momentarily turn on and cause excessive current to flow through R_S. If a sufficiently large voltage drop develops across R_S, the non-inverting input of amplifier A3 may pull 0.6V more negative than the inverting input (negative rail). This may cause A3's output to invert its phase (goes positive) which keeps Q1 on, causing a positive feedback circuit lock-up. The diode clamp prevents this condition from occurring. If a smaller current limit is required, a low-leakage Schottky diode may be used in place of the silicon diode.

4

USING A FALSE-GROUND REFERENCE

Not all single supply circuits work well with the 0V ground system. For example, audio signals or video signals may be best handled using a false-ground system by biasing the amplifiers to the mid-point of the supply. Then the signal can be AC coupled through the amplifier chain. This removes the necessity of level shifting at each amplifier stage as would otherwise be required if the 0V ground system is used. It also saves the cost of additional components to do level shifting.

It is often assumed that a false-ground circuit need only be a simple buffer amplifier without the bypass capacitors and compensation. In some cases, one can get by without them as long as the false-ground node does not see any dynamic or transient load changes. These can occur when driving the ground pin of a D-A or an A-D converter. In these applications, the false-ground node must hold its voltage constant with minimum perturbation. If reference "bounce" is present, conversion error may result, or noise may be injected into the circuit.

The choice of the quality of the false-ground rests on whether the circuit is sensitive to the false-ground perturbation, both in DC and AC terms. Not all applica-

tions necessarily require a high-quality, low impedance false ground. In fact, in some cases, it may be sensible to use both false-ground as well as negative rail ground references in different parts of the circuit. One needs to observe the level shifting requirement when interfacing the two. It depends on what works best.

A solid false-ground can be easily implemented using a voltage divider or a reference voltage buffered by an amplifier. The choice of the op amp and the implementation is critical to a good reference node without reference "bounce". An example is shown in Figure 4.3.

These circuits have elaborate compensations to allow for heavy capacitive bypasses at the false-ground output. The benefit of a big capacitor is that not only does the false-ground present a very low DC resistance to the load, its AC impedance is low as well. The capacitor serves as a "charge reservoir" to absorb any momentary load current surges, thus minimizes reference "bounce". A reasonably fast settling op amp also helps to replenish the discharge quickly for rapid recoveries from disturbances.

Proper recovery requires the op amp to have sufficient output current sinking as well as sourcing capabilities. Furthermore, the amplifier's output current level should not operate close to the current limit point as a surge of current can easily push it over the limit. Undesirably long recovery will result.

SUPPLY SPLITTER REFERENCE GENERATORS

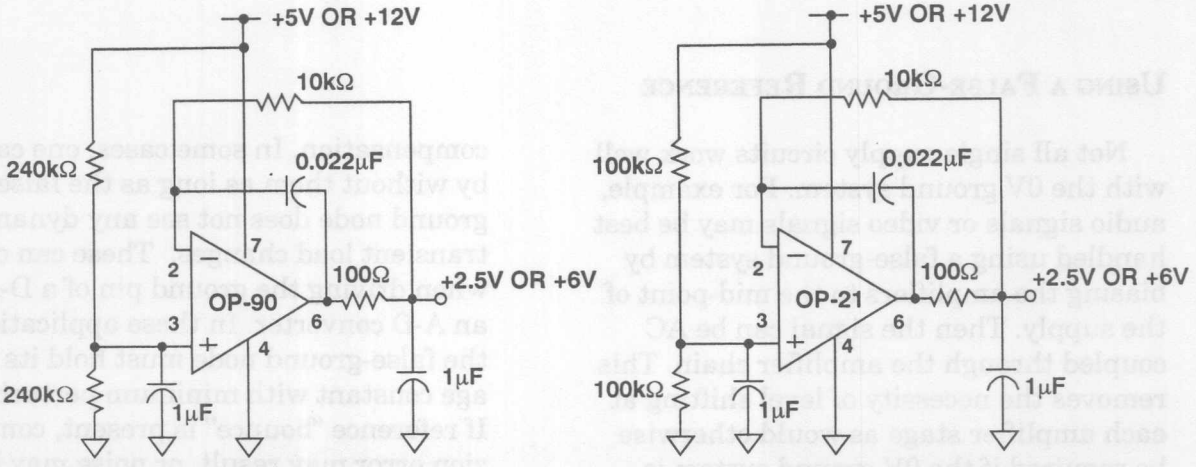


Figure 4.3

A 50/60Hz NOTCH FILTER USES FALSE-GROUND

To process AC signals, it can be easier to use false-ground bias. A 50/60Hz notch filter for eliminating line noise in a patient monitoring equipment having several kilohertz bandwidth may not be sensitive to false-ground perturbations. Such an application might use a simple false-ground circuit as shown in Figure 4.4 that biases the amplifiers to the midpoint of a +12V supply. This notch filter achieves nearly 40dB rejection of 60Hz pickup at a Q of 0.75. To reject 50Hz frequency, simply change the resistors in the twin-T section (R1 through R5) from 2.67kΩ to 3.16kΩ.

This circuit helps reject 50Hz or 60Hz power line frequency pick-up that tends to obscure low frequency physiological signals, such as heart rates, blood pressures, EEGs, ECG, etc. The notch filter achieves almost 40dB (at a Q=0.75) of rejection using standard off-the-shelf components.

The filter uses a pair of the OP-482's quad op amps in a twin-T configuration whose frequency selectivity is very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Mylar is a good choice for the twin-T's capacitors, and the relative matching of the capacitors and resistors determines the filter's passband symmetry. Using 1% resistors and 5% capacitors produced satisfactory results.

The amount of rejection and the Q of the filter is solely determined by one resistor, and is as shown in Figure 4.5. For example, at a Q=1, the filter measured 35dB rejection of 60Hz noise. Additional rejection beyond 40dB at 60Hz can be achieved by cascading identical filter sections.

The third of the OP-482 amplifier, A3, buffers the supply splitter to create a false-ground reference voltage at +6V. No special output bypassing is necessary to

4

A 50/60 Hz SINGLE-SUPPLY NOTCH FILTER

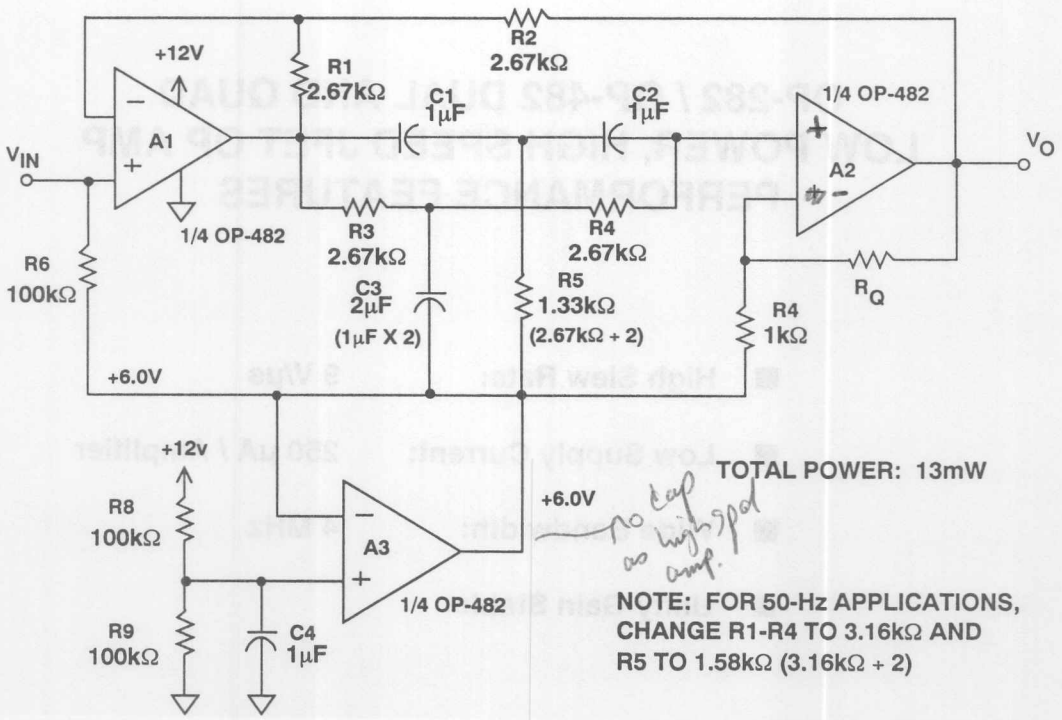


Figure 4.4

RQ, REJECTION AT 60 Hz, AND FILTER'S VOLTAGE GAIN AS A FUNCTION OF THE FILTER Q

Filter Q	RQ (kΩ)	Rejection (dB)	Voltage Gain
0.75	1.0	40	1.33
1.00	2.0	35	1.50
1.25	3.0	30	1.60
2.50	8.0	25	1.80
5.00	18	20	1.90
10.0	38	15	1.95

Figure 4.5.

OP-282 / OP-482 DUAL AND QUAD LOW POWER, HIGH SPEED JFET OP AMP PERFORMANCE FEATURES

- **High Slew Rate:** 9 V/μs
- **Low Supply Current:** 250 μA / Amplifier
- **Wide Bandwidth:** 4 MHz
- **Unity Gain Stable**

Figure 4.6

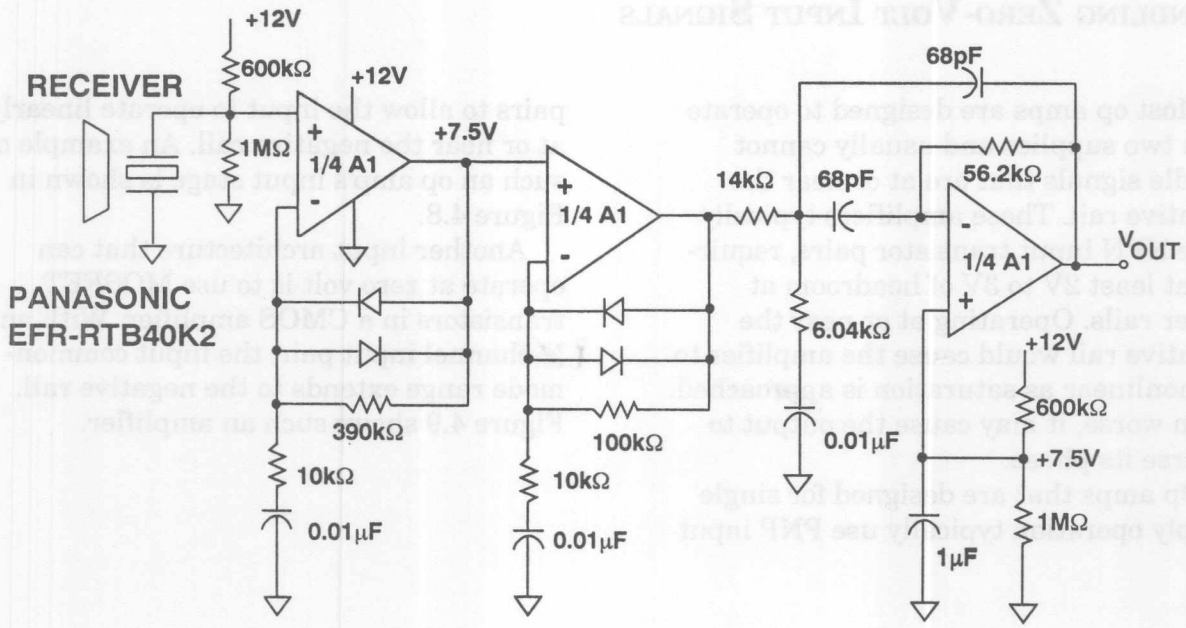
improve the quality of the false ground as the op amp buffer has more than sufficient bandwidth and fast settling characteristics that are well beyond the signal bandwidth.

The OP-482 is chosen because it can pass signals more than 1 MHz at a Q of 1 while consuming a relatively low power of 13 mW, making it suitable for battery operated or portable medical instrumentation. In addition, the OP-482's FET input has low current noise that interfaces well with the high impedance of ECG and EEG probes. Some OP-482's features are shown in Figure 4.6.

AN ULTRASONIC CLAMPING RECEIVER USING A FALSE GROUND REFERENCE

Another application example where it makes sense to use false ground reference is an ultrasonic sensor amplifier as shown in Figure 4.7 where simple diode feedback provides crude but effective gain control for wide dynamic signal range.

A 40kHz ULTRASONIC CLAMPING/LIMITING RECEIVER



NOTE: A1 IS OP-482
DIODES ARE IN914

Figure 4.7

This circuit amplifies a 40kHz ultrasonic wave signal through a pair of low-cost clamping amplifiers before feeding a bandpass filter to extract a clean 40kHz signal for processing. The ultra-sound signal is AC-coupled into the false-ground bias node by virtue of the capacitive piezoelectric sensing element. Rather than using a supply splitter (1/2 the supply voltage) bias, the false-ground is set at 7.5V, which is halfway between the input and output range of the op amp to get the maximum signal swing. The 600 kΩ and the 1 MΩ divider provides the bias.

Each amplifier stage provides AC gain while passing on the DC self-bias. As long as the output signal at each stage is less than a diode's forward voltage, each amplifier has unrestricted gain to amplify low level signals. However, as the signal strength increases, the feedback diodes begin to conduct, shunting the feedback current, and thus reducing the gain. Although distorting the waveform, the diodes effectively maintain a relatively constant amplitude even with large signals that otherwise would saturate the amplifier. In addition, the this design is considerably more stable than feedback type AGC.

The overall circuit has a gain range from -2 to -400, where the inversion comes from the bandpass filter stage. Operating with a Q of 5, the filter restores a clean, undistorted signal to the output. Total supply current draws 1 mA maximum for the entire circuit making battery operation feasible.

HANDLING ZERO-VOLT INPUT SIGNALS

Most op amps are designed to operate with two supplies and usually cannot handle signals that are at or near the negative rail. These amplifiers typically have NPN input transistor pairs, requiring at least 2V to 3V of headroom at either rails. Operating at or near the negative rail would cause the amplifier to go nonlinear as saturation is approached. Even worse, it may cause the output to reverse its phase.

Op amps that are designed for single supply operation typically use PNP input pairs to allow the input to operate linearly at or near the negative rail. An example of such an op amp's input stage is shown in Figure 4.8.

Another input architecture that can operate at zero volt is to use MOSFET transistors in a CMOS amplifier. With an N-channel input pair, the input common-mode range extends to the negative rail. Figure 4.9 shows such an amplifier.

OP-90 PNP INPUT STAGE DESIGN ALLOWS ZERO-VOLT INPUT OPERATION

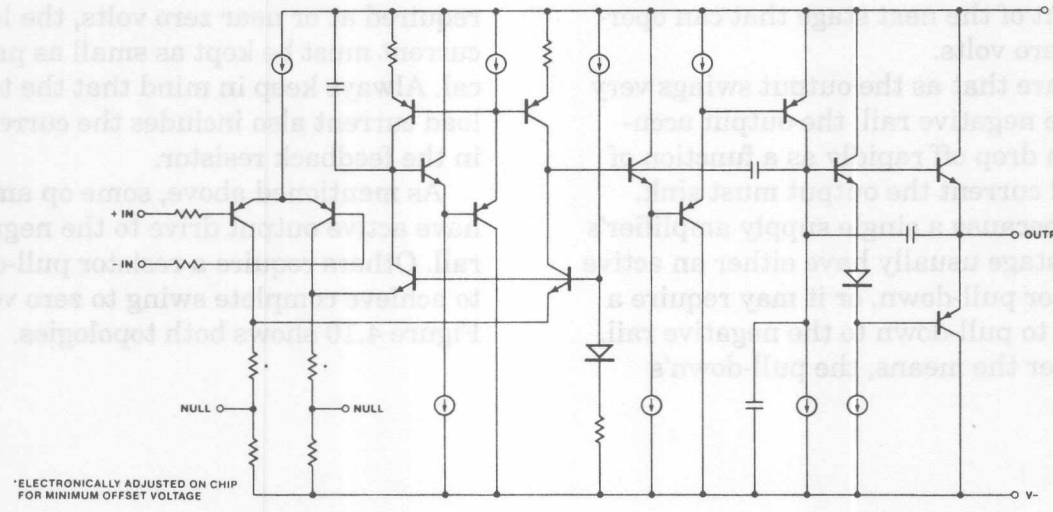


Figure 4.8

OP-80 CMOS OP AMP ALLOWS ZERO VOLT INPUT OPERATION

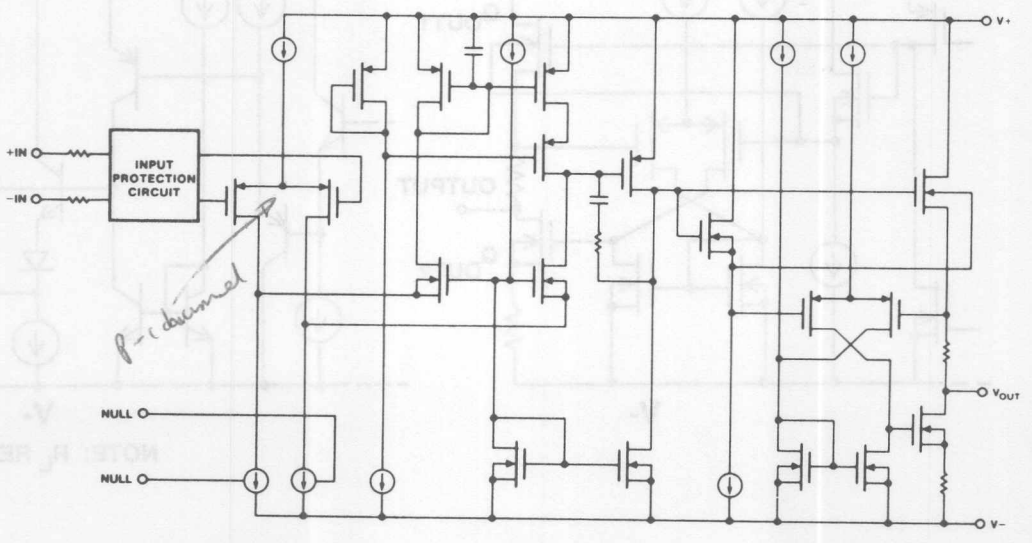


Figure 4.9

HANDLING ZERO-VOLT OUTPUT SIGNALS

Ideally a single supply op amp's output should be capable of swinging to the negative rail, especially if it is feeding into the input of the next stage that can operate at zero volts.

Beware that as the output swings very near the negative rail, the output accuracy can drop off rapidly as a function of the load current the output must sink. This is because a single supply amplifier's output stage usually have either an active transistor pull-down, or it may require a resistor to pull-down to the negative rail. Whatever the means, the pull-down's finite resistance develops a voltage drop that prevents the output from swinging fully to the negative rail. If accuracy is required at or near zero volts, the load current must be kept as small as practical. Always keep in mind that the total load current also includes the current flow in the feedback resistor.

As mentioned above, some op amps have active output drive to the negative rail. Others require a resistor pull-down to achieve complete swing to zero volt. Figure 4.10 shows both topologies.

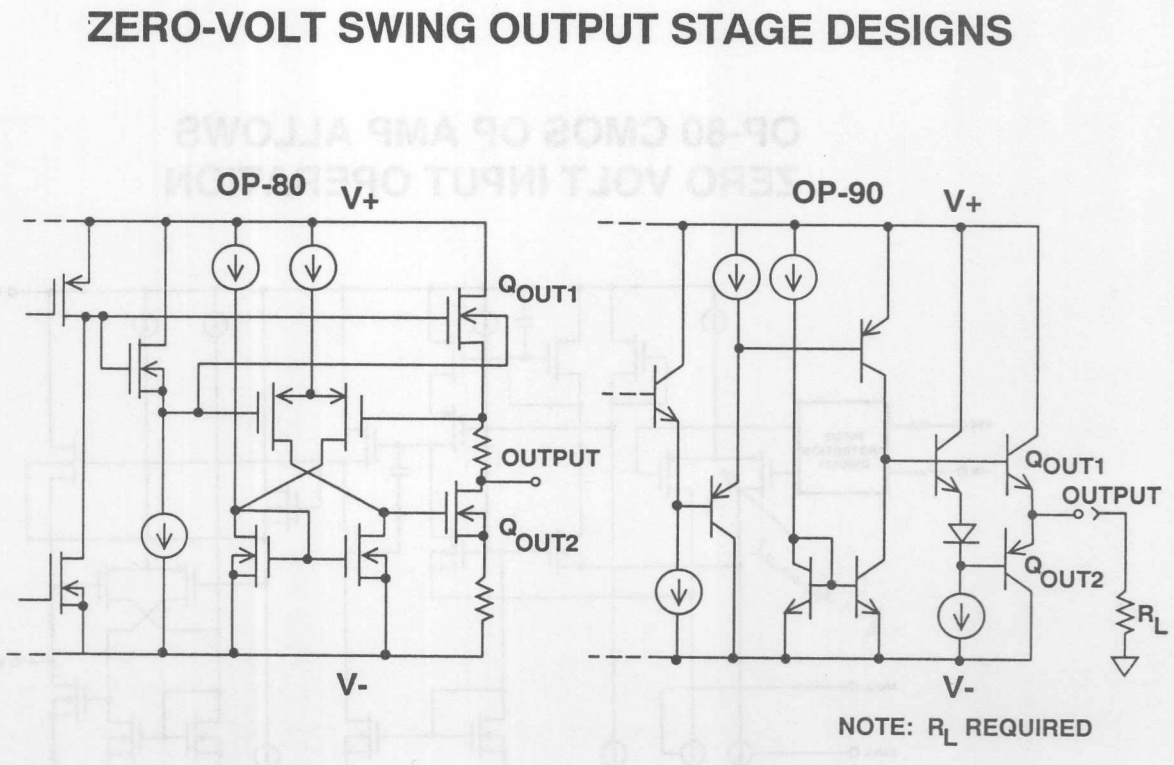


Figure 4.10

Figure 4.10(a)'s OP-80 output stage relies on the Q_{OUT2}'s internal ON-resistance to pull the output down to the negative rail. Including a source resistance, the total pull-down resistance is typically 400 Ω. As long as the load currents is less than 1 μA, its output will swing to within 1mV of the negative rail.

The OP-90 utilizes a conventional push-pull emitter-follower output stage as shown in Figure 4.8(b). It provides low impedance drive except for output voltages less than 0.5V to the negative rail. Below this voltage, the bottom output transistor Q_{OUT2} saturates, clamping the output at a base-emitter voltage above the negative rail. If no external pull-down resistor is provided, the top output transistor Q_{OUT1} turns off completely as its base voltage tends to pull less than its base-emitter voltage, cutting off the base drive. However, a pull-down resistor would keep the Q_{OUT1} active, and therefore linear operation continues as the output swings to the negative rail.

THE KEY IS ZERO-VOLT SWING WITH LINEARITY

It is not sufficient for a single supply amplifier to just swing to zero volts. Accuracy can only be assured if its linearity does not drop off significantly, at least to within millivolts to the rail. The best way is to measure an amplifier's linearity as its output swings to the negative rail using a circuit as that in Figure 4.11.

A small amount of nonlinearity, such as a "bowing" or an irregular "S" shape may not be significant enough to cause concern. However, if the curve shows a radical discontinuity or exhibits a large "glitch", that may be an indication that the amplifier is not suited to operate at or near the negative rail. The designer must determine whether such behavior is acceptable in the application.

A good measurement should look something like that in Figure 4.12. The example measurement was made using the OP-90 with an output resistor pull-down to a negative bias of -5V. The OP-90 exhibits excellent linearity below 0.5V and indeed behaves well as its output swings to 0.0V. No appreciable offset fall-off was evident. This type of amplifier provides accurate measurement of low level signal while operating at zero-volt input and zero-volt output.

TEST CIRCUIT TO MEASURE SINGLE-SUPPLY AMPLIFIER'S LINEARITY NEAR ZERO-VOLTS

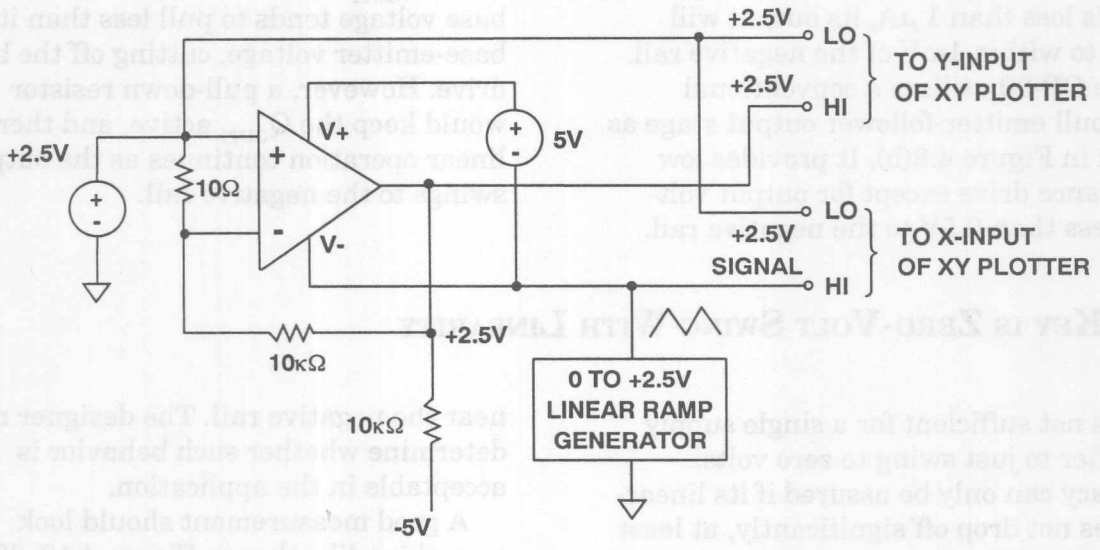


Figure 4.11

A ZERO-IN / ZERO-OUT, SINGLE SUPPLY AMPLIFIER SHOULD EXHIBIT LINEAR PERFORMANCE NEAR ZERO VOLTS OUTPUT

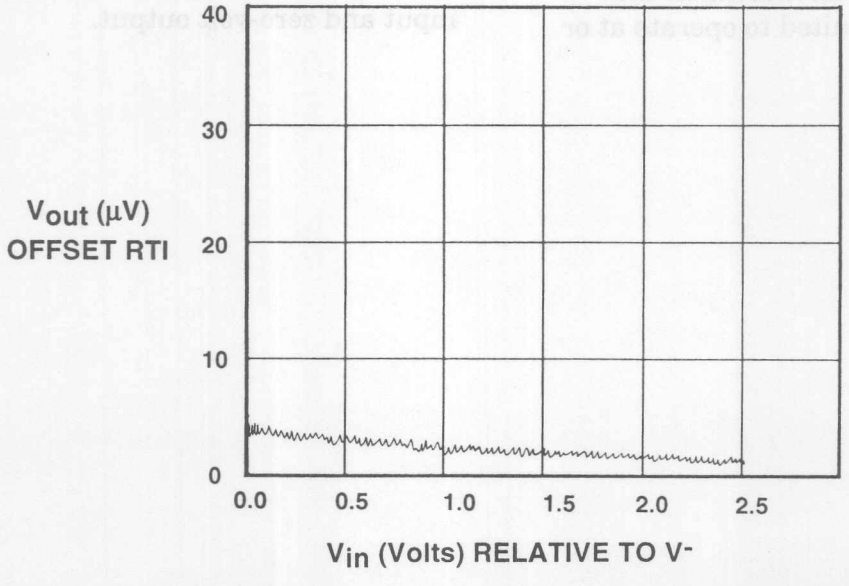


Figure 4.12

Application Example: Designing a True Single-Supply Instrumentation Amplifier

It is not straight forward to design a true instrumentation amplifier that has zero-in and zero-out capabilities. A standard 2 op amp instrumentation amplifier, shown in Figure 4.13, requires special considerations when operating with the negative supply pin at ground.

The main issue is that amplifier "A" needs to be able to sink any current that flows through resistor R_3. With -IN at 0.0V, the output V_{OA} will be at ground potential. Any voltage on the +IN will cause current I_{SINK} to flow through R_3 and into V_{OA}. If V_{OA} changes with changing current, this error will be gained up to the circuit's output V_{OB}, by the ratio of R_4 to R_3. Typical values for a gain of 100 are $R_2 = R_3 = 20\ k\Omega$ and $R_1 = R_4 = 99R_2 = 1.98\ M\Omega$. Assuming a +5V supply and a maximum differential voltage of 40 mV, the maximum amount of sink current is $I_{SINK} = 2\ \mu A$, which occurs when -IN = 40 mV. While this seems like a very small amount, it is significant because amplifier "A" needs to maintain $V_{OA} = 0.000V$. Even as little as a 1 mV error on V_{OA} will lead to a 99 mV error at the output.

While the OP-90 has zero-in / zero-out operation, its output is not able to sink current when its voltage is at 0.000V. Normally a pull-down resistor on the output allows the voltage to swing to around 100 μV. However, since $R_3 = 20\ k\Omega$, the pull-down resistor would need to be less than 400 Ω. Using this value will result in up to 10 mA of extra supply current at high common-mode voltages. Obviously 10mA is unacceptable in a low power design. Thus, how can a true instrumentation amplifier be made when it is used in single supply? One answer to this challenge is an addition of two discrete CMOS N-channel FET transistors configured as a current mirror as shown in Figure 4.14.

The 10 kΩ resistor in combination with Q_1 set up the quiescent current in the mirror, which is approximately 340 μA with a gate-to-source voltage of 1.6V. This keeps Q2 turned on and provides a very low resistance current sink that pulls V_{OA} down to ground. A desirable feature is that this resistance does not shift appreciably as I_{SINK} changes, thus resulting in accurate operation of the instrumentation amplifier.

The benefit of using this method over a simple pull-down resistor is that as the common mode voltage is increased the sink current is limited to just 340 μA by the current mirror. Thus the most current that will be consumed by the two transistors is 680 μA. For example, a common mode voltage of 4.0V results in a V_{OA} voltage of 4.0V. This condition would require the OP-290 to source 10mA with a 400 Ω pull-down in contrast to only 340μA in the case of with the current mirror, producing significant saving in power supply current.

A TRADITIONAL 2 OP-AMP INSTRUMENTATION AMPLIFIER

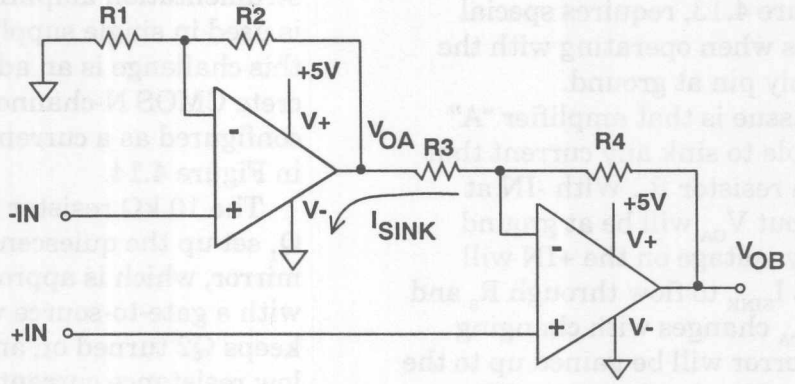


Figure 4.13

A TRUE SINGLE-SUPPLY, ZERO IN/ZERO OUT INSTRUMENTATION AMPLIFIER USING THE OP-290

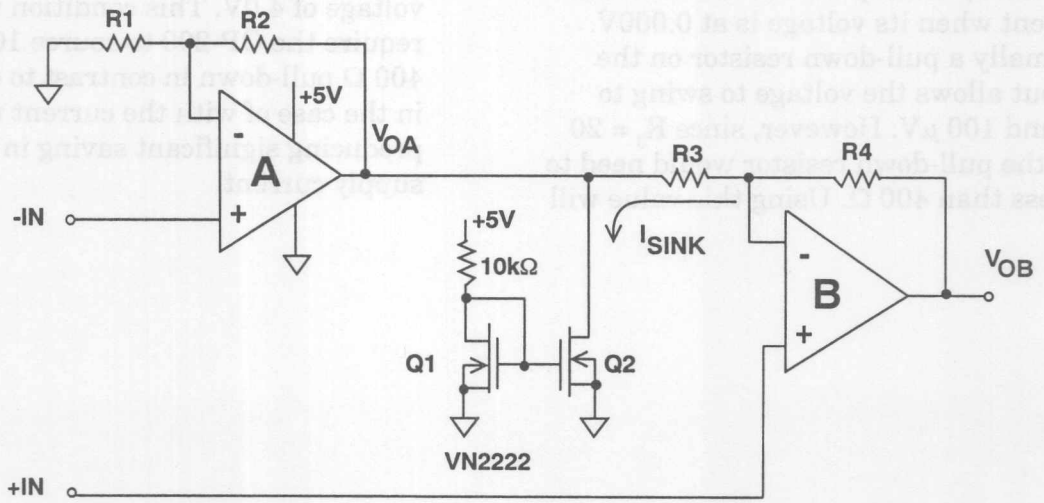


Figure 4.14

OTHER LIMITATIONS OF ZERO-VOLT OUTPUT AMPLIFIERS

No Inverting Amplifier. While the simple non-inverting amplifier configuration serves most amplification functions, grounded rail does not lend itself to inverting a signal. That is, an inverting amplifier usually cannot be implemented unless the input is biased up to a "false-ground" voltage other than the rail.

Unipolar Operation Only. Another way of saying it is that ground-referred single supply non-inverting amplifiers cannot amplify negative signals. They can, but only if used in the inverting mode. This is obvious yet when required, makes the design considerably more complex. An example of a unipolar-only signal conditioning circuit is the thermocouple amplifier in Figure 4.15. This amplifier limits the temperature measurement range from 0°C to 200°C by scaling the amplifier output from 0V to 2.00V, respectively. Clearly the amplifier is not designed to measure temperature below 0°C, that is, below zero volts by virtue of having only one supply. If a negative signal needs to be measured, it is possible to level shift such that the amplifier can deal with negative polarity.

A COLD JUNCTION COMPENSATED BATTERY POWERED THERMOCOUPLE AMPLIFIER

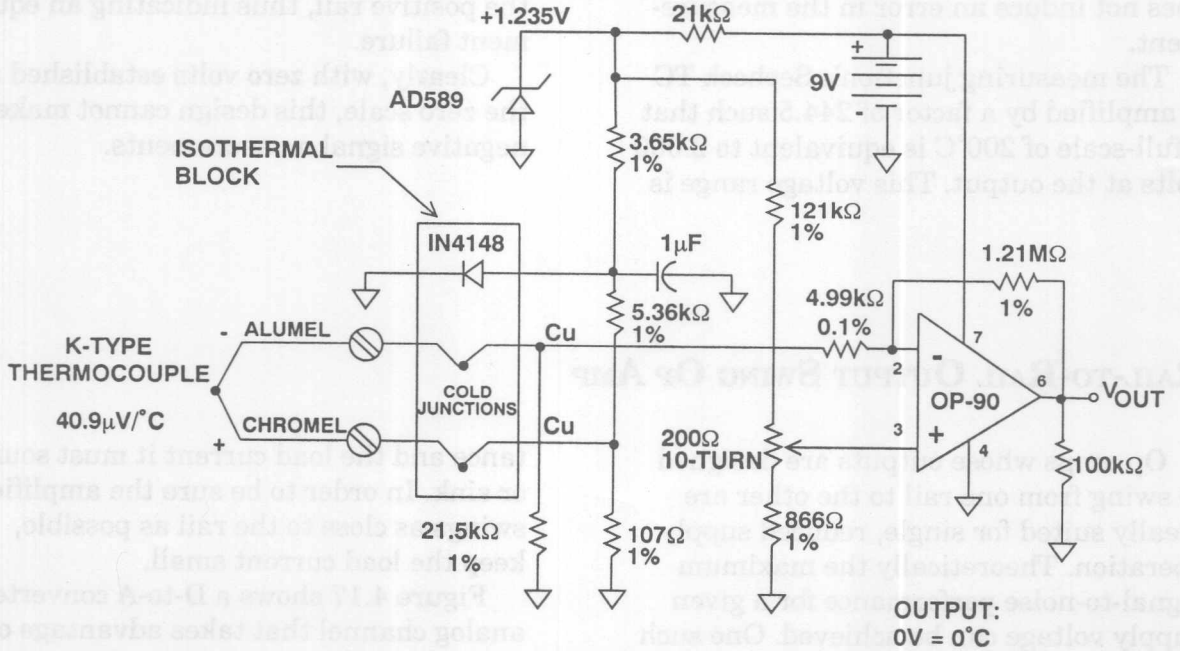


Figure 4.15

This amplifier utilizes the linear portion of the K type thermocouple from 0°C to 200°C. Within this temperature range, the thermocouple's Seebeck coefficient centers at 40.9 μV/°C with a variation of +0.5 μV/°C and -0.44μV/°C. This corresponds to a maximum error of ±1°C at any temperature within this range.

Compensating the cold-junction is made easier by terminating the junctions at the PC board. The operation of cold-junction compensation circuits has been described in the temperature transducer section of this seminar. The object is to keep both terminating junctions at the same temperature at all times regardless of the ambient change. The compensation is accomplished by sensing the junctions temperature with an inexpensive 1N4148 diode, by placing it as close to the junctions as possible. Its temperature coefficient of -2.1mV/°C is divided down by the 107 Ω and the 5.36 kΩ divider to yield a -40.9μV/°C that would exactly cancel the cold-junction T.C. of the thermocouple. Thus any ambient temperature change does not induce an error in the measurement.

The measuring junction's Seebeck TC is amplified by a factor of 244.5 such that a full-scale of 200°C is equivalent to 2.000 volts at the output. This voltage range is compatible with most low-cost single-chip integrating A/D converter for panel meter applications. The 1.235V reference provides stable biasing for the cold-junction compensator as well as for offsetting the amplifier.

A single calibration can be made by adjusting the 200 Ω potentiometer for a 0.00V output with the thermocouple immersed in 0°C ice bath. Although the potentiometer resistance makes up a small part of the 121 kΩ resistor leg, its temperature coefficient should be chosen such that it is smaller than that of the fixed resistors to minimize its overall drift effect.

During normal operation, the 21.5 kΩ resistor is part of the cold-junction compensation circuit whose parallel combination with the 107 Ω resistor forms the T.C.-correction voltage dividing ratio with the 5.36 kΩ. However, it is purposely placed in the "-" side of the thermocouple so that if the thermocouple is disconnected or open-circuited, the 21.5 kΩ pull-down will cause the output to saturate to the positive rail, thus indicating an equipment failure.

Clearly, with zero volts established as the zero scale, this design cannot make negative signal measurements.

Rail-to-Rail Output Swing Op Amp

Op amps whose outputs are designed to swing from one rail to the other are ideally suited for single, reduced supply operation. Theoretically the maximum signal-to-noise performance for a given supply voltage can be achieved. One such rail-to-rail device is the OP-295 dual operational amplifier.

Similar to zero-out op amps, how close a rail-to-rail op amp can swing to either supply depends on its finite output resistance and the load current it must source or sink. In order to be sure the amplifier swings as close to the rail as possible, keep the load current small.

Figure 4.17 shows a D-to-A converter analog channel that takes advantage of the wide output swing of a rail-to-rail op amp. The entire circuit operates off a single +5V supply, and its output swings from 0V to 4.095V full-scale, in 1 mV per LSB increments. Thus the op amp must

OP-295 DUAL RAIL-TO-RAIL OP AMP KEY FEATURES

- Rail-to-Rail Output Swing
- Sinks and Sources Current at the Rails
- Single-Supply Operation ..... +3V to +36V
- Low Offset Voltage ..... 250µV Max
- Low Supply Current ..... 175µA Max
- Gain-Bandwidth Product ..... 100 kHz
- Unity-Gain Stable

Figure 4.16

faithfully reproduce accurate voltages from less than 500 μV to the full-scale of 4.095V in order to preserve the 12-bit performance of the DAC.

In this design, the CMOS D-to-A converter is connected in a voltage switching output mode rather than the normal current output mode so that its output is positive.

In the voltage output mode, the R-2R ladder functions as a voltage divider. A 1.23V reference is selected so that the I_{OUT} pin of the CMOS DAC is biased up no more than 1.25V. The purpose of this is to preserve the full 12-bit linearity performance of the DAC. This is because the I_{OUT} pin is the summing node to which all the R-2R ladder branches are switched by a bank of CMOS transistors whose channel ON-resistances are part of each 2R resistance leg. A minimum of 3.5V gate drive is necessary to fully turn on each transistor. If the I_{OUT} voltage increases beyond 1.25V, the gate drive voltage is correspondingly reduced and hence increases the 2R resistance. Even a slight shift results in poor DAC linearity performance.

The output voltage at the V_{REF} pin exhibits a constant impedance, typically 11 kΩ. The output swings from zero volts for all 0's code to a full-scale reference voltage of 1.23V. The OP-295 serves as a buffer and provides gain up the full-scale output voltage of 4.096V. Overall, the circuit provides 1mV per bit of programmable control. The OP-295 allows the output swing to within 100 μV of ground. In addition, its offset contributes less than 250 μV error. Thus full 12 bit performance is realized.

A 5-VOLT 12-BIT DAC WITH 0 TO +4.095V OUTPUT SWING

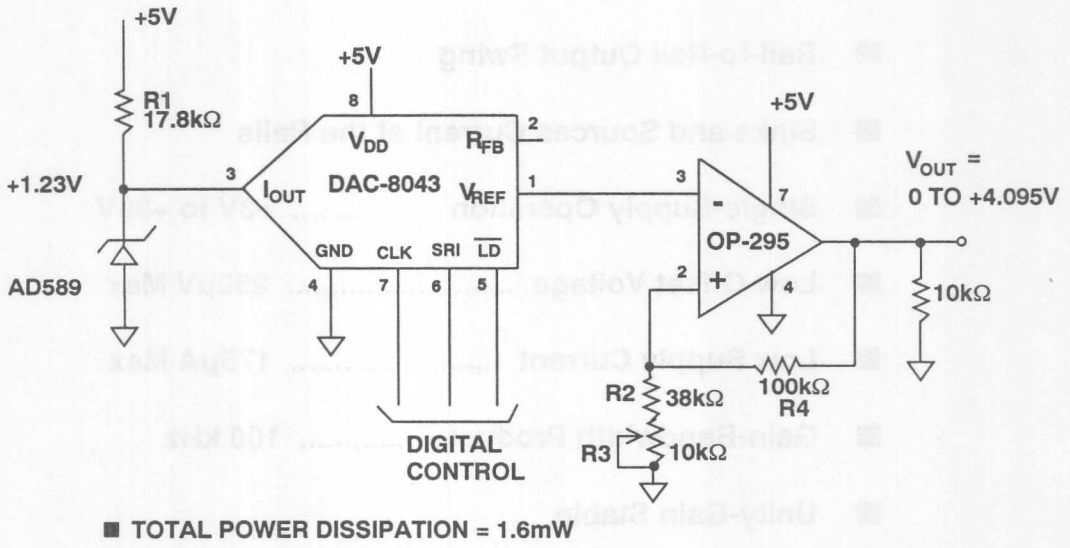


Figure 4.17

A 4.5V REFERENCE REGULATOR WITH <20mV NO-LOAD DROPOUT

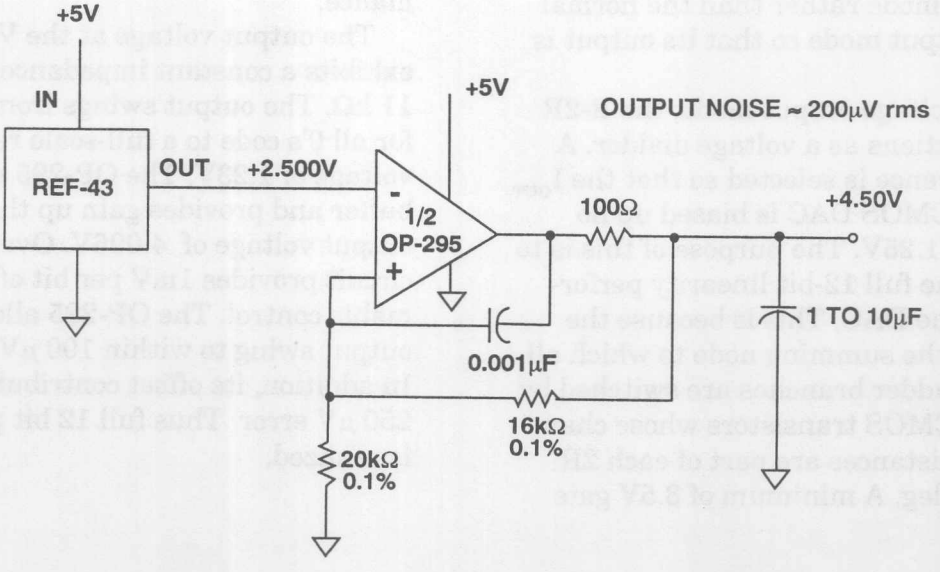


Figure 4.18

The op amp's rail-to-rail swing capability insures the full-scale output will always meet specifications regardless of supply tolerance.

Another useful application is a 4.5V reference that is powered by a single +5V supply as in Figure 4.18. The REF-43 provides a temperature-stable 2.500V reference to the OP-295. It in turn amplifies the signal to 4.50V output.

The amplifier is frequency compensated so that it can drive a 1μF to 10μF output capacitance oscillation. Furthermore, a large capacitor provides a charge reservoir to keep the output stable in the event of a sudden load current surge.

PRECISION SINGLE-SUPPLY OP AMP CHOICES ARE LIMITED

The industry-standard precision op amps such as the OP-07, OP-77, OP-177, AD707/708, etc. are designed to operate with dual, higher voltage (±15V) supplies. Their precision performance is optimized for these supply voltages. As such, trying to operate them at lower voltages may be inadvisable as their specifications may no longer apply. Indeed many do not even function if their inputs are forced to the negative rail, or if they are powered by a single +5V supply.

Very few single-supply op amps exhibit sufficiently low input offset and offset drift to qualify them as precision op amp. The OP-90/OP-290/OP490 come close to precision performance yet can operate off single supply. A comparison of single-supply op amps is given in Figure 4.19.

SINGLE SUPPLY PRECISION OP AMPS

		Max V_{OS}	Max TC V_{OS}	Max I_S (/Amplifier)
Single	OP-20	250μV	1.5μV/°C	80μA
Single	OP-21	100μV	1.0μV/°C	300μA
Single	OP-80	1.5mV	-	325μA
Single	OP-90	150μV	2.5μV/°C	20μA
Dual	OP-220	150μV	1.5μV/°C	85μA
Dual	OP-221	150μV	1.5μV/°C	400μA
Dual	OP-290	200μV	3.0μV/°C	20μA
Dual	OP-295	250μV	<10μV/°C	175μA
Quad	OP-420	2.5mV	10μV/°C	450μA
Quad	OP-421	2.5mV	10μV/°C	450μA
Quad	OP-490	0.5mV	5μV/°C	20μA

Figure 4.19

USING PRECISON OP AMPS IN SINGLE-SUPPLY, LOW VOLTAGE APPLICATIONS

If low offset is required in a single supply, low voltage application, then it may be necessary to choose dual supply, precision op amps to do the job. As mentioned before, most precision op amps do not guarantee their specifications at lower supply voltages. Under these circumstances, the rule to follow is to design conservatively. If the application calls for conditions that are beyond the recommended ranges, most likely the device manufacturer will not be able to guarantee devices' performance — at least not without some additional testing cost. However, often their applications engineering staff may be able to provide sufficient insight as to how to derate from the performance specifications so that appropriate error budgeting can be done.

Most manufacturers' data sheets do provide sufficient information and characteristics of the device to allow for proper "derating" for worst case designs. The following sections provides some guidelines.

HOW LOW CAN THE SUPPLY VOLTAGE GO?

Some device data sheet provides a supply voltage versus supply current curve or a supply voltage range specification that indicate what the device can operate. Furthermore, it is important to decide for the application where the input voltage range and output voltage swing range need to be in order that an op amp choice can be made. Remember that most precision op amps do require a certain amount of supply headroom for both rails. At low supply voltages this means a greatly reduced signal swing.

For example, the industry standard OP-177's input voltage is guaranteed to have a ±13V range with a ±15V supply. At this voltage, the output is guaranteed to swing ±12V into 2 kΩ load. For all practical purposes at reduced supply voltages, the headroom required can be considered to remain constant. Consequently, at ±5V (or +10V) supply, the OP-177's input linear range drops to only ±3V. Similarly its worst-case output swing is expected to have a minimum of ±2V.

INPUT OFFSET VOLTAGE DERATED BY POWER SUPPLY REJECTION

Precision op amps' input offset voltage specification is normally based on a symmetrical, dual supply, and with an input common-mode voltage at zero. At reduced supplies, additional error sets in, in the form of input offset that is introduced by the supply reduction. Consequently the worst-case input offset voltage at reduced supplies can be derated by this additional error.

HOW LOW THE SUPPLY VOLTAGE CAN GO DEPENDS ON:

- THE AMPLIFIER'S INPUT/OUTPUT SWING REQUIREMENT AND CAPABILITY OVER THE FULL TEMPERATURE RANGE

Example: OP-177E (-40°C to +85°C)

	Guaranteed @ ±15V Supply	Expected @ ±5V Supply
Input Voltage Range	±13V	±3V
Output Swing Range	±12V	±2V

Rule to remember: Input/Output headroom is fixed regardless of supply

- THE DEVICE'S MINIMUM SUPPLY OPERATING SPECIFICATION

Figure 4.20

DERATE INPUT OFFSET VOLTAGE ERROR BY THE POWER SUPPLY REJECTION ERROR

- Example: OP-177E @ -40°C to +85°C, V_S Reduced from ±15V to ±5V

Initial Input Offset Voltage:	20µV
Power Supply Rejection Error: (1µV/V × 20V V_S Change)	20µV
Derated Input Offset Voltage:	40µV

Figure 4.21

SUPPLY CURRENT DROPS AS SUPPLY VOLTAGE DECREASES

Generally the op amp's supply current will drop as the supply voltage is reduced, but usually not linearly. Most data sheets specify the maximum supply current at a given supply voltage. But it only gives a *typical* characteristic curve showing the supply current level as a function of supply voltage. The question is what can be counted on as the *worst-case* supply current at a reduced voltage?

It is unlikely any op amp manufacturer has the ready answer to this question and would not be willing to guarantee this or other out-of-the-ordinary specification without conducting an exhaustive characterization and yield studies, which are both expensive and time-consuming. Short of this, one can approach this problem by conservatively derating the specification. An example is shown in Figure 4.22.

ESTIMATE WORST-CASE SUPPLY CURRENT BY CONSERVATIVELY DERATING THE SPECIFICATION

■ Example: OP-177E @ -40°C To +85°C

	Typ	Max
Supply Current @ ±15V	1.6mA	2.0mA

Typical Supply Current: 0.75mA @ ±5V
(From Characteristic Curve)

Normal Derating: (1.25 × 0.75mA): 0.938mA

Apply Additional 30% Derating: 1.22mA
(1.3 X 0.938mA)

Figure 4.22

DERATING INPUT OFFSET VOLTAGE DRIFT

Input offset voltage drift is more difficult to derate, as generally little or no data sheet information is provided to indicate how it behaves as the supply voltage is reduced. In these cases, there are two ways to approach the problem. The more accurate approach is to measure the drift of a sample of devices at both the rated supply voltages as well as at reduced supply. Then apply statistical projection to derive a high-confidence worst-case drift. However, this approach is costly and time-consuming.

The other approach is to derate based on known guaranteed specifications.

Similar to derating the input offset voltage as described in above, the supply rejection ratio provides a good indicator of the behavior of the input offset drift characteristic at reduced supplies. Worst-case offset drift can be calculated based on the guaranteed initial V_{os} @ 25°C assuming it is at one polarity drifting to the opposite polarity of the data sheet's guaranteed maximum V_{os} error due to temperature plus reduced supply voltages. This is shown in Figure 4.23 for the OP-177G.

DERIVING INPUT OFFSET VOLTAGE DRIFT AT REDUCED SUPPLY VOLTAGES

■ Example: OP-177G @ -40°C To +85°C, V_S Reduced From ±15V To ±5V

Initial V_{OS} (@ 25 C) = 60µV

Total V_{OS} (over temp):

Maximum V_{OS}	= 100µV
PSRR (106dB) Error	= 100µV
	200µV

Worst-Case V_{OS} Drift = (60µV + 200µV) / 65°C
(+25°C To -40°C) = 4µV/°C

Figure 4.23

The above worst-case analysis assumes that the drift is linear, although in reality it is almost never linear over the entire temperature range. However, the nonlinear behavior generally is not radical enough to significantly affect the worst-case estimate.

NOISE INCREASES AS SUPPLY VOLTAGES DECREASE

As the supply voltages decrease, the corresponding reduction in supply current causes the op amp's input stage current to decrease. The consequence of it is the input voltage noise tends to increase.

How much the voltage noise increases is difficult, if impossible, to predict as usually no information is given to indicate its noise level as a function of the supply voltage. Furthermore, one cannot assume the input stage current is linearly proportional to the total supply current, and hence provide a reliable prediction of the current noise level.

The best way is to measure the noise voltage at the supplies that one intends to operate. A simple voltage noise test circuit is shown in Figure 4.24 below.

VOLTAGE NOISE TEST CIRCUIT AT REDUCED SUPPLIES
0.1Hz TO 10Hz
VOLTAGE GAIN = 10,000

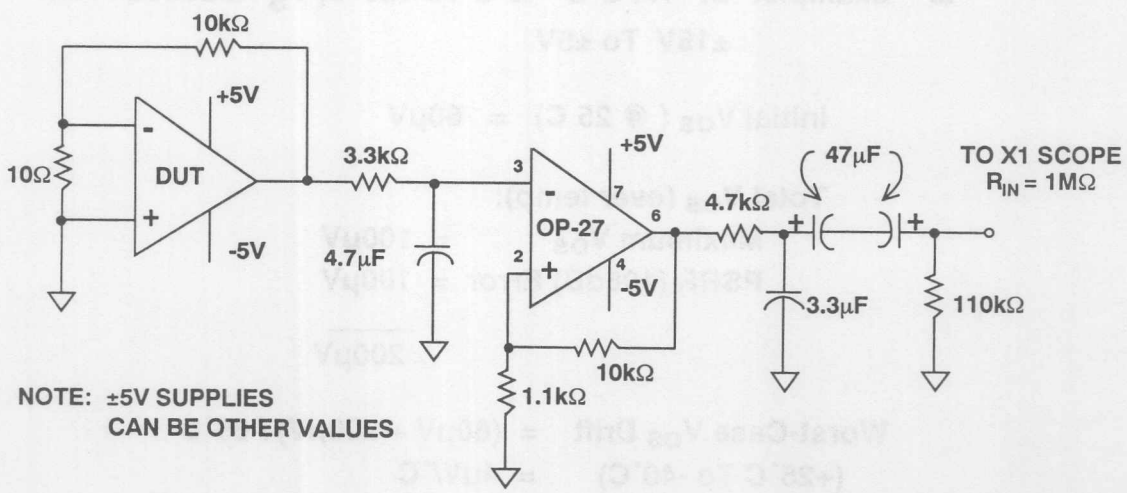


Figure 4.24

Be aware that the DUT stage has a gain of 1,000. If the op amp under test has an offset voltage more than 200 μV, it may be enough to drive one or both op amp stages into saturation. In that case, an erroneously low noise will be measured at the output. High offset op amps can be measured by reducing the D.U.T. stage's feedback resistance from 10 kΩ to 2 kΩ. In which case, the test circuit can accommodate op amps that have up to 1 mV offset.

REDUCED BANDWIDTH AND SLEW RATE

All AC parameters tend to get worse with reduced supply voltages. Most notable are bandwidth and slew rate. That is because the op amp's supply currents tend to decrease, pushing the internal transistors' operating points lower. Some op amp data sheets do show AC characteristic curves or have specifications at lower supply voltages. This is usually true for single supply op amps as they are specifically designed for low voltage operations. However, most precision op amps that are designed for ±15V do not offer much AC information at reduced supplies. Consequently, one must measure these performance characteristics at the appropriate voltages.

Generally most precision measurement applications do not call for any stringent bandwidth or slew rate performance. In fact, a reduced bandwidth may provide built-in noise band filtering.

LOW SUPPLY CURRENT INCREASES NOISE

Most single supply op amps are designed to draw low supply current, at the expense of having higher voltage noise. This tradeoff may be necessary because the system must be powered by a battery. However, this condition is worsened because all circuit resistances tend to be higher. As a result, in addition to the op amp's voltage noise, Johnson noise (resistor thermal noise) is also a significant contributor to the total noise of the system.

The choice of monolithic op amps that combine the characteristics of low noise and single supply operation is rather limited. Most single supply op amps have noise on the order of 30 to 60 nV/$\sqrt{\text{Hz}}$. On the other hand, a dual-supply, 5 nV/$\sqrt{\text{Hz}}$ op amp's input and output voltage ranges require at least a couple of volts from either supply rails.

In order to achieve both low noise and low supply voltage operation, discrete designs may provide the solution. The circuit in Figure 4.25 uses a rail-to-rail op amp (OP-295) and a discrete PNP matched transistor pair (MAT-03) to achieve true zero-in / zero-out single supply operation with an input voltage noise of 3.1nV/$\sqrt{\text{Hz}}$ at 100 Hz. R_5 and R_6 yield a gain of 1000, making this circuit ideal for maximizing dynamic range when amplifying low level signal in single supply. The OP-295 provides rail-to-rail output swings allowing this circuit to operate with 0 to 5V outputs. Only half of the OP-295 is used leaving the other uncommitted op amp for use elsewhere.

A LOW NOISE SINGLE SUPPLY PREAMPLIFIER

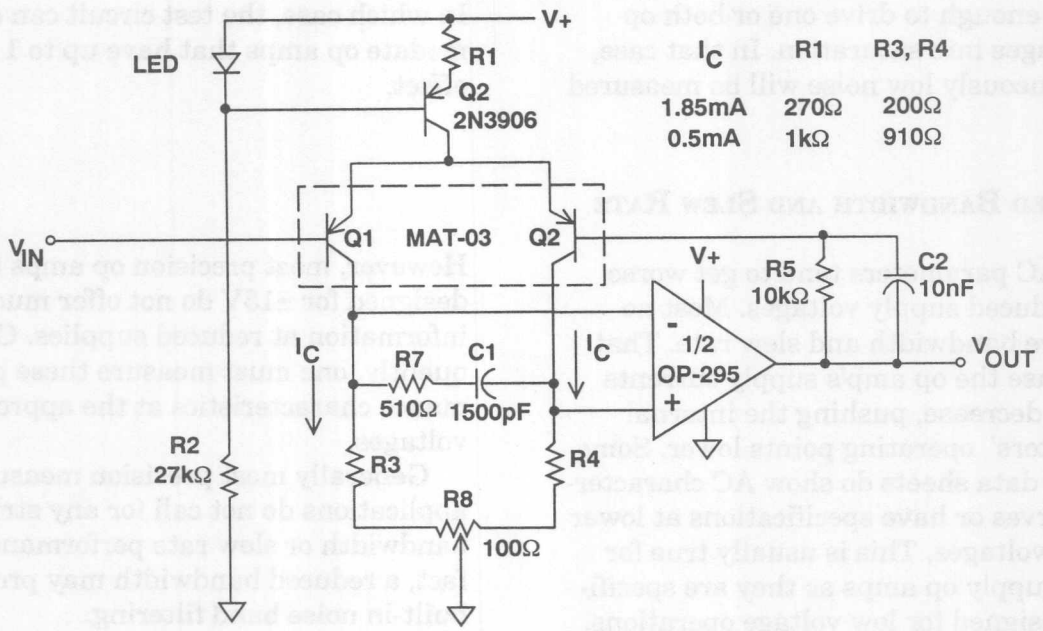


Figure 4.25

The input noise is controlled by the MAT-03 transistor pair and its collector current level. Increasing the collector current reduces the voltage noise. This particular circuit was tested with 1.85 mA and 0.5 mA of current. Under these two cases, the input voltage noise measured 3.15nV/$\sqrt{Hz}$ and 8.6 nV/$\sqrt{Hz}$ at 100Hz, respectively. The high collector currents lead to higher supply current consumption, higher input bias current, and higher current noise. For example, the MAT-03's typical h_{FE} of 165 produces bias currents of 11 μA and 3 μA, respectively. Based on the high bias currents, this circuit is best suited for applications requiring low source impedances, such as magnetic pick-ups or low impedance strain gauge sensors. In addition, high source impedance will degrade the noise performance. For example, a 1 kΩ resistor generates 4nV/$\sqrt{Hz}$ of broadband noise, which is already greater than the preamp by itself.

The collector current is set by R_1 in combination with the LED and Q2. The LED provides a 1.6V reference whose temperature coefficient closely matches that of Q2's base-emitter junction TC, thus producing a constant 1.0V drop across R_1. With R_1 equal to 270 Ω, the tail current is 3.7 mA, and the collector current is half that, or 1.85 mA. The value of R_1 can be altered to adjust the collector current.

Whenever R_1 is changed then R_3 and R_4 should also be adjusted. To maintain a common-mode input range that includes ground, the collectors of Q1 and Q2 should not go above 0.5V, otherwise they could saturate. Thus R_3 and R_4 have to be small enough to prevent this condition. Their values and the overall performance for two different values of R_1 are summarized in Figure 4.26.

Lastly, the potentiometer R_8 is needed to null the offset voltage to zero. Similar performance can be obtained using an OP-90 as the output amplifier with a savings of about 185 μA of supply current. However, the output swing will not include the positive rail, and the bandwidth will reduce to approximately 250 Hz.

SINGLE SUPPLY LOW NOISE PREAMP PERFORMANCE

	I_C = 1.85mA	I_C = 0.5mA
R1	270Ω	1.0kΩ
R3,R4	200Ω	910Ω
e_n @ 100Hz	3.15nV/$\sqrt{Hz}$	8.6nV/$\sqrt{Hz}$
e_n@ 10Hz	4.2nV/$\sqrt{Hz}$	10.2nV/$\sqrt{Hz}$
I_{SY}	4.0mA	1.3mA
I_B	11μA	3μA
Bandwidth	1kHz	1kHz
Closed Loop Gain	1000	1000

Figure 4.26

OUTPUT DRIVE CAPABILITY LIMITED

Low power op amps typically operate on very low levels of quiescent stage currents. Consequently, their output transistors' base drive is usually small. As a result, the output drive capability is limited as well. Typical low power op amps can handle several milliamps before the output transistor becomes base-current starved. Most will limit at about 10 mA.

Indeed, low power op amps are primarily designed for applications that conserve power, and therefore are not often called upon to deliver much current. Output voltage swing is usually much more of a concern.

HIGH CIRCUIT IMPEDANCES ARE SUSCEPTIBLE TO NOISE PICKUP

Since low power circuits tend to use high value resistors to conserve power, this tends to make the circuit more susceptible to externally induced radiated noise and conducted noise. Even a small amount of parasitic capacitance can create a significant conduction path for noise to penetrate.

For example, as little as 1 pF of parasitic capacitance allows a 5V logic transition to cause a large disturbance in a 100kΩ circuit as illustrated in Figure 4.27.

HIGH CIRCUIT IMPEDANCES INCREASE SUSCEPTIBILITY TO NOISE PICKUP

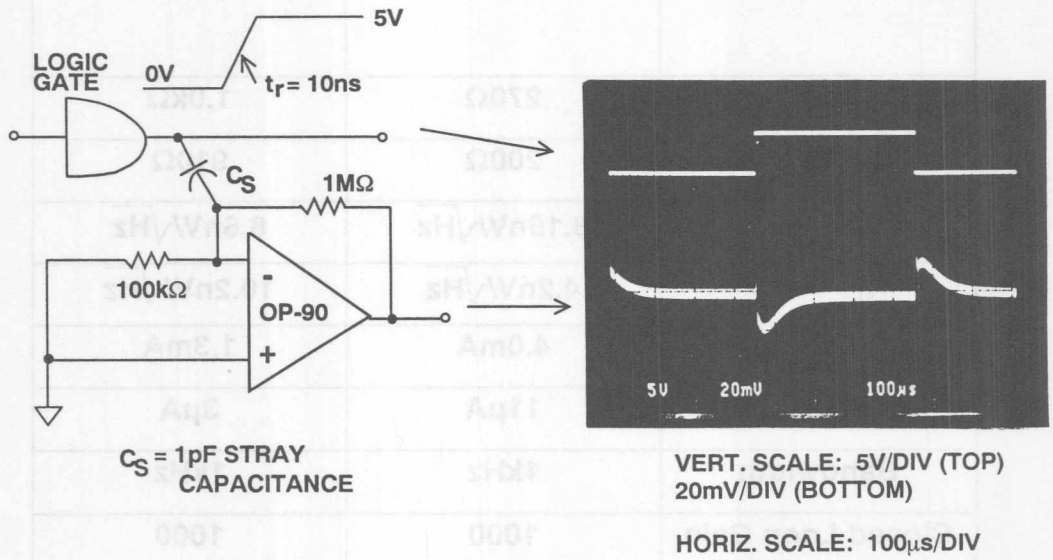


Figure 4.27

This serves to illustrate that high impedance circuits are full of potential parasitics which can cause a good paper design to perform poorly when actually implemented. One needs to pay particular attention to the routing of signals. Interestingly, many high-frequency layout techniques for eliminating parasitics can also be applied here for low frequency, low power circuits — for different reasons. While circuit parasitics cause unwanted phase shifts and instabilities in high frequency circuits, the same parasitics pick up unwanted noise in low power precision circuits.

CIRCUIT LAYOUT GUIDELINES TO MINIMIZE NOISE PICKUP PROBLEMS

- Keep Circuit Trace Interconnection Short
- Keep Circuit Compact
- Keep Summing Junction Component Leads Short
- Bypass Power Supplies
- Keep Digital Circuit Traces Away From Analog Circuits
- Use Single Point Ground Where Possible

Figure 4.28

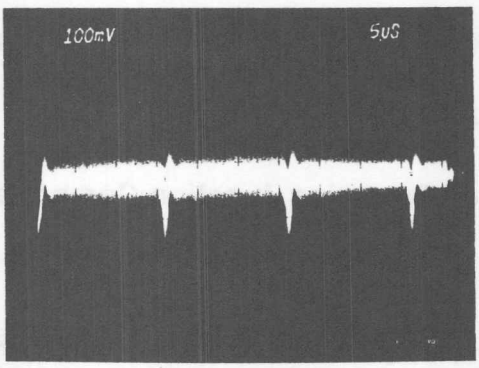
HOW TO POWER ANALOG CIRCUITS USING A +5V LOGIC SUPPLY

Since +5V is ubiquitous and universally available in every system, we are constantly tempted to use it to power analog circuits. With a bit of sound engineering and careful filtering, there is no reason why this cannot be accomplished in most cases.

The first mistake often made is to tap the supply close to the logic circuit, usually because of convenience, without rerouting the supply connections. The problem starts when the fast logic transition edges induce high current pulses which last nanoseconds to sub-nanoseconds. With the logic circuits located some distance away from the supply, as little as a few inches can have significant resistance and inductance allowing the current pulse to generate several 100 millivolts of voltage glitches.

These spikes usually permeate throughout the logic circuit's ground and the supply lines. Figure 4.29 shows what a typical computer system's +5V supply at the logic circuit looks like with all the noise riding on it. Tapping the logic supply at this point will corrupt the analog circuits with unwanted high frequency spike noise. Much of this noise is not common-mode (same amplitude and phase) to the supply and ground lines. Therefore, the analog circuit cannot reject it easily. Filtering them becomes very difficult.

DO NOT USE +5V LOGIC SUPPLIES TO POWER ANALOG CIRCUITS



VERTICAL SCALE: 100mV / div.
HORIZONTAL SCALE: 5µs / div.

Figure 4.29

DIFFERENTIAL LC FILTER TURNS NOISY LOGIC SUPPLIES INTO NOISE-FREE ANALOG SUPPLIES

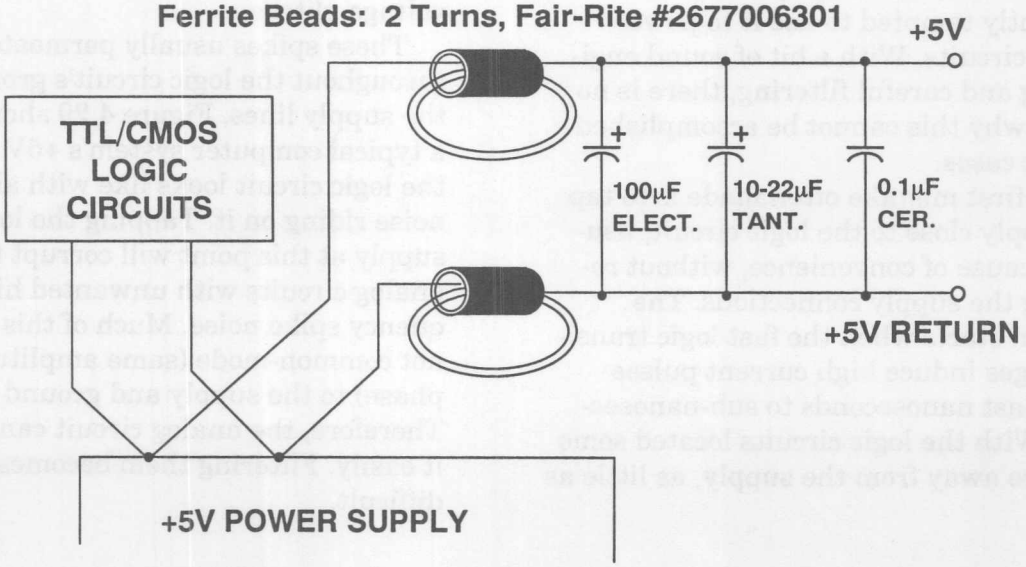


Figure 4.30

However, glitch noise directly at the power supply output is usually much less than it is directly at the noisy logic circuit interface. However, some glitch noise may still be present directly at the power supply output, not due to the logic circuit noise, but because of the power supply's high energy switching circuit (typical of a switching power supply). For these reasons, all analog circuits should be powered directly from the power supply outputs using appropriate filtering between the power supply output and the analog circuits. A clean, analog-grade supply can be generated from a +5V logic supply using a differential LC filter with separate power supply and return lines as shown in Figure 4.30.

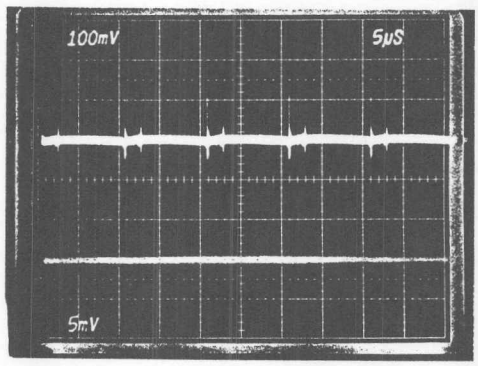
The supply output is virtually free of any glitch noise as evident in the scope photo in Figure 4.31, which compares the input and output sides of the filter. All capacitors used were selected from commonly available types. Lower noise can be attained using low ESR (Equivalent Series Resistance) type electrolytic and tantalum capacitors.

The circuit as shown can easily handle 100 mA of load current without the risk of saturating the ferrite core. Higher current capacity can be designed using correspondingly larger ferrites. The same or similarly valued circuit can also be used for higher supply voltages such as +12V and +15V.

LC FILTER VIRTUALLY ELIMINATES ALL GLITCH NOISE

BEFORE FILTER

AFTER FILTER



VERTICAL SCALE: 100mV / div.
HORIZONTAL SCALE: 5μs / div.

Figure 4.31

+3V SUPPLY OPERATION?

The current trend is for systems to move from +5V supply to +3V supply in order to accommodate higher speed logic circuits at reduced levels of power consumption. Actual implementations have so far been confined to certain specific applications such as camcorders, cellular communications, etc. Although these applications are relatively few in comparison to other applications for low supply amplifiers, they are growing and increasing in popularity. Perhaps in the future, +3V operation for analog circuits will become an important requirement.

Going to +3V or less will narrow op amp and component selection even further. All the above design considerations and tradeoffs will become more complex.

SECTION V
APPLICATIONS FOR AMPLIFIERS IN AUDIO

- A Low Noise Microphone Preamplifier with DC Servo Loop

- Line Receivers:
  Basic Discrete Audio Line Receiver, Integrated Line Receiver

- Line Drivers:
  "Inverter / Follower" Line Drivers, Cross-Coupled Differential Line Drivers, Integrated Line Drivers, A High Performance Composite Audio Line Driver Stage

SECTION V

APPLICATIONS FOR AMPLIFIERS IN AUDIO

WALT JUNG

INTRODUCTION

Today, IC amplifiers are available which perform many of the tasks required within audio systems. Many of these functions can be performed by standard op amps, although not always with optimum performance.

Audio circuit performance requirements can often be demanding in terms of very low noise, very high current and/or voltage outputs, and low signal distortion. While standard amplifiers exist which excel in all of these areas, some functions may need higher levels of system integration to make them performance and cost effective to the audio designer. Some cases in point are described in the sections following, under audio line drivers and receivers.

Another factor strongly influencing audio circuit design is the concept of the *universal* single/dual audio op amp readily available at low cost. Quite often however the only critical specification qualifying such devices is simply and solely their low cost. Frequently other IC devices might be available which can meet or exceed performance in one or more key areas, but don't get due consideration because of entrenched standards.

Audio, like many other electronic design areas, needs full and thoughtful regard of many issues for the most effective device selection. Distortion under load must be low, common mode rejection must be high, power consumption must be reasonable, and a minimum of related components should be required.

Fortunately, a wide variety of very high performance IC amplifiers are available to meet these audio demands. Some of them are designed specifically for audio application requirements, such as balanced input/output interfacing, very low voltage noise, high output currents, etc. Others achieve one or more of these objectives through the use of standard IC devices, in topologies most useful to audio requirements. The circuits following illustrate examples of both of these design approaches in high performance audio applications, with characterization data accompanying them to aid assessment.

A LOW NOISE MICROPHONE PREAMPLIFIER WITH DC SERVO OUTPUT

The SSM-2017 audio preamplifier chip is a versatile differential input IC with an input voltage noise of less than $1nV/\sqrt{Hz}$, and low distortion. The gain of the device is set via one external resistor, R_g, and it is adjustable over a range of 1-1000 times. Differential inputs of the SSM-2017 allow balanced input signal operation, and the single-ended output signal of the device appears between the output and reference terminals. It operates from dual power supplies of ±22V or less, and drives loads of 2kΩ or more.

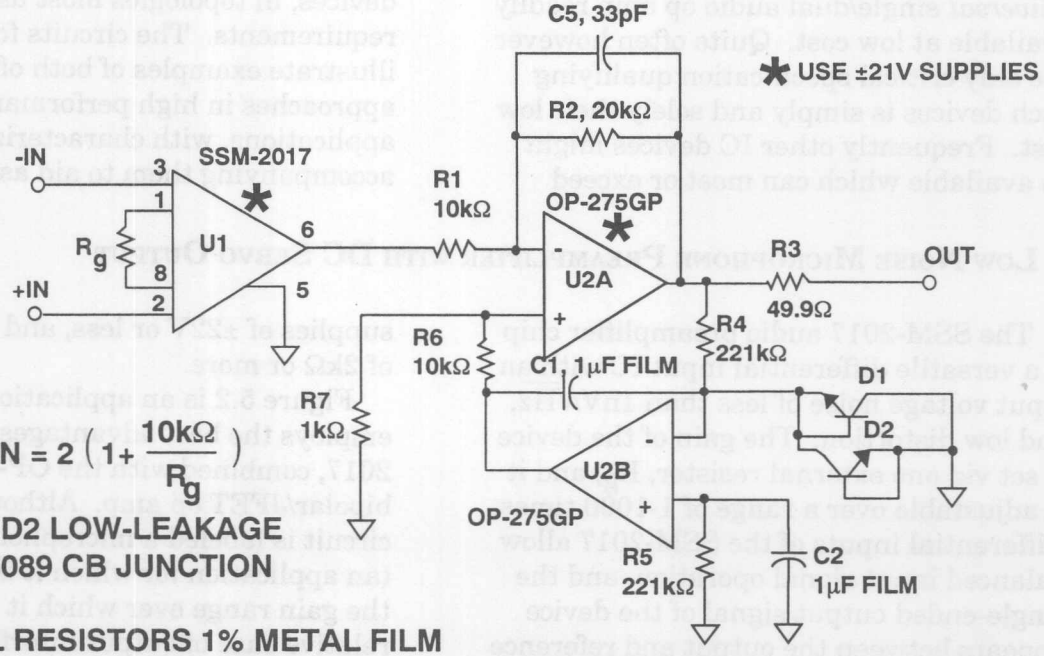
Figure 5.2 is an application which employs the best advantages of the SSM-2017, combined with the OP-275 dual bipolar/JFET op amp. Although this circuit is labeled a microphone preamp (an application for which it is well suited) the gain range over which it operates and relative ease of output interfacing make it general purpose as well.

AUDIO SPECIFICATIONS AND CONSIDERATIONS

- Total Harmonic Distortion (THD)
- Noise
- Output Level and Drive Capability
- Power Dissipation
- Cost
- Single IC or Multiple Components

Figure 5.1

LOW-NOISE MICROPHONE PREAMP WITH DC SERVO LOOP



- GAIN = $2\left(1+\frac{10k\Omega}{R_g}\right)$
- D1, D2 LOW-LEAKAGE 2N5089 CB JUNCTION
- ALL RESISTORS 1% METAL FILM

Figure 5.2

As noted, the SSM-2017's strengths lie in low noise and distortion, and gain flexibility/simplicity. It is, however, rated only for 2kΩ or higher loads, making drive for 600Ω loads relatively limited with the basic device. However, the circuit here uses a combination technique, where virtues of two different IC amplifiers merge into a single overall structure which is useful to these points.

Here, the SSM-2017 is used to high advantage in the programmable gain input stage, and it is combined with a fixed gain, high current output buffer with DC servo stage, using the OP-275. This allows the best performance features of both ICs to be realized, each optimized for their respective input/output functions. The OP-275 output buffer provides the low distortion high level drive into 600Ω loads, with the second half of the IC used as a servo to control output offset. The OP-275 gain stage U2A also is operated at a modest gain of 2 times, keeping the required output swing of the SSM- 2017 to a minimum and distortion low.

DESIGN CONSIDERATIONS

The circuit uses stage U1 as a gain programmable SSM-2017 preamp block, where the gain of this stage is set by R_g. This gain, G1, is essentially as described on the SSM-2017 data sheet, or:

$$G1 = \frac{10k\Omega}{R_g} + 1 \quad .$$

The second stage of the circuit is a inverting buffer using the OP-275 op amp U2A, where the stage gain (G2) will be:

$$G2 = -R_2/R_1 \quad .$$

In this design the values for R_1-R_2 are fixed at 10kΩ/20kΩ, so the gain G2 is -2. The overall gain G is the product of G1 and G2, or:

$$G = 2\left(\frac{10k\Omega}{R_g} + 1\right) .$$

In practice, R_g is selected as a gain control for the entire circuit, using a minimum gain of 2, as:

$$R_g = \frac{20k\Omega}{G - 2} .$$

Note that these gain figures will be altered somewhat by loading due to R3.

Also, because of the signal inversion in stage U2, the respective input signs of U1 are reversed regarding overall operation. Various input interface schemes to U1 can be used for connections to both microphones or other sources.

The DC servo stage U2B senses the output DC from U2A and compares this level against the common reference point. U2B is an inverting integrator with an overall low frequency rolloff of about 0.12 Hz. With this servo loop operating, the net output DC offset will be essentially the sum of the voltage offset of U2B, and the offset current errors, and will be independent of the output DC offset of U1. With 1% values used for R_4 and R_5, the circuit's overall DC offset should typically be about 2mV. For lowest integration errors, film capacitors should be used for C_1 and C_2, such as polycarbonate or polyester types. Diodes D_1 and D_2 provide protective clamping for U2B.

MICROPHONE PREAMP PERFORMANCE

This amplifier's performance is quite good over programmed gain ranges of 2-2000. For a typical audio load of 600Ω, THD+N at various gains and an output level of 10Vrms is shown in Figure 5.3. For all but the very highest gain the THD+N is consistent and well below 0.01%, while the gain of 2000 becomes more limited by noise.

In terms of other operating hints, maximum output will be a function of the power supplies, and can be as high as 10Vrms, with higher voltage supplies. Note that output resistor R_3 will limit the swing available when driving 600Ω, but should be retained for short circuit protection. Thus supplies on the order of ±20V are appropriate for the highest output into 600Ω. Aside from this maximum swing consideration, the circuit can be operated on lower supply voltages, with proportionally less output.

To get the most from this circuit 1% metal film resistors are recommended, and a neat, compact layout should be used. Regulated power supplies should be used, and they should also be well bypassed with large electrolytics returned to the output common point.

LOW NOISE MICROPHONE PREAMP THD + N PERFORMANCE, V_{out} = 10V rms, R_{load} = 600Ω

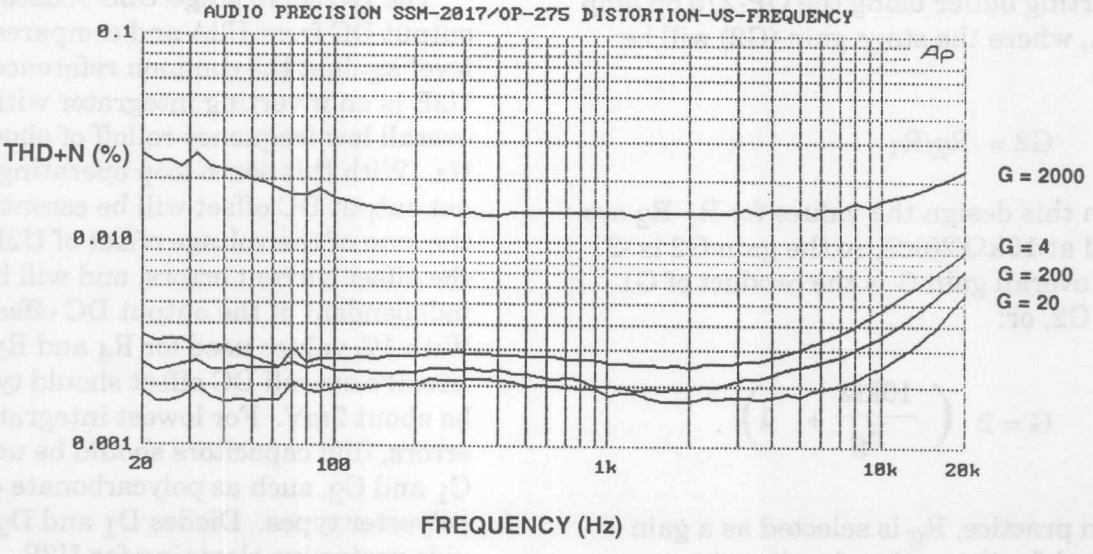


Figure 5.3

LINE DRIVERS AND RECEIVERS FOR HIGH PERFORMANCE AUDIO

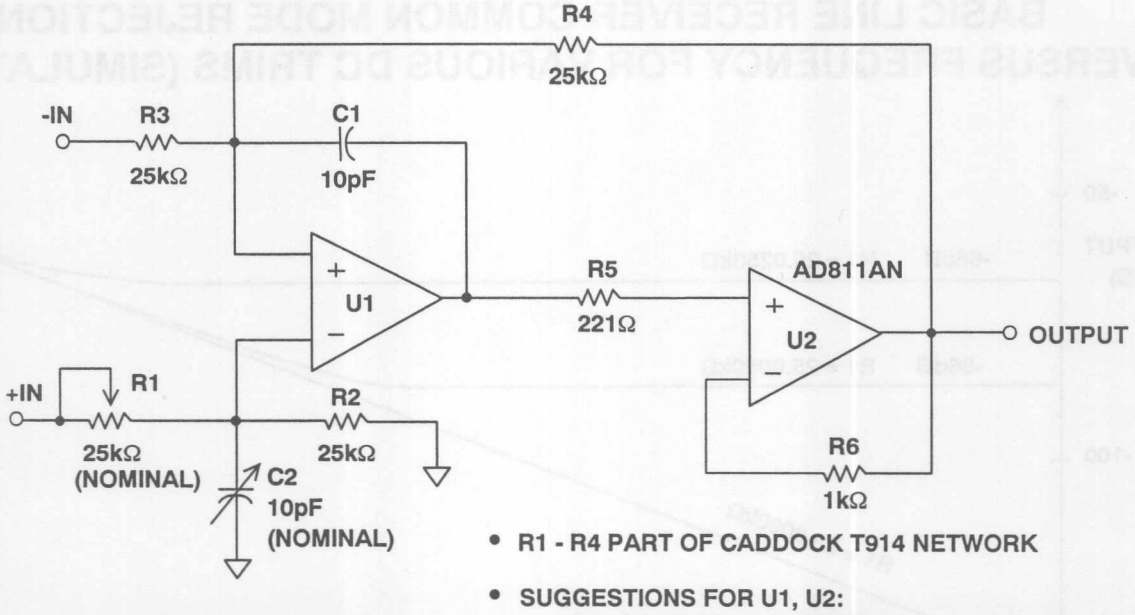
The functions of sending and receiving audio signals between the various components of audio systems has traditionally involved tradeoffs between expense and performance. Everyone can easily understand that fully differential or balanced transmission systems are best at rejecting noise, both low frequency and RF. Given that, what is more difficult is the management of large system designs using differential drivers/receivers. Keeping the final design within reasonable boundaries of cost, size and weight while reaping the technical benefits has not always been a straightforward task.

LINE RECEIVERS

A brief operational review of a standard differential line receiver function will help understand why designs for these devices have evolved into what they are today. Figure 5.4 is a diagram of a classic differential amplifier, using a four resistor bridge and a single (buffered) op amp for the gain stage. (In system terms, this general circuit is also known as an *instrumentation amplifier*, IA for short. and is discussed elsewhere in these notes.

Within this audio discussion, we will call it simply a line receiver for brevity — to be understood as short for *differential* line receiver). This line receiver is *critically* dependent upon the resistors for good performance, a point which should be clear shortly. The amplifier can also be critical; if not chosen carefully for such parameters as CMRR it also can limit performance, as it can for other reasons.

BASIC AUDIO LINE RECEIVER



- R1 - R4 PART OF CADDOCK T914 NETWORK
- SUGGESTIONS FOR U1, U2:
  - (a) U1 = OP-275, U2 OPTIONAL
  - (b) U1 = OP-275, U2 = AD811
  - (c) U1 = AD744, U2 = AD811

Figure 5.4

As a matter of fact, this circuit appears (on the surface at least) to be somewhat trivial... all one needs to implement it are four good resistors and a decent op amp. Dependent upon your definition of "good", this can indeed get you going, at least in a functional sense. But how well the circuit will work in terms of common mode rejection (CMR) is another story altogether.

The main purpose of this circuit is to reject noise common to both inputs, as might be picked up on a twisted pair cable for example. However, even with a high quality op amp for U1, the noise rejection properties of the circuit can only be as good as the matching of the four resistors. To be more precise, the resistors *ratios* R_2/R_1 and R_4/R_3 must match extremely well to reject noise (their absolute values are secondary in importance to their ratio matching).

It is tempting to just pick four 1% resistors from a batch, a step which can yield ratio matching of say 0.1% (at least for a while). However, even with care this will just achieve a CMR of better than 60dB, and if you used the four 1% resistors where only *one* was off by 1%, you'd get about a 46dB CMR.

Clearly then, this circuit is one which needs four resistors made and trimmed simultaneously on a single substrate, to be most effective. Only in this way can the very tight ratio requirements be achieved initially and held stable over time and temperature.

SIMULATION RESULTS

A couple of simulations show just how critical the circuit is with regard to the resistors, and is reflected in Figure 5.5.

In this figure, a display of CMR in dB of this circuit is shown, with three of the four resistors fixed at 25kΩ, and one, R_1,

BASIC LINE RECEIVER COMMON MODE REJECTION VERSUS FREQUENCY FOR VARIOUS DC TRIMS (SIMULATION)

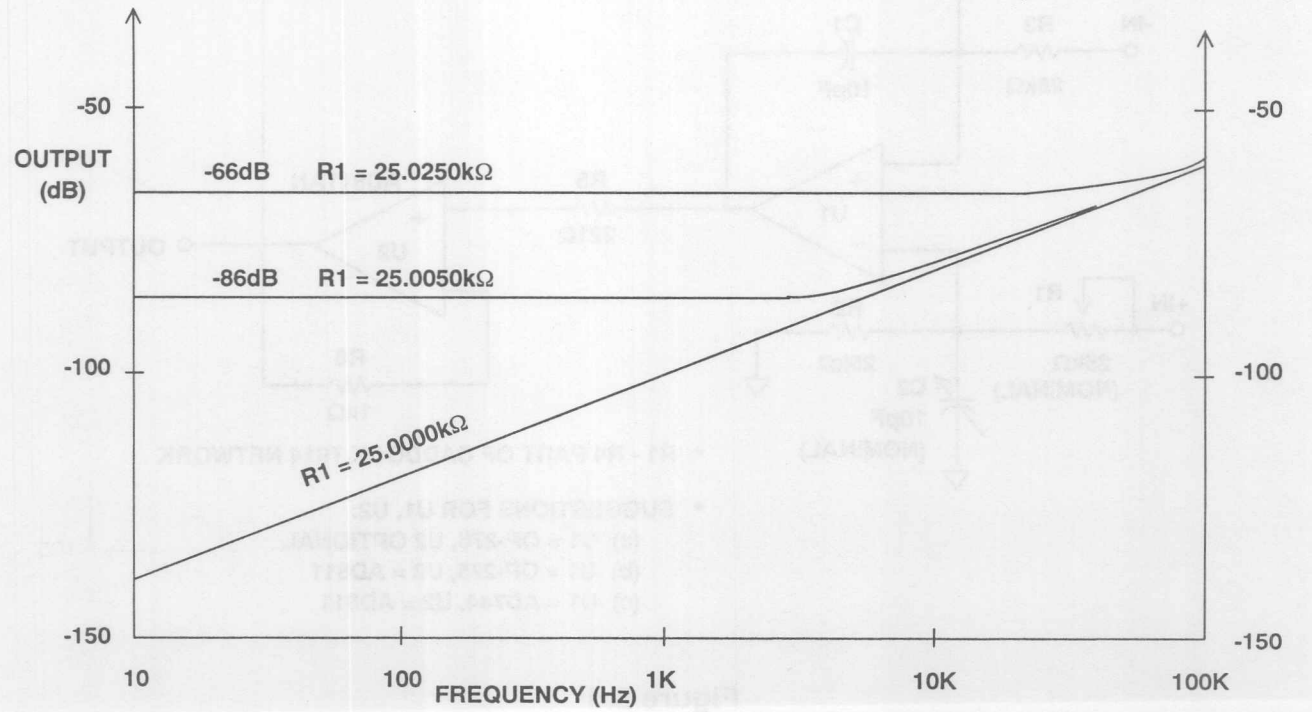


Figure 5.5

is stepped. In the simulation, R_1 ranges from 25.0250kΩ (plus 25Ω or 0.1%) down to exactly 25kΩ (a perfect match), with steps of 0.0025kΩ (2.5Ω or 0.01%). For clarity, only the range extremes are shown in the figure. The 0.1% mismatch curve is at the top of the display, where the CMR is 66dB. The CMR increases to 86dB for the step where R_1 is 25.0025kΩ (plus 0.01%). For the last step, where the four resistors are balanced perfectly, the CMR is frequency dependent, limited by the mismatch of capacitors C_1-C_2 (10 and 10.1pF).

Some important points come from this experiment. To realize a CMR of greater than 80dB, the resistors need to be matched to 0.01%. In more general terms, one can extrapolate up/down this scale as well, that is more than 100dB CMR requires matching to 0.001%. Obviously, high CMR performance with this type of circuit demands extreme performance of the resistor network, more so when potentially degrading effects of time and temperature are factored in. Stable networks of this type using thin film technology are commercially available from companies such as Caddock and Vishay, but they are not inexpensive in the tight ratio matches required.

The above discussions deal with DC matching, but in fact the ratio needs to be maintained for AC as well as DC, to achieve flat noise rejection over frequency. For this to be effective, the nodal capacitances from the R_2/R_1 and R_4/R_3 junctions need to be balanced. In an actual circuit this can be achieved with very low and balanced parasitic capacitances at these points. In an AC simulation, the capacitors C_1 and C_2 were used to illustrate this point, with C_2 varied in 1pF steps from 5pF to 10pF. The results are shown in Figure 5.6.

BASIC LINE RECEIVER COMMON MODE REJECTION VERSUS FREQUENCY FOR VARIOUS AC TRIMS (SIMULATION)

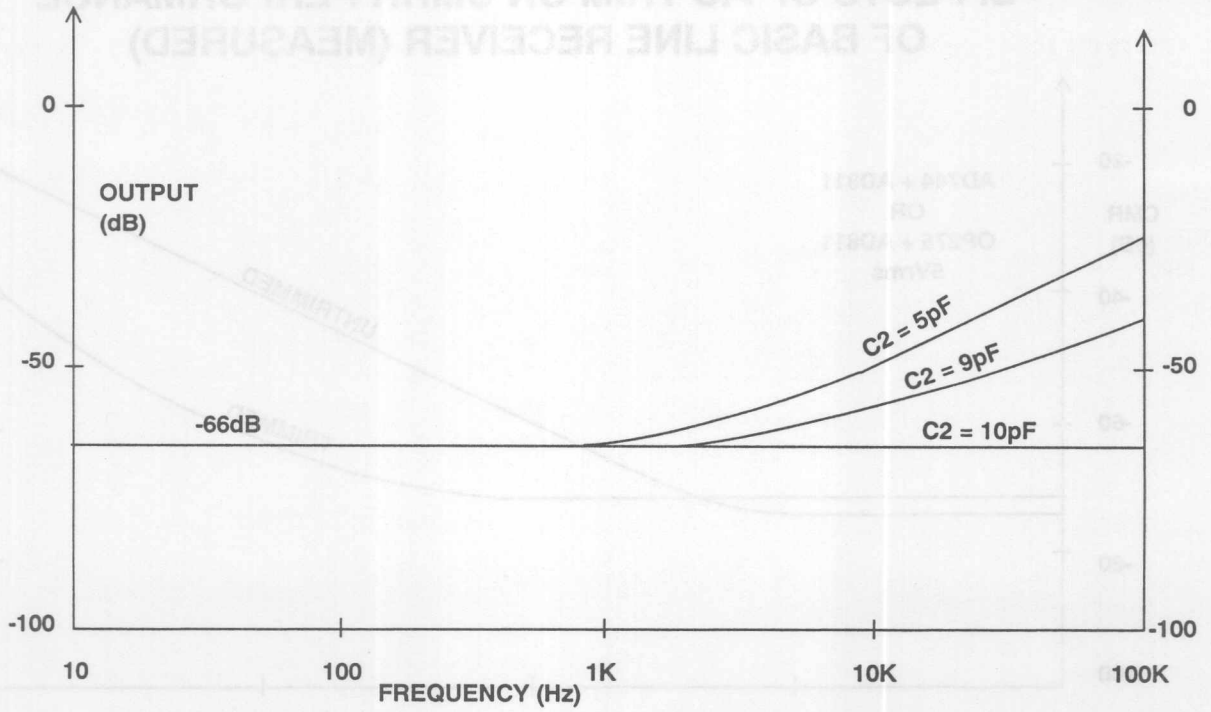


Figure 5.6

In this test R_1 is fixed at the 0.1% mismatch point, making the DC CMR 66dB (as before). C_2 is 5pF at the top curve, and steps up in value to 10pF for the bottom curve (best AC balance). As can be seen, this capacitive unbalance starts to degrade the CMR at progressively lower frequencies for larger capacity imbalances.

MEASURED PERFORMANCE

The circuit of Figure 5.4 is not just hypothetical, it was built with the components as noted, and lab results show good agreement with the simulations. With the circuit as shown, the user has an option of operating U1 either buffered or unbuffered, by the optional use of the U2 follower. If an AD811 is used here as noted, the circuit has an output capability of more than 100mA, making it useful with lower output drive ICs for U1 such as the AD744. Or, if a huskier output device such as the OP-275 is used for U1, the need for a buffer is more moot, since the OP-275 by itself is rated to drive 600Ω loads. For loads appreciably lower than 600Ω, use of the U2 buffer will preserve the low distortion typical of this circuit. (Note that if an AD811AN is used for U2 above ±12V, a heat sink such as Aavid 5801 is suggested).

CMR performance of the circuit is shown in Figure 5.7, for conditions of trimmed and untrimmed for AC, and a 5Vrms CM input, with ±15V supplies.

The upper curve represents CMR performance of either the OP-275 or the AD744 (both buffered) with a 0.1% ratio match type T914 25kΩ network, and *no* capacitive trimming. The stray capacity mismatches of the breadboard limit the high frequency CMR to much less than the DC level, with CMR deteriorating above 1kHz. With trimmed 10pF

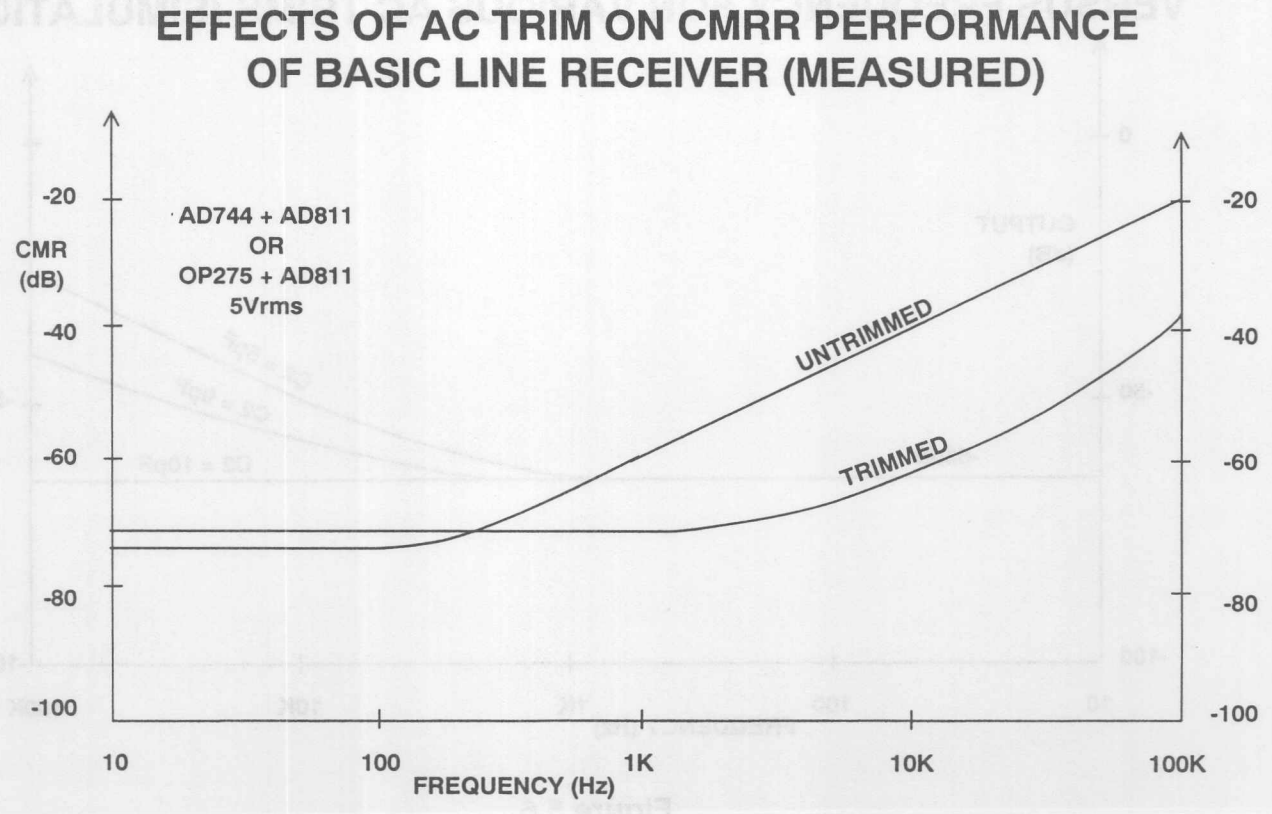


Figure 5.7

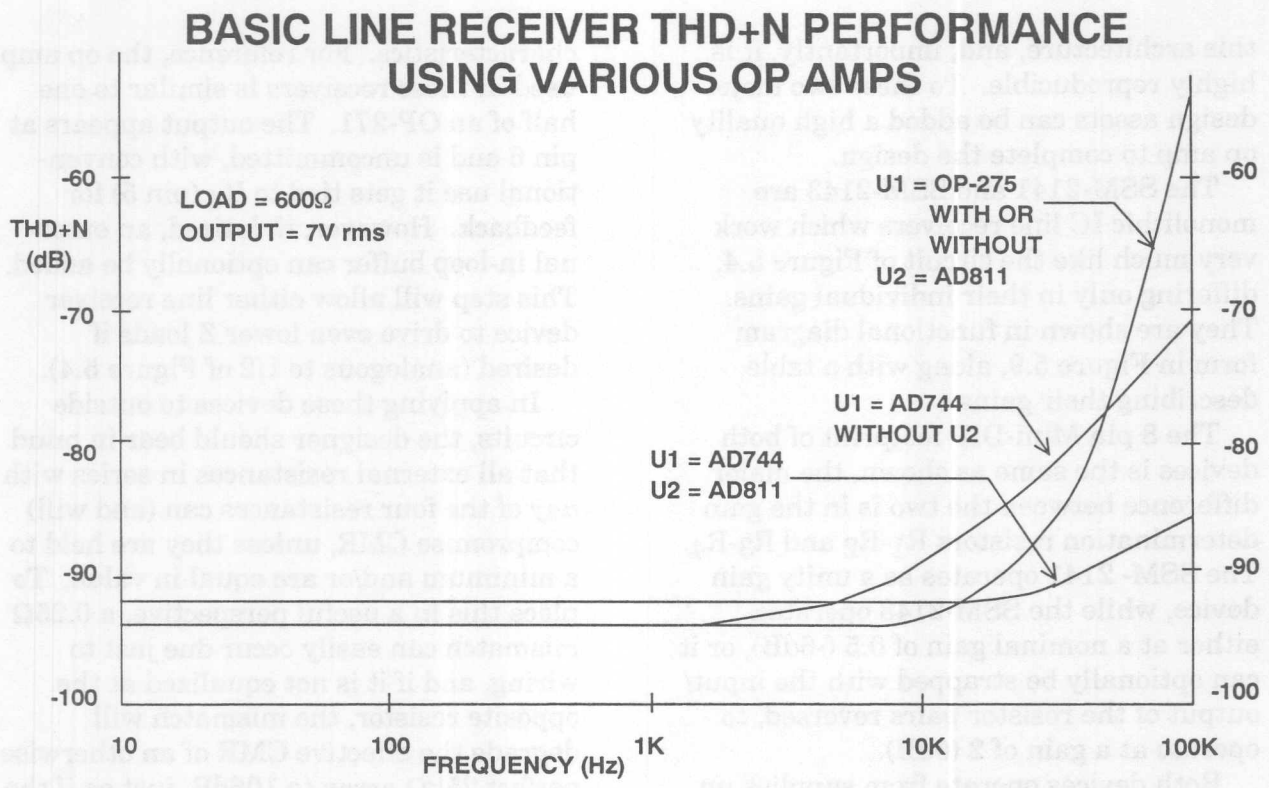


Figure 5.8

capacitors added, CMR is preserved to above 10kHz. These CMR data show that both DC and AC balance are necessary for best performance.

In terms of distortion, THD+N data at a 7Vrms level with a load of 600Ω is shown in Figure 5.8, with the two op amps operated both buffered and unbuffered.

The OP-275 shows little consequence operating without a buffer, while the AD744 THD+N at high frequencies shows a rise from -86dB to -73dB at 100kHz. The distortion performance of both devices in this circuit is excellent.

INTEGRATED LINE RECEIVERS

An optimum way to build the line receiver circuit under discussion is via *monolithic* technology. With this method, using a high performance op amp plus a trimmed thin film resistor network with low parasitics, all pertinent aspects which impact line receiver performance are under direct control during manufacture. As has been observed, getting the highest performance from an op amp plus resistor network approach such as Figure 5.4 demands either precise control of a single network, or circuit-by-circuit trim of one of the four resistors for the optimum ratio. In addition to this low frequency CM trim, there must also be an AC trim. These factors make the duplication of a high performance version of this circuit expensive, time consuming, and demanding of both instrumentation and operator skills.

In contrast, the precise trim of thin film networks is one of the strengths of the AD manufacturing processes. Low parasitic capacitance can be designed into

this architecture, and, importantly, it is highly reproducible. To these two major design assets can be added a high quality op amp to complete the design.

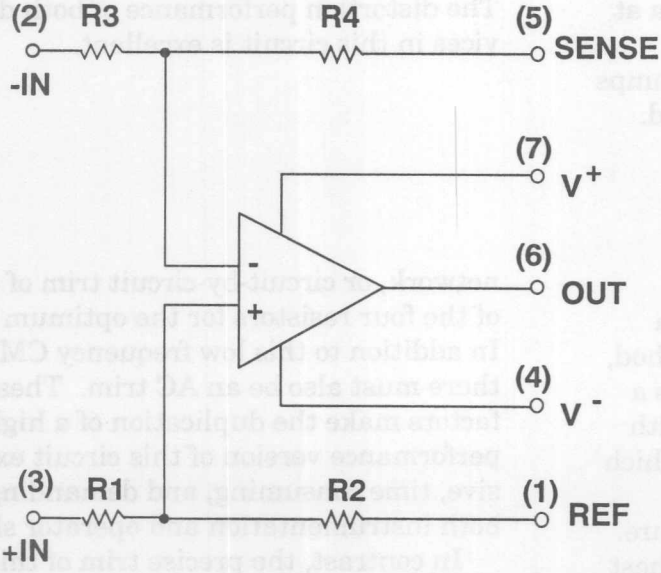
The SSM-2141 and SSM-2143 are monolithic IC line receivers which work very much like the circuit of Figure 5.4, differing only in their individual gains. They are shown in functional diagram form in Figure 5.9, along with a table describing their gains.

The 8 pin Mini-DIP footprint of both devices is the same as shown, the major difference between the two is in the gain determination resistors R_1-R_2 and R_3-R_4. The SSM- 2141 operates as a unity gain device, while the SSM-2143 operates either at a nominal gain of 0.5 (-6dB), or it can optionally be strapped with the input/output of the resistor pairs reversed, to operate at a gain of 2 (6dB).

Both devices operate from supplies up to ±18V, can drive 600Ω loads, and they have low distortion and excellent CMR characteristics. For reference, the op amp used in these receivers is similar to one half of an OP-271. The output appears at pin 6 and is uncommitted, with conventional use it gets tied to R_4 (pin 5) for feedback. However, if desired, an external in-loop buffer can optionally be added. This step will allow either line receiver device to drive even lower Z loads if desired (analogous to U2 of Figure 5.4).

In applying these devices to outside circuits, the designer should bear in mind that all external resistances in series with *any* of the four resistances can (and will) compromise CMR, unless they are held to a minimum and/or are equal in value. To place this in a useful perspective, a 0.25Ω mismatch can easily occur due just to wiring, and if it is not equalized at the opposite resistor, the mismatch will degrade the effective CMR of an otherwise perfect 25kΩ array to 106dB, just as if the internal resistors had drifted. In practice then, these circuits are best fed from low

SSM-2141/SSM-2143 LINE RECEIVER



DEVICE	R1, R2	R3, R4	GAIN
SSM-2141	25kΩ	25kΩ	OdB
SSM-2143	12kΩ	12kΩ	-6dB

Figure 5.9

SSM-2141 AUDIO LINE RECEIVER CMR AND THD + N PERFORMANCE

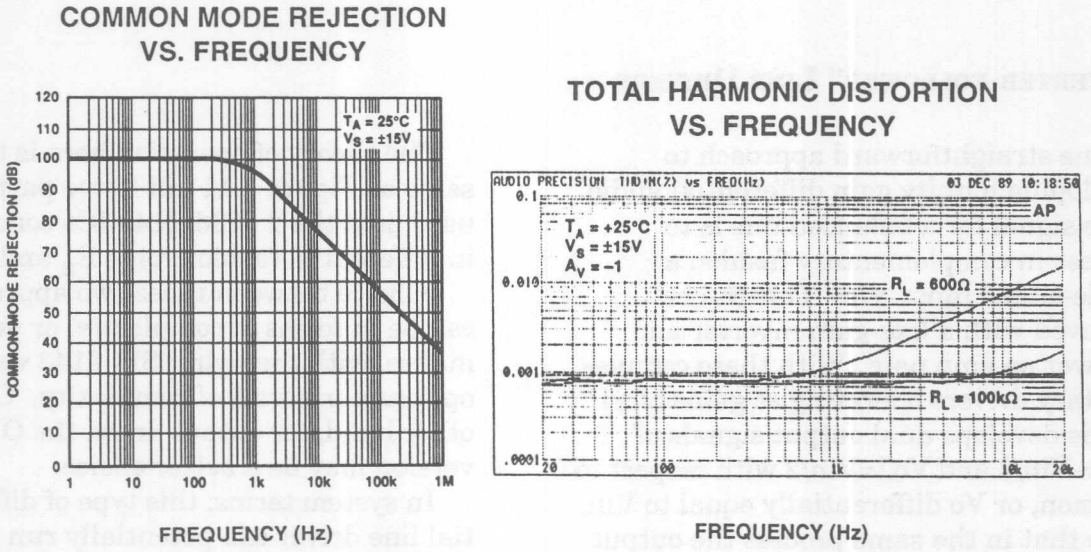


Figure 5.10

impedance and truly balanced sources, and all interfacing to them should be done mindful of this goal.

Perhaps the most outstanding attribute of these devices is their CMR performance, shown in Figure 5.10 (these data are for the SSM-2141, but the SSM-2143 is similar). For the SSM- 2141 the DC-to-1kHz CMR is typically 100dB, and even at 10kHz it is still about 80dB. The SSM-2143 (not shown), using lower resistor values, has a somewhat lower typical CMR of 90dB, but maintains this to about 10kHz. The SSM-2141 THD+N performance also shown in Figure 5.10 is also very good for both 600Ω and 100kΩ loads.

With a companion differential line driver (next section), these two line receivers allow convenient as well as flexible interfacing between points in audio systems, as well as other instrumentation up to 100kHz. However, they both are also more generally useful as flexible gain blocks within a system, not necessarily requiring the full CM performance aspects. For example, they are useful as either precise inverting or non-inverting gains blocks, due to the very accurate internal resistor ratios. With the SSM-2141 typical gain accuracy of 0.001%, very precise, single chip unity gain inverters and summers can be built at low overall cost.

LINE DRIVERS

Unlike the case for the differential line receiver, a standard circuit topology for differential line drivers is not quite as clear-cut. Two circuit types are discussed in this sections, with their contrasts in performance and complexity.

"INVERTER-FOLLOWER" LINE DRIVERS

One straightforward approach to developing a unity gain differential audio drive signal for a balanced line is to process in complementary fashion a single-ended input Vin. This can be achieved with a like-gain inverter and follower op amp pair. With these complementary drivers operating at gains of ±1/2, this develops dual output signals of Vo1=-Vin/2 and Vo2=Vin/2 with respect to common, or Vo differentially equal to Vin. Note that in the same process the output Vo can also be scaled up if desired, since there is an inherent 6dB gain in headroom with differential operation.

This "inverter/follower" driver can be easily accomplished with a dual op amp such as the OP-275, and a set of discrete resistors (or a 20kΩ/10kΩ thin film network), as shown in Figure 5.11.

Here U1A provides the gain of -1/2 channel, while U1B operates at a gain of +1/2. The differential output signal across the balanced line is Vin for high impedance loads, and the differential output impedance is 600W. Output current drive can be increased by lowering the matched resistances R_a and R_b. Note that the similar values for the gain resistors around U1A/U1B make their purchase easy in either discrete or network form. Like gain values for the A and B circuit halves also provide matched bbandwidth and good balance versus frequency. Overall, this circuit is high in performance for its cost and reasonable simplicity.

Figure 5.12 shows a similar but more concise arrangement using a pair of SSM-2143 line receivers as integral precision amplifiers to develop the ±Vin signals.

The theory of operation here is the same as Figure 5.11 but fewer parts are used, just the 2 SSM-2143 ICs connected in differential fashion, plus R_a and R_b.

Choice between these two approaches can be in terms of complexity, or performance, with the twin SSM-2143 version optimum in terms of complexity. On the other hand, for output drive, the OP-275 version may be a better choice.

In system terms, this type of differential line driver can potentially run into application problems, and should be used with some caveats in mind. In reality, these two driver circuits are mirror-imaged single-ended drivers, and they produce voltage output signals with respect to the source (Vin) common point.

At the load end of a cable being driven, if the stage receiving the signal is a differential input with high impedance (i.e., like the SSM-2141 or SSM-2143), there is no real problem in application for either of these two line driver circuits. Note however that R_a must be *closely* matched to R_b for best CMR, if a 25kΩ receiver is to be used. This suggests low values for R_a and R_b, such as 100Ω or less.

However, one side of the differential output from Figure 5.11 or Figure 5.12 *cannot be grounded without side effect.* This is because the source drive Vo is *not* truly floating, as would be in the case of a transformer winding. In this application sense, these two circuits are *pseudo differential*, and as such they shouldn't be used indiscriminately. Nevertheless, within small and defined systems they do have an obvious advantage of simplicity,

INVERTER/FOLLOWER DIFFERENTIAL LINE DRIVER USING OP-275 DUAL OP AMP

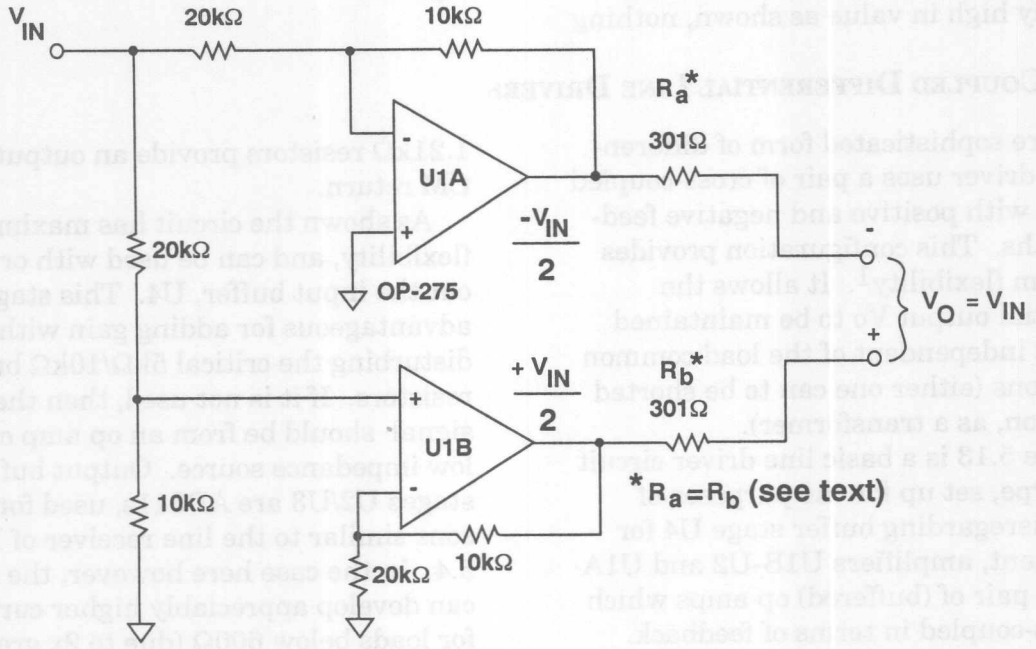


Figure 5.11

INVERTER/FOLLOWER DIFFERENTIAL LINE DRIVER USING SSM-2143 GAIN BLOCKS

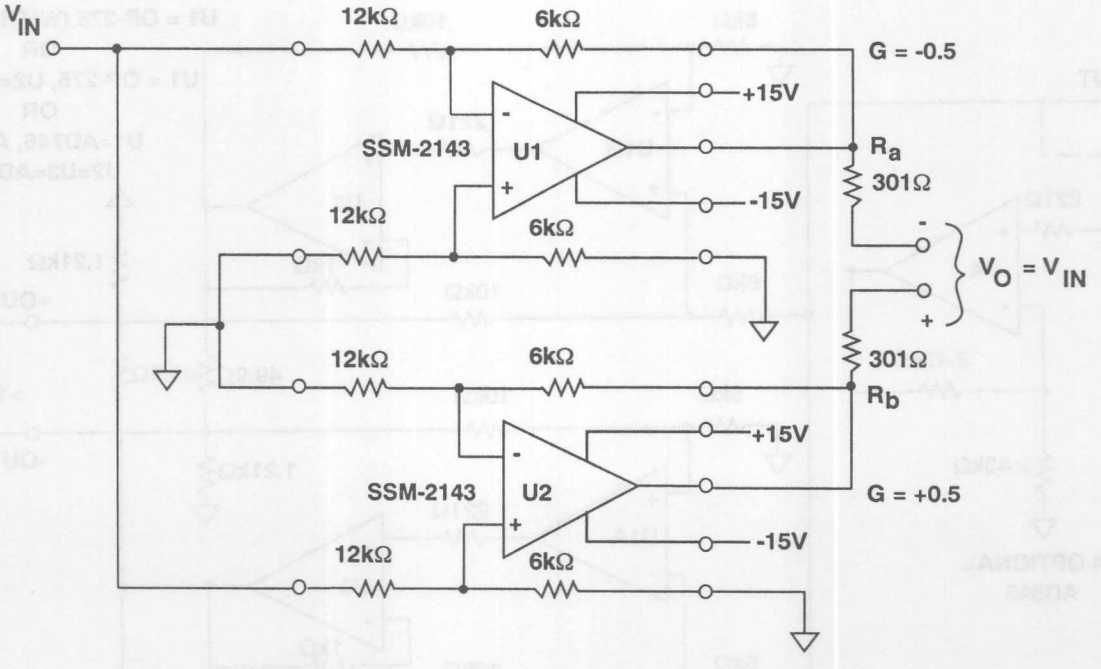


Figure 5.12

and can achieve high performance in signal fidelity. Note that with the matched source resistances R_a and R_b relatively high in value as shown, nothing will be damaged even if the output is shorted... other than a loss of half the signal!

CROSS-COUPLED DIFFERENTIAL LINE DRIVERS

A more sophisticated form of differential line driver uses a pair of cross-coupled op amps with positive and negative feedback paths. This configuration provides maximum flexibility[1]. It allows the differential output Vo to be maintained constant independent of the load common connections (either one can to be shorted to common, as a transformer).

Figure 5.13 is a basic line driver circuit of this type, set up for the purposes of tests. Disregarding buffer stage U4 for the moment, amplifiers U1B-U2 and U1A-U3 are a pair of (buffered) op amps which are cross-coupled in terms of feedback. Each amplifier has a precision four resistor bridge network for feedback, and feeds a differentially connected load R_L through the 49.9Ω build out resistors. The two 1.21kΩ resistors provide an output DC CM return.

As shown the circuit has maximum flexibility, and can be used with or without the input buffer, U4. This stage is advantageous for adding gain without disturbing the critical 5kΩ/10kΩ bridge resistors. If it is not used, then the input signal should be from an op amp or other low impedance source. Output buffer stages U2/U3 are AD811s, used for reasons similar to the line receiver of Figure 5.4. In the case here however, the output can develop appreciably higher currents for loads below 600Ω (due to 2x greater voltage swing). Again, heat sinking of the AD811AN is suggested above ±12V supplies.

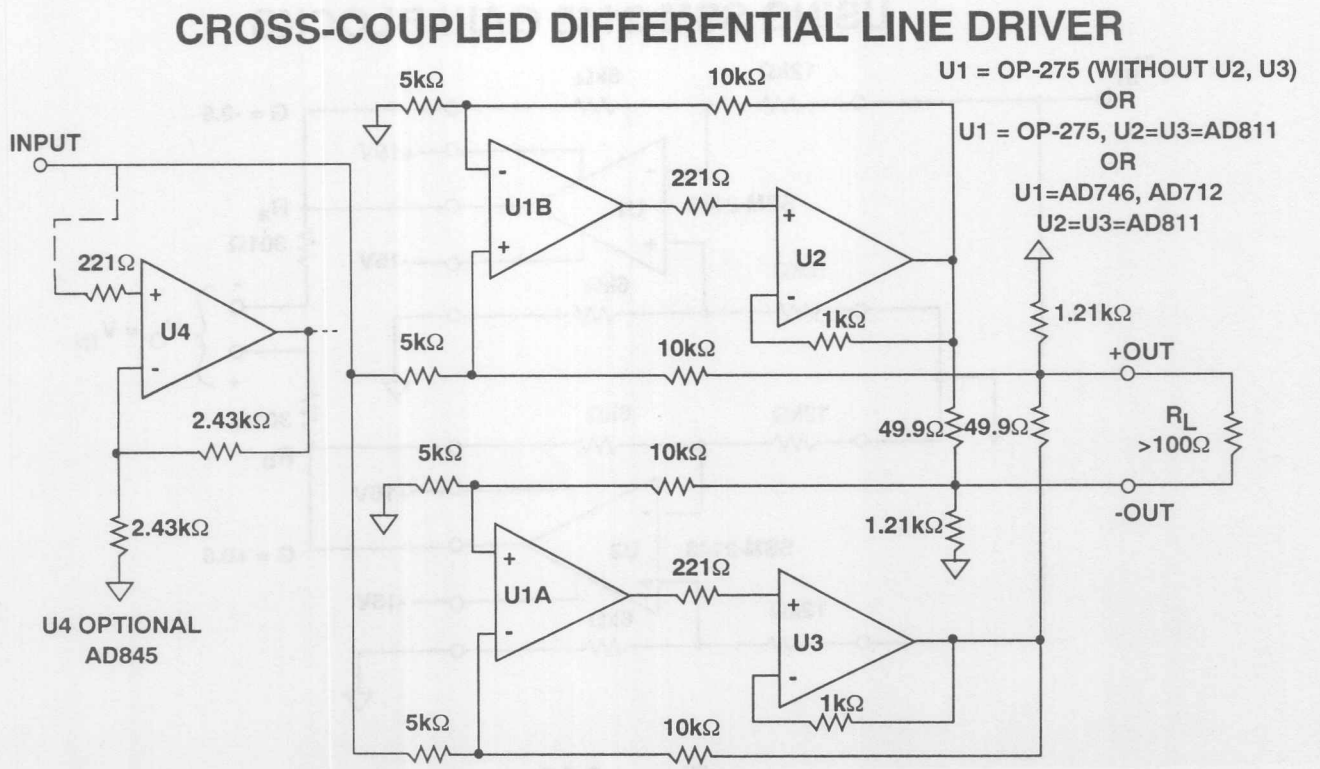


Figure 5.13

CROSS COUPLED DIFFERENTIAL LINE DRIVER THD+N PERFORMANCE USING VARIOUS OP AMPS

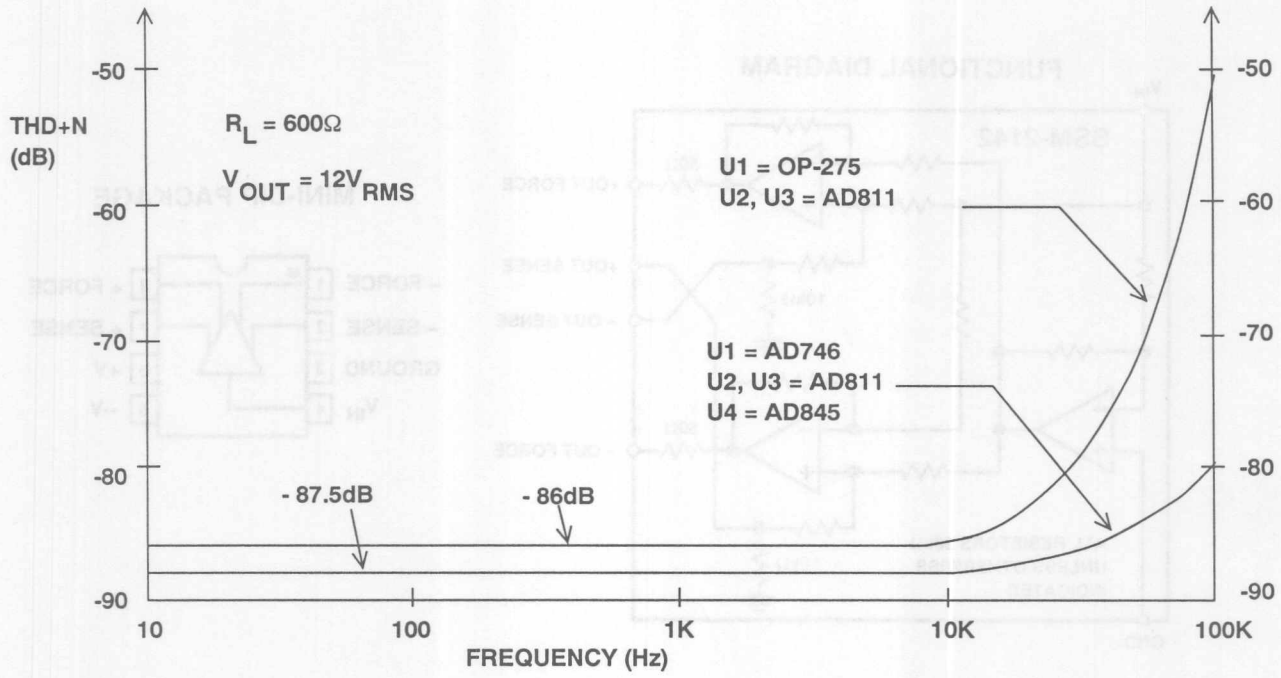


Figure 5.14

PERFORMANCE MEASUREMENTS

The circuit was tested with a variety of op amps used for U1 and U4, and with AD811 output buffers. The loading used was 600Ω, with an output swing of 12Vrms; Figure 5.14 shows the results of these tests.

For frequencies approaching 100kHz, the higher SR devices show the lowest distortion, as indicated by the AD845/ AD746 curve. With OP-275 devices used for U1 and U4, the distortion is higher at the high frequency extreme due to the device's 20V/μs SR, but is still very low below 20kHz. Other amplifiers useful in this configuration are the AD711 and AD712 (not shown). Or, OP-275 devices can be used *without* the output U2-U3 buffer, allowing a minimum component circuit.

Like the line receiver circuit, this line driver is quite critical as to resistor ratios, in fact it is even more demanding since it uses more of them. This factor tends to make it impractical just as it is shown, for any amplifier combination or performance level.

SSM-2142 LINE DRIVER CONFIGURATION

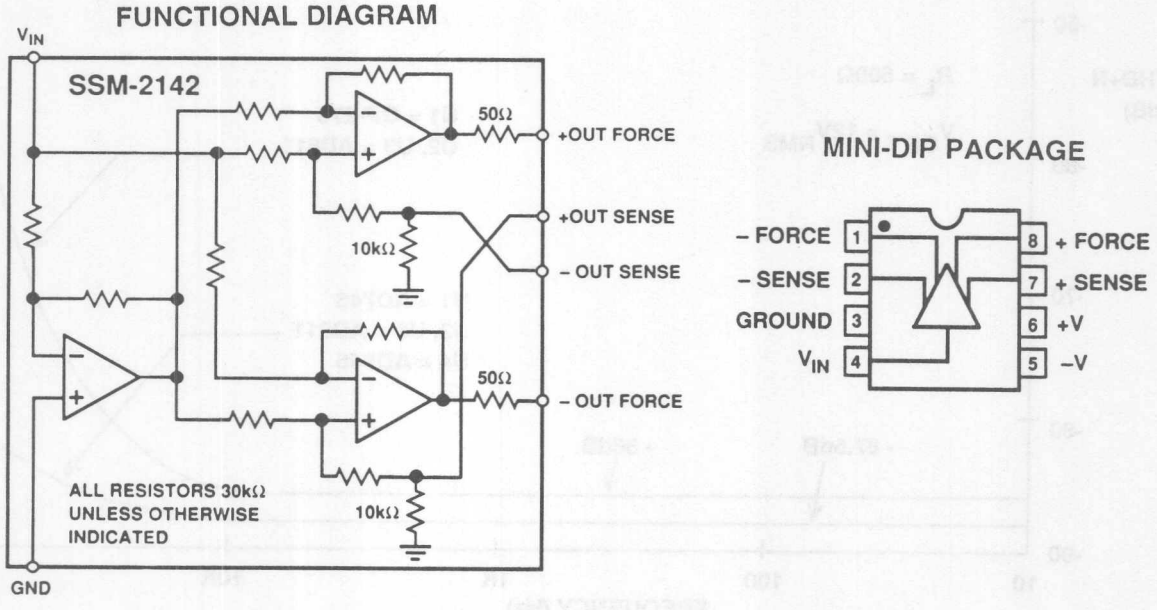


Figure 5.15

SYSTEM APPLICATION OF SSM-2142 LINE DRIVER WITH SSM-2141 OR SSM-2143 LINE RECEIVER

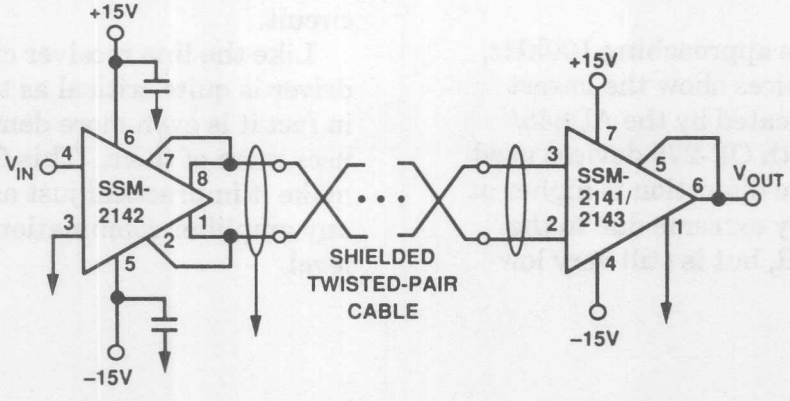


Figure 5.16

INTEGRATED LINE DRIVERS

On the other hand, the inherent features of laser trimmed monolithic technology can make a complex circuit such as the balanced line driver thoroughly practical. Like the SSM-2141 and SSM-2143 line receivers, applying these concepts to a driver circuit results in an efficient and useful IC. This product, the SSM-2142 balanced line driver, is shown in functional form in Figure 5.15. The multiple resistor array and trio of op amps shown in Figure 5.15a is packaged in the 8 pin miniDIP IC footprint of Figure 5.15b.

The SSM-2142 is designed for a single-ended to differential gain of 2 times, and in use can be simply strapped with the respective FORCE/SENSE pins tied together. In a system application, the SSM-2142 is used with either an SSM-2143 or an SSM-2141 line receiver, as shown in Figure 5.16, with the differential mode signal being transmitted via shielded twisted pair cable. This hookup comprises a complete single-ended to differential and back to single-ended transmission system, with noise isolation in the process.

With the use of the SSM-2143 gain of 0.5, the SSM-2142 gain of 2 is complemented, and the overall system gain is unity. If the SSM-2141 is used as the receiver, the gain is 2 overall. The THD+N performance of the unity gain SSM-2142/SSM- 2143 system is shown in Figure 5.17, for the conditions of a 5Vrms input/output signal, both with/without a 500' cable.

SSM-2142/SSM-2143 SYSTEM THD + N PERFORMANCE, Vin = Vout = 5V rms

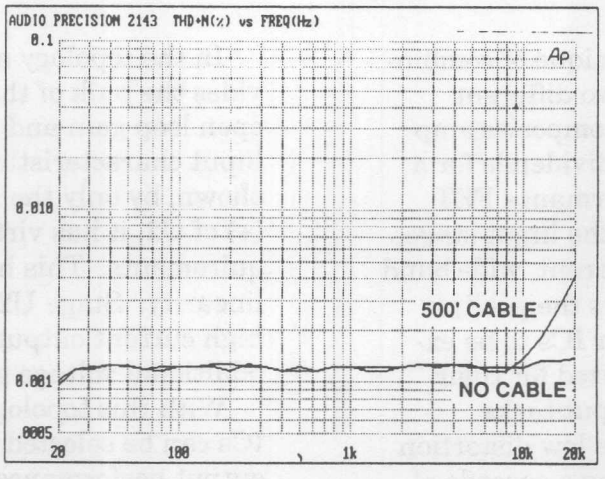


Figure 5.17

A HIGH PERFORMANCE AUDIO COMPOSITE LINE DRIVER STAGE

IC op amps of various types are often used as simple non- inverting gain stages to drive output lines. Typically, such line driver stages operate with voltage gains of 5-10 times (14-20 dB), work from medium-to-high impedance sources, and may drive difficult loads (600Ω or less, paralleled with several nF of capacitance). Ideally these goals are achieved with minimum non-linearity, providing low distortion operation over the full audio range.

However, this line stage has some requirements which basically conflict; it must drive low Z loads, but it cannot distort in doing so. It must operate with stability from medium to high Z sources, with minimal changes in DC offset, noise, and distortion as the source impedance changes (for example, operating from a level control). Unfortunately, high output currents can evoke thermal feedback in an op amp IC. When present, this result can also be a problem for both DC and low frequency AC signals.

A family of op amps with general specifications meeting these goals is the FET input category. Better quality FET op amps have good DC specs, namely low offset voltage. In addition, they have input bias currents of just a few pA (low enough that DC current related errors are generally negligible for source resistances below a megohm). The combination of these attributes makes net DC errors low enough that an entire line driver stage can be DC coupled. Sadly though, while many good to excellent FET input op amps exist, very few have outstanding audio performance driving 600Ω (or lower) loads.

For ±10V peak signals (7Vrms), a 600Ω load requires ±17mA. However, this Ohm's law criterion is too simplistic. Actually, these levels must be delivered with low levels of total harmonic distortion (THD), preferably 0.001% (10ppm) or less over the audio range. When lower full scale distortion is desired, and/or lower impedances must be driven, the optimum IC choice becomes more challenging.

COMPOSITE AMPLIFIERS TO THE RESCUE

Fortunately, the technique of combining the best aspects of two different amplifiers into a single composite amp structure produces real dividends for a line driver. A high performance FET input IC can be used as the input stage, combined with a high current, wide band output stage. This allows the positive features of two dissimilar ICs to be exploited, with each optimized for their respective input and output tasks.

Figure 5.18 shows this low distortion composite amplifier, using a cascade of two amplifier ICs. Two gain stages are used, U1 and U2, with individual performance selected as follows.

In the topology shown, stage U1 provides the bulk of the overall amplifier open loop gain and determines the basic input characteristics. With U1 loaded as shown, by only the high impedance input (+) of U2, it has virtually zero drive requirements. This helps to maximize linearity. Stage U2 provides primarily a high current output, but it also provides additional voltage gain via local feedback.

With this topology, individual U1/U2 ICs can be selected for unique input or output performance advantages. These are characteristics not available in one device, or, even when available, not cost effective.

LOW DISTORTION COMPOSITE AMPLIFIER

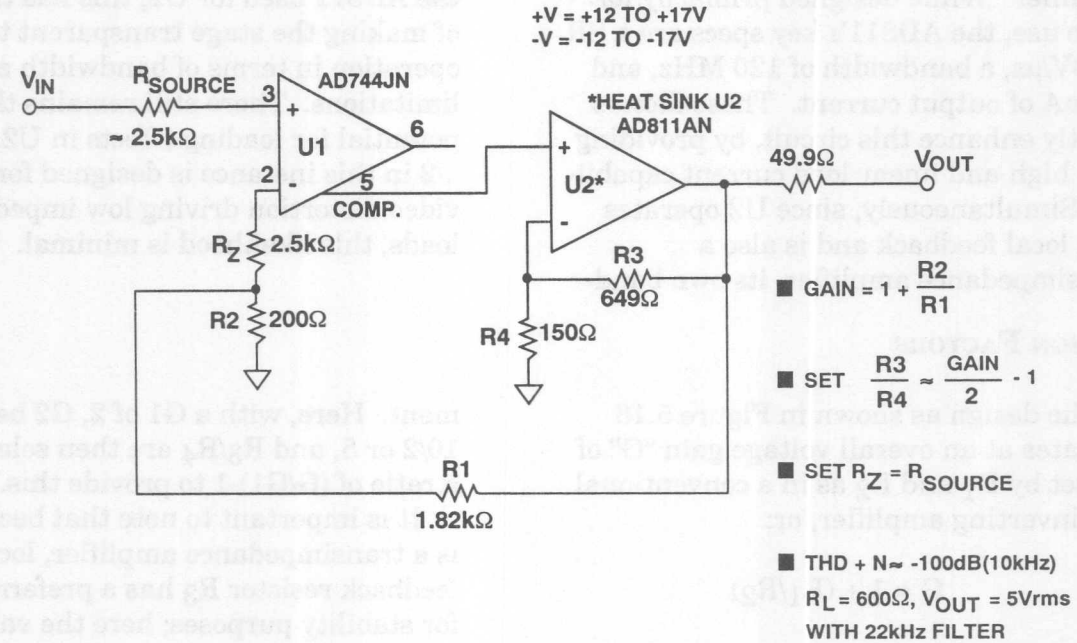


Figure 5.18

CIRCUIT DESCRIPTION

In this application U1 is an AD744, a high SR, fast settling FET input op amp with a basic THD of 0.001% below 10kHz (See Figures 16 and 20 of AD744 data sheet.) Note however, that since this characterization data is for a standard gain-of-10 follower, the net performance of the AD744 in this composite amplifier is appreciably better. This is due to several topology dependent factors.

One factor is that the U1 stage operates unloaded, which removes any output current related distortion within this stage. Another key point is that the overall gain bandwidth and SR of U1 are boosted, by a factor equal to the voltage gain of U2 (G2). For example, a 75V/μs SR in stage U1 becomes 75V/μs times G2, assuming the SR of U2 is appreciably higher (discussed further below).

A third ingredient which can lower frequency dependent distortion products is the use of input impedance compensation, which ideally balances both the R and C components seen at the input amp's two inputs (See the AD743 data sheet for a more detailed discussion of input impedance compensation in FET input op amps.) If used, this compensation serves to minimize the non-linear effects of FET input amplifier common mode capacitance. To implement this in Figure 5.18, an optional feedback resistance Rz is added, between R_1-R_2 and U1's (-) input. Rz is simply made equal to the nominal source impedance, Rsource (Rsource is shown here as the equivalent source resistance typical of a 50kΩ level control, operating at a low nominal level). For the performance tests below, Rz was not used.

U2 in this application is an AD811AN, a high performance transimpedance amplifier. While designed primarily for video use, the AD811's key specs are a SR 2500V/μs, a bandwidth of 120 MHz, and 100mA of output current. These factors greatly enhance this circuit, by providing both high and linear load current capability. Simultaneously, since U2 operates with local feedback and is also a transimpedance amplifier, its own bandwidth remains essentially high and constant as the U2 local gain changes. With the AD811 used for U2, this has the effect of making the stage transparent to overall operation in terms of bandwidth and SR limitations. There still remains the potential for loading effects in U2. But, as U2 in this instance is designed for low video distortion driving low impedance loads, this likelihood is minimal.

DESIGN FACTORS

The design as shown in Figure 5.18 operates at an overall voltage gain "G" of 10, set by R_1 and R_2 as in a conventional non inverting amplifier, or:

$$G = 1 + (R_1/R_2) \quad .$$

The individual stability requirements of U1 and U2 must also be met by the design. In this case U1 is stable at a gain G1, which is 2 (or more), therefore U2's gain G2 should be made equal to

$$G2 \leq G/(G1) \quad .$$

In the design process, by first considering G and G1, stage two gain G2 is made to satisfy the overall stability requirement. Here, with a G1 of 2, G2 becomes 10/2 or 5, and R_3/R_4 are then selected for a ratio of (G/G1)-1 to provide this.

It is important to note that because U2 is a transimpedance amplifier, local feedback resistor R_3 has a preferred value for stability purposes; here the value is 649Ω. The designer should fix R_3 at 649Ω, then set U2 stage gain via R_4, as:

$$R_4 = \frac{649\Omega}{(G/G1)-1} \quad .$$

(Note: R_4/R_3 are not as critical to gain as R_1/R_2, and they can be more loosely specified).

MEASURED PERFORMANCE

With these design and device selection factors, the composite amplifier performance is remarkable for its modest complexity. For a typical audio load of 600Ω, THD+N at an output level of 5Vrms is on the order of 10 ppm (-100dB) for frequencies below 20kHz, as shown in Figure 5.19. Note that lower operating levels may appear to have higher distortion, but will actually be more limited by the noise of the AD744.

In terms of operating hints, maximum output will be a function of the power supplies, and can approach 10Vrms with supplies of about ±17V supplies (both devices are rated for a maximum of ±18V). For supply voltages of ±12 or more however, a clip-on heat sink is recommended for U2, such as the Aavid 580100. For low impedance loads, the supplies should be well bypassed with large electrolytics, returned to the load common point.

Note that the general principles of this composite amp can be used for other devices in the U1/U2 positions, with different factors of optimization. For example, for lowest voltage noise from high Z sources, an AD745 (or AD743) device will be useful at U1.

COMPOSITE LINE AMPLIFIER THD + N PERFORMANCE, V_{out} = 5V rms, R_{load} = 600Ω, 22kHz Filter

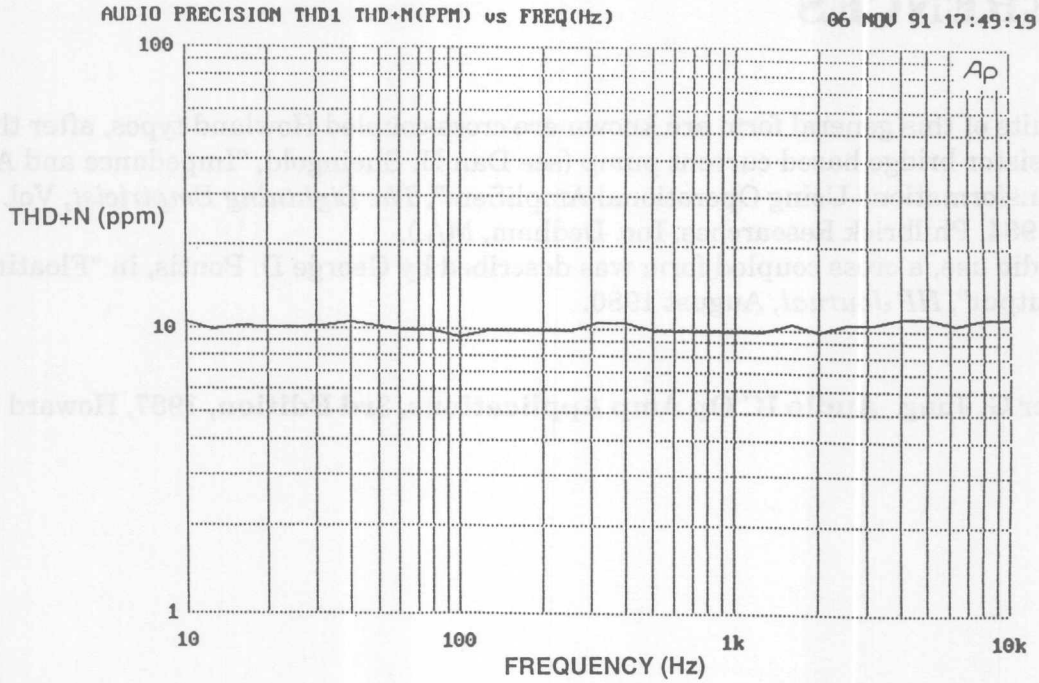


Figure 5.19

REFERENCES

[1] Circuits of this general form are known are cross-coupled Howland types, after the classic resistor bridge based current pump (see Dan H. Sheingold, "Impedance and Admittance Transformations Using Operational Amplifiers", *The Lightning Empiricist*, Vol. 12, #1, Jan. 1964, Philbrick Researches, Inc. Dedham, MA.).

For audio use, a cross coupled form was described by George D. Pontis, in "Floating a Source Output", *HP Journal*, August 1980.

[2] Walter G. Jung, **Audio IC Op Amp Applications, 3rd Edition**, 1987, Howard W. Sams.

SECTION VI
PASSIVE AND ACTIVE ANALOG FILTERING

- Introduction to Filter Design and Implementation
- Antialiasing Filter Design Example
- A Programmable State Variable Filter
- A Seven-Pole FDNR 20kHz Antialiasing Filter
- A 2MHz Biquad Bandpass Filter Using a 30MHz Quad Op Amp
- Practical Considerations In Filter Implementation:
  Passive Components, Active Components
- A 12MHz Sallen-Key Filter Using a Current Feedback Amplifier

SECTION VI

PASSIVE AND ACTIVE ANALOG FILTERING

HANK ZUMBAHLEN

INTRODUCTION TO FILTER DESIGN AND IMPLEMENTATION

Filtering is an important part of analog signal processing. Filtering can be used to reduce unwanted signals, limit bandwidth, help recover wanted signals, minimize aliasing in sampled data systems, and smooth the output of DACs. There are five classes of filters. *Lowpass* filters pass all frequencies below the cutoff frequency and block all frequencies above the cutoff frequency. *Highpass* filters are the inverse of the lowpass filters. They block the low frequencies and pass those above the cutoff frequency. *Bandpass* filters pass those frequencies between the lower cutoff and upper cutoff frequencies and reject all others. *Bandstop* filters are the inverse of bandpass filters. They reject frequencies between the cutoff frequencies and pass all others. *Allpass* filters pass all frequencies equally but introduce a predictable phase delay to the signal.

CLASSES OF PASSIVE AND ACTIVE FILTERS

- Lowpass
- Highpass
- Bandpass
- Bandstop
- Allpass

Figure 6.1

Traditional filters were passive, that is designed with no active elements. Active components were too costly and had very poor performance. Inductors, capacitors, and resisters were used to synthesize the filter. This approach has several difficulties because inductors become physically large for low frequency filters and have poor characteristics at high frequencies. There is a great deal of interaction between the different sections of the filter. Impedance levels must be precisely controlled. Close component tolerances are difficult to manufacture and maintain. Despite these limitations passive filters are still dominant at high frequencies, primarily due to dynamic performance limitations of op amps.

Active filters answer some of the limitations of the passive filter by offering isolation between stages and eliminating the need for inductors. Their use at high frequencies is limited by the dynamic performance of the active elements.

A filter can be specified in terms of five parameters as shown in Figure 6.4. The *cutoff frequency* F_c is the frequency at which the filter response leaves the error band (or the -3dB point for a Butterworth filter). The *stopband frequency* F_s is the frequency at which the minimum attenuation in the stopband is reached. The *passband ripple* A_{max} is the variation (error band) in the passband response. The *minimum passband attenuation* A_{min} defines the signal attenuation within the passband. The *order* M of the filter is the number of poles in the transfer function.

PASSIVE FILTERS

- Designed with Inductors, Capacitors, Resistors
- Large Inductors Required for Low Frequency Filters
- Interaction Between Filter Stages
- Component Tolerances Difficult to Manufacture and Maintain
- Still the Only Solution at High Frequencies Due to Active Component Limitations

Figure 6.2

ACTIVE FILTERS

- Eliminate Need for Inductors
- Good Interstage Isolation
- High Frequency Use Limited by Op Amp Dynamic Performance

Figure 6.3

KEY FILTER DESIGN PARAMETERS

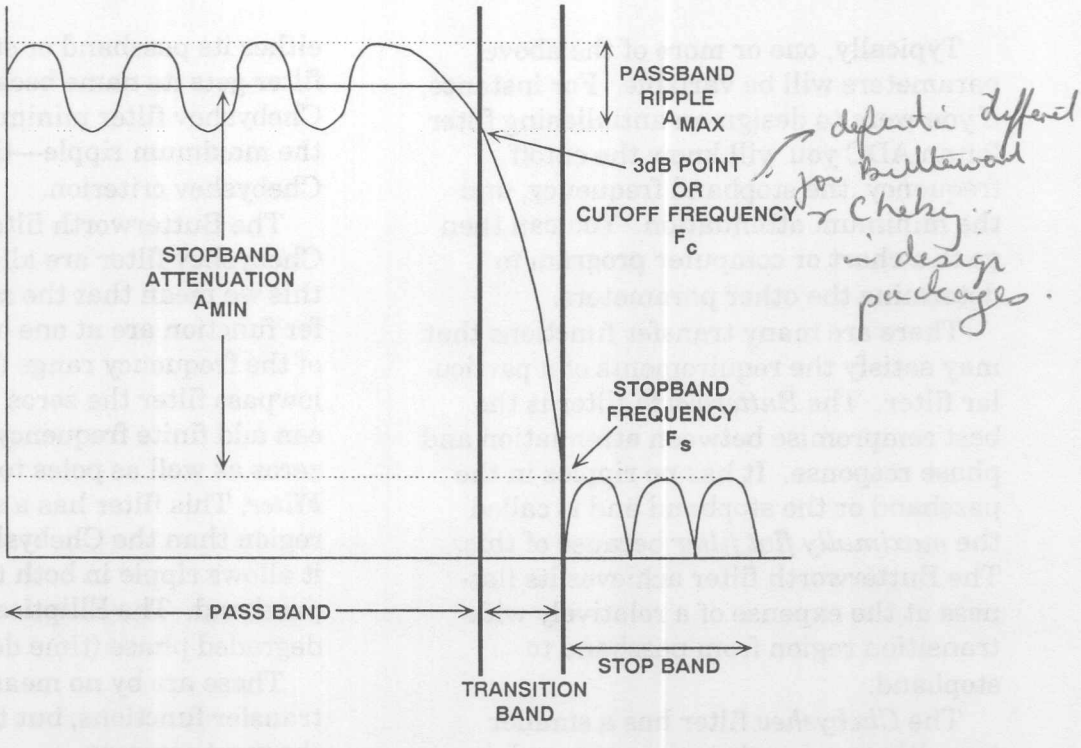


Figure 6.4

FILTER SPECIFICATIONS

- Cutoff Frequency, F_C
- Stopband Frequency, F_S
- Passband Ripple, A_{max}
- Stopband Attenuation, A_{min}
- Filter Order, M

Figure 6.5

Typically, one or more of the above parameters will be variable. For instance, if you were to design an antialiasing filter for an ADC you will know the cutoff frequency, the stopband frequency, and the minimum attenuation. You can then go to a chart or computer program to determine the other parameters.

There are many transfer functions that may satisfy the requirements of a particular filter. The *Butterworth* filter is the best compromise between attenuation and phase response. It has no ripples in the passband or the stopband and is called the *maximally flat filter* because of this. The Butterworth filter achieves its flatness at the expense of a relatively wide transition region from passband to stopband.

The *Chebyshev* filter has a smaller transition region than the same-order Butterworth filter, but it has ripples in either its passband or stopband. This filter gets its name because the Chebyshev filter minimizes the height of the maximum ripple—this is the Chebyshev criterion.

The Butterworth filter and the Chebyshev filter are all-pole designs. By this we mean that the zeros of the transfer function are at one of the two extremes of the frequency range (0 or ∞). For a lowpass filter the zeros are at $f = \infty$. We can add finite frequency transfer function zeros as well as poles to get an *Elliptical Filter*. This filter has a shorter transition region than the Chebyshev filter because it allows ripple in both the stopband and passband. The Elliptical filter also has degraded phase (time domain) response.

These are by no means all possible transfer functions, but they do represent the most common.

POPULAR FILTER DESIGNS

- **Butterworth: All Pole, No Ripples in Passband or Stopband, Maximally Flat Response**
- **Chebyshev: All Pole, Ripple in Passband, Shorter Transition Region than Butterworth for Given Number of Poles**
- **Elliptical: Ripple in Both Passband and Stopband, Shorter Transition Region than Chebyshev, Degraded Phase Response, Poles and Zeros**

Figure 6.6

Once the order of the filter and the specifications of filter have been determined, the design charts (see Reference 1) or computer programs are consulted, and the linear and quadratic factors of poles for the transfer function are determined. All filters, regardless of order, are made up of one- or two-pole sections. The single pole section is defined by its cutoff frequency, which is the -3dB point. The pole pair in a two-pole filter section is defined by its resonant frequency (F_o) and Q, which indicates the peaking of the section. Sometimes alpha (α) is used instead of Q ($Q=1/\alpha$).

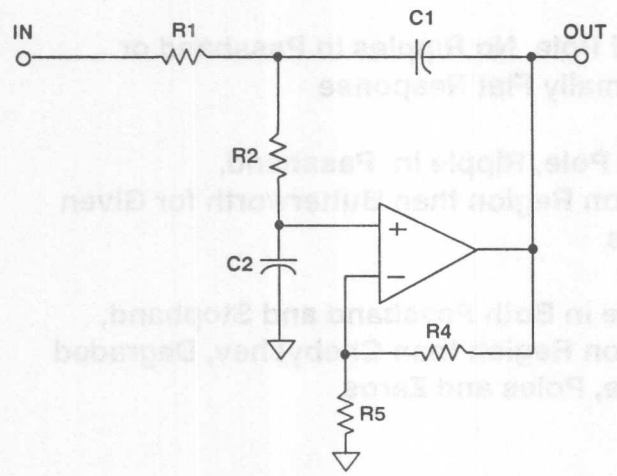
When the values of F_o and Q are defined, the configuration for the realization of the filter is then chosen: Butterworth, Chebyshev, or Elliptical.

For passive filters, these values, along with the filter characteristic impedance determine the inductor, capacitor, and resistor values.

For active filters, it is necessary to decide which of the realizations to use. The three most common are the *Sallen-Key* (voltage controlled voltage source), *multiple feedback*, and *state variable*. Each realization has its own advantages and disadvantages.

The Sallen-Key configuration shown in Figure 6.7 is the least dependent on the performance of the op amp, and the signal phase is maintained. For this filter the ratio of the largest resistor value to the smallest resistor value and the ratio of the largest capacitor value to the smallest capacitor value is low. The frequency term and Q terms are somewhat independent, but they are very sensitive to the gain parameter. The Sallen-Key is very Q-sensitive to element values for high Q sections. The design equations are given in Figure 6.7.

VOLTAGE CONTROLLED VOLTAGE SOURCE (SALLEN-KEY) REALIZATION



H = Circuit Gain Below Cutoff

α = Damping Ratio = 1/Q

F_O = Cutoff Frequency

Choose C1

$K = 2\pi F_O C1$

$M = \frac{\alpha^2}{4} + H - 1$

$C2 = M\ C1$

$R1 = \frac{2}{K\alpha}$

$R2 = \frac{\alpha}{2MK}$

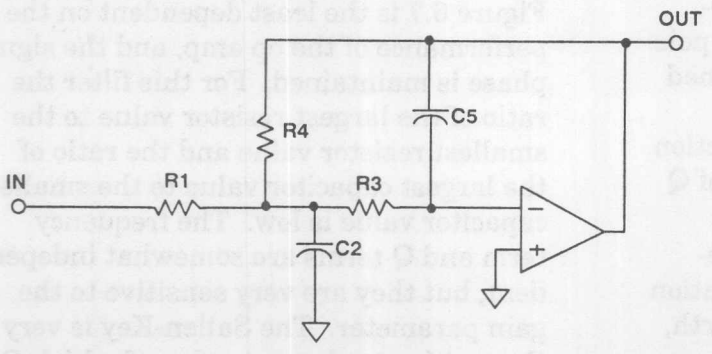
Choose R5

$R4 = R5(H - 1)$

For H = 1, R4 = 0, R5 = Open

Figure 6.7

MULTIPLE FEEDBACK REALIZATION



F_O = Cutoff Frequency

α = Damping Ratio = 1/Q

H = Absolute Value of Circuit Gain

Choose C5

$K = 2\pi F_O C1$

$C2 = \frac{4C5}{\alpha^2}(H + 1)$

$R1 = \frac{\alpha}{2HK}$

$R3 = \frac{\alpha}{2K(H + 1)}$

$R4 = HR1$

Figure 6.8

The multiple feedback filter shown in Figure 6.8 uses an op amp in the inverting configuration. The dependence on the op amp parameters is greater than in the Sallen-Key realization. It is hard to generate high Q sections due to the limitations of the open loop gain of the op amp. The maximum to minimum component value ratios are higher than in the Sallen-Key realization. The design equations are also given in Figure 6.8.

The state-variable realization shown in Figure 6.9 offers the most precise implementation, at the expense of many more circuit elements. All parameters can be adjusted independently, and lowpass, highpass, and bandpass outputs are available simultaneously. The gain of the filter is also independently variable. Since all parameters of the state variable filter can be adjusted independently, component spread is minimized. Also variations due to temperature and component tolerances are minimized. The design equations for the state variable filter are given in Figure 6.9.

Another active filter technique that has recently become more popular is the *Frequency Dependent Negative Resistor* (FDNR), which is a subset of the *General Impedance Converter* (GIC). In the FDNR the passive realization goes through a transformation by 1/s. Therefore inductors, whose impedance is sL, transform into a resistor of value L. Similarly, a resistor of value R becomes a capacitor of value R/s. A capacitor of impedance 1/sC transforms into a frequency dependent variable resistor, which is given the designation D. Its impedance is $1/s^2C$. The transformations to the FDNR configuration and the GIC implementation of the D element are given in Figure 6.10.

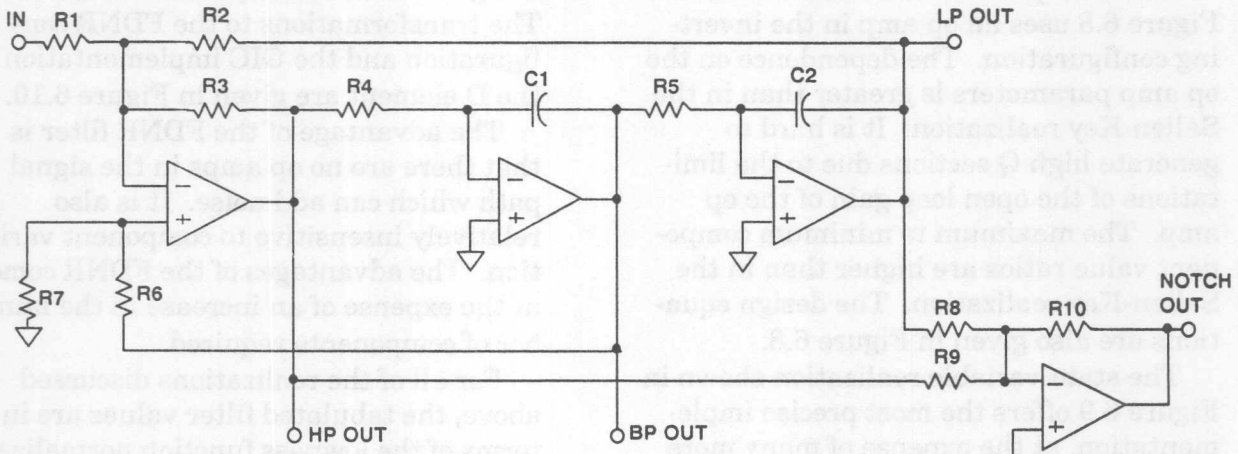
The advantage of the FDNR filter is that there are no op amps in the signal path which can add noise. It is also relatively insensitive to component variation. The advantages of the FDNR come at the expense of an increase in the number of components required.

For all of the realizations discussed above, the tabulated filter values are in terms of the lowpass function normalized to a frequency of 1 radian/second with an impedance level of 1Ω. To realize the final design, the filter values are scaled by the appropriate frequency and impedance.

Similarly, the lowpass prototype is converted to a highpass filter by scaling by 1/s in the transfer function. In practice this amounts to capacitors becoming inductors with a value 1/C and inductors becoming capacitors with a value of 1/L for passive designs. For active designs resistors become capacitors with a value of 1/R, and capacitors become resistors with a value of 1/C.

Transformation to the bandpass response is a little more complicated. If the corner frequencies of the bandpass are widely separated (by more than 2 octaves) the filter is made up of separate lowpass and highpass sections. In the case of a narrowband bandpass filter the design is much more complicated and is usually done using a computer program or design tables.

STATE VARIABLE REALIZATION



LOWPASS GAIN = -R2/R1

HIGHPASS GAIN = -R3/R1

$$\text{BANDPASS GAIN} = \frac{R6 + R7}{R1R7\left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}\right)}$$

$$F_O = \frac{1}{2\pi}\sqrt{\frac{R3}{R2 \cdot R4 \cdot R5 \cdot C1 \cdot C2}}$$

$$Q = \frac{1}{\alpha} = \frac{R6 + R7}{R7}\left(\frac{1}{\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}}\right)\sqrt{\frac{R4 \cdot C1}{R2 \cdot R3 \cdot R5 \cdot C2}}$$

FOR NOTCH FREQUENCY = F_Z

FOR $F_O = F_Z$, $\frac{R2 \cdot R9}{R3 \cdot R8} = 1$

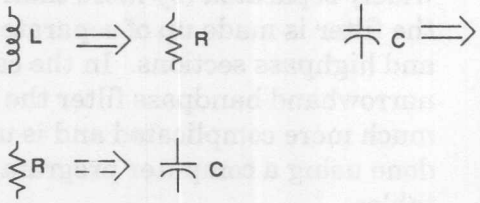
FOR $F_O > F_Z$, $\frac{R2 \cdot R9}{R3 \cdot R8} < 1$

FOR $F_O < F_Z$, $\frac{R2 \cdot R9}{R3 \cdot R8} > 1$

$$\frac{F_Z^2}{F_O^2} = \frac{R2 \cdot R9}{R3 \cdot R8}$$

Figure 6.9

FREQUENCY DEPENDENT NEGATIVE RESISTOR 1/S IMPEDANCE TRANSFORMATION



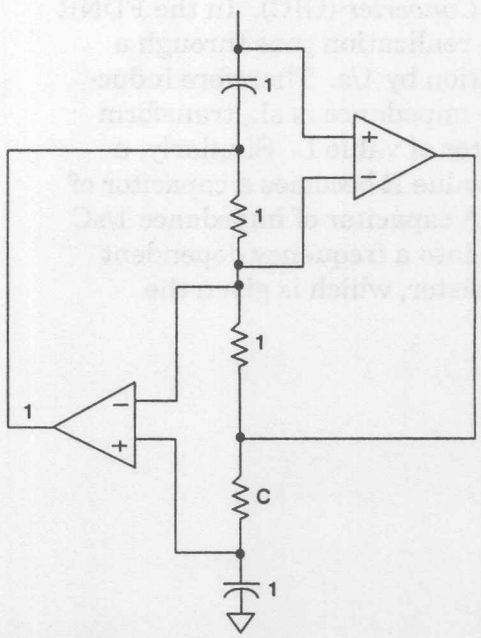


Figure 6.10

SOME ACTIVE FILTER REALIZATIONS

- Sallen-Key: Good Phase Response, Least Dependent on Op Amp Performance, Sensitive to Element Values for High Q Sections
- Multiple Feedback: Less Sensitive to Element Values, High Q Sections Difficult due to Op Amp Open Loop Gain Limitations
- State-Variable: Most Precise, More Components, All Parameters Independently Adjustable
- Frequency Dependent Negative Resistance (FDNR): Op Amps not in Signal Path, More Components, Relatively Insensitive to Component Variations

Figure 6.11

ANTIALIASING FILTER DESIGN EXAMPLE

We will now design passive and active antialiasing filters based upon the same specifications. The active filter will be designed in four ways: Sallen-Key, multiple feedback, state variable, and Frequency Dependent Negative Resistance (FDNR). We choose the Butterworth filter in order to give the best compromise between attenuation and phase response.

The specifications for the filter are as follows:

ANTIALIASING FILTER SPECIFICATIONS

- Cutoff Frequency F_C = 8kHz
- Stopband Attenuation F_S at 50kHz = 70dB
- Best Balance Between Attenuation and Phase Response Choose Butterworth Design
- From Design Charts, for f = 6.25 (50kHz/8kHz), M = 5

Figure 6.12

Consulting the design charts (Reference 1, p. 82), we see that for 70dB of attenuation at a frequency of 6.25 (50kHz/8kHz) a fifth order filter is required.

We now consult the tuning tables (Reference 1, p. 341) and find:

ALPHA AND F_0 VALUES FROM TUNING TABLES

Stage	Alpha	F_0
1	---	1.000
2	1.618	1.000
3	0.618	1.000

Figure 6.13

The first stage is a real pole, thus the lack of an alpha value. It should be noted that this is not necessarily the order of implementation in hardware. In general you would typically put the real pole last and put the second order sections in order of decreasing alpha (increasing Q).

For the passive design we will choose the zero input impedance configuration. From the design table (Reference 1, p. 313) we find the following normalized values for the filter:

NORMALIZED PASSIVE FILTER VALUES FROM TABLES

L1 = 1.5451 C2 = 1.6944

L3 = 1.3820 C4 = 0.8944

L5 = 0.3090

Figure 6.14

These values are for a 1 rad/second filter with a 1 Ω termination. To scale the filter we divide all reactive elements by the desired cutoff frequency, 8kHz (50265 rad/sec). We also need to scale the impedance. For this example, we choose a value of 1000 Ω. To scale the impedance we multiply all resistor and inductor values and divide all capacitor values by the impedance scaling factor. After scaling, the circuit looks like Figure 6.15.

For the Sallen-Key active filter, we use the design table shown in Figure 6.7. The values for C1 in each section are chosen to give reasonable resistor values. The implementation is shown in Figure 6.16. For the Sallen-Key realization to work correctly, it is assumed to have a zero-impedance driver and a return path for dc. Both of these criteria are approximately met when you use an op amp to drive the filter.

Figure 6.17 shows a multiple feedback realization of our filter. It was designed using the equations in Figure 6.8.

The state variable filter is shown in Figure 6.18, and the Frequency Dependent Negative Resistance (FDNR) realization is shown in Figure 6.19. In the conversion process from passive to FDNR, the D element is normalized for a capacitance of 1F. We then scale the filter to a more reasonable value (0.01μF in this case).

In all of the filters above the values shown are the exact calculated values. These exact values are rarely obtainable. We must therefore either substitute the nearest standard value or use series/parallel combinations. Any variation from the ideal values will cause a shift in the filter response characteristic, but often the effects are minimal. The computer can be used to evaluate these variations on the overall performance and determine if they are acceptable.

In active filter applications using op amps, the dc accuracy of the amplifier is often critical to optimal filter

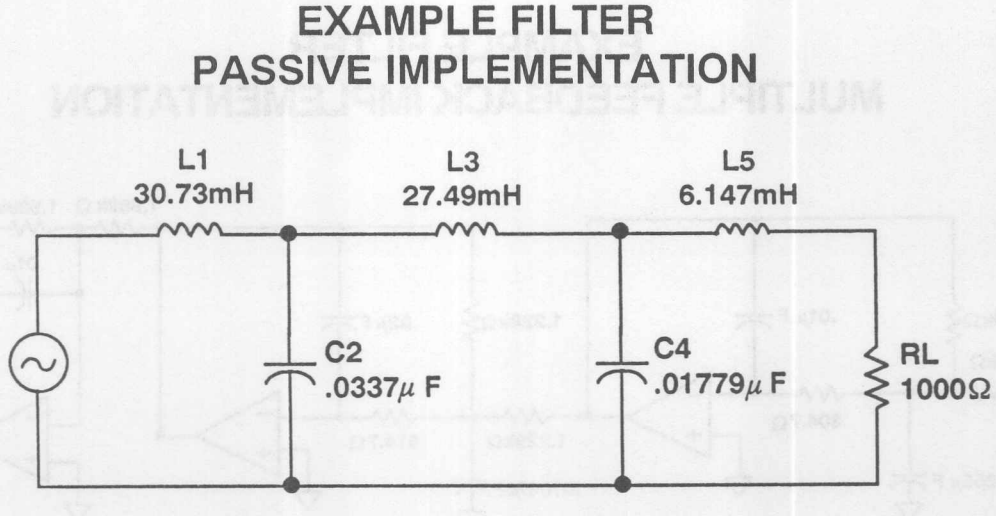


Figure 6.15

EXAMPLE FILTER
SALLEN-KEY IMPLEMENTATION

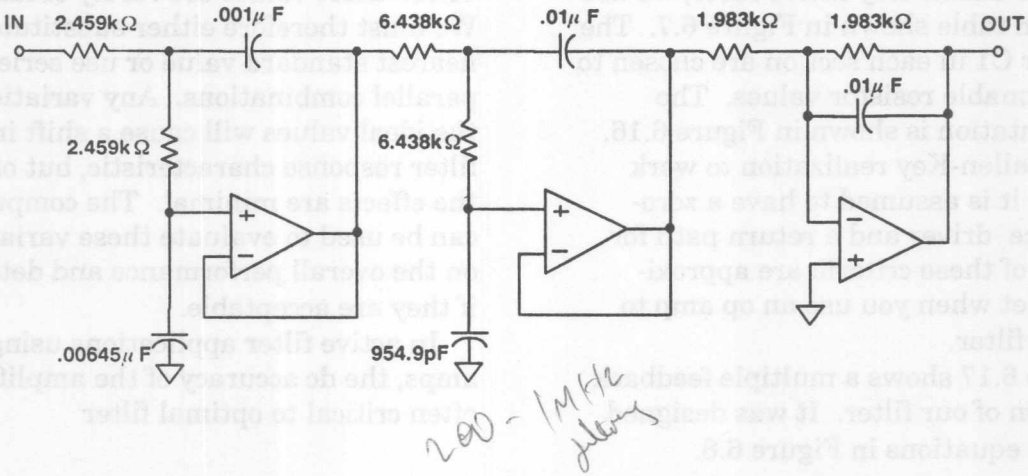


Figure 6.16

EXAMPLE FILTER
MULTIPLE FEEDBACK IMPLEMENTATION

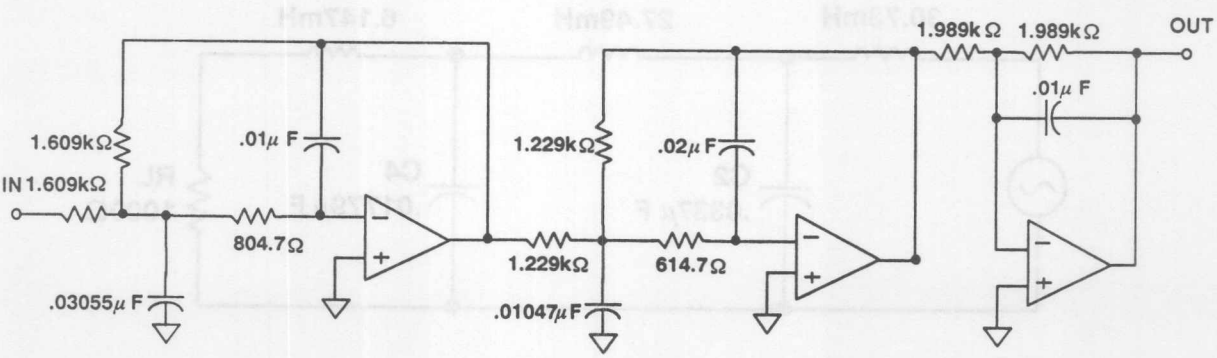


Figure 6.17

EXAMPLE FILTER
STATE VARIABLE IMPLEMENTATION

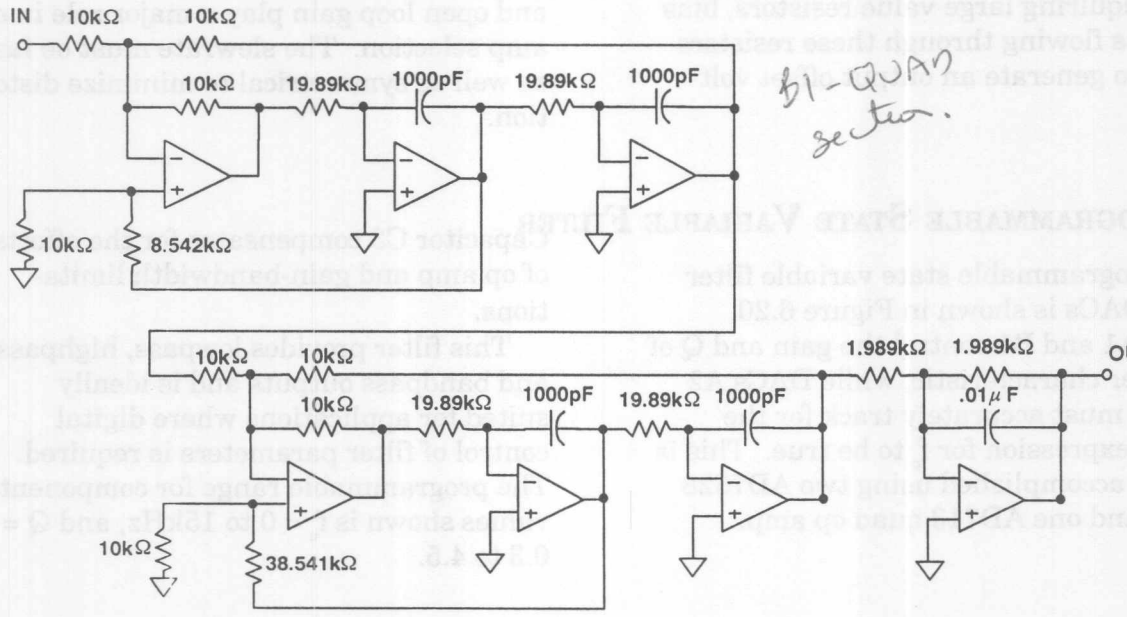


Figure 6.18

EXAMPLE FILTER
FDNR IMPLEMENTATION

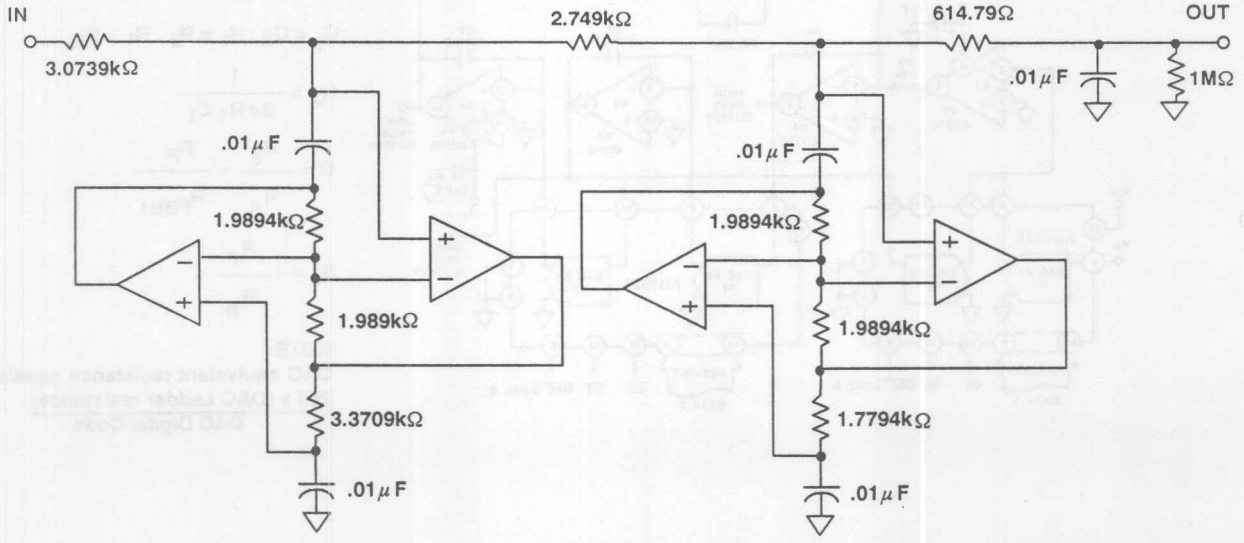


Figure 6.19

performance. The amplifier's offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value resistors, bias currents flowing through these resistors will also generate an output offset voltage.

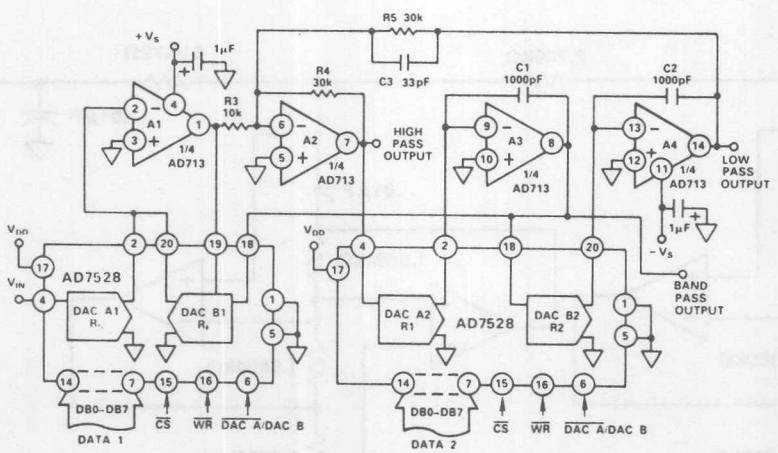
In addition, at higher frequencies, an op amp's dynamics must be carefully considered. Here, slewrate, bandwidth, and open loop gain play a major role in op amp selection. The slewrate must be fast as well as symmetrical to minimize distortion.

A PROGRAMMABLE STATE VARIABLE FILTER

A programmable state variable filter using DACs is shown in Figure 6.20. DACs A1 and B1 control the gain and Q of the filter characteristic, while DACs A2 and B2 must accurately track for the simple expression for f_c to be true. This is readily accomplished using two AD7528 DACs and one AD713 quad op amp. Capacitor C3 compensates for the effects of op amp and gain-bandwidth limitations.

This filter provides lowpass, highpass, and bandpass outputs and is ideally suited for applications where digital control of filter parameters is required. The programmable range for component values shown is f_c = 0 to 15kHz, and Q = 0.3 to 4.5.

A PROGRAMMABLE STATE VARIABLE FILTER CIRCUIT



CIRCUIT EQUATIONS

$$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$$

$$f_C = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_0 = -\frac{R_F}{R_S}$$

NOTE:
DAC equivalent resistance equals
256 x (DAC Ladder resistance)
DAC Digital Code

Figure 6.20

SEVEN-POLE FDNR 20kHz ANTIALIASING FILTER

Figure 6.21 shows a 7-pole antialiasing filter for a 2x oversampling (88.2kSPS) digital audio application. This filter has less than 0.05dB passband ripple and 19.8 ± 0.3μs delay, dc-20kHz. The filter will handle a 5V rms signal (V_S = ±15V) with no overload at any internal nodes. The frequency response of the filter is shown in Figure 6.22.

20kHz FDNR AUDIO ANTIALIASING FILTER

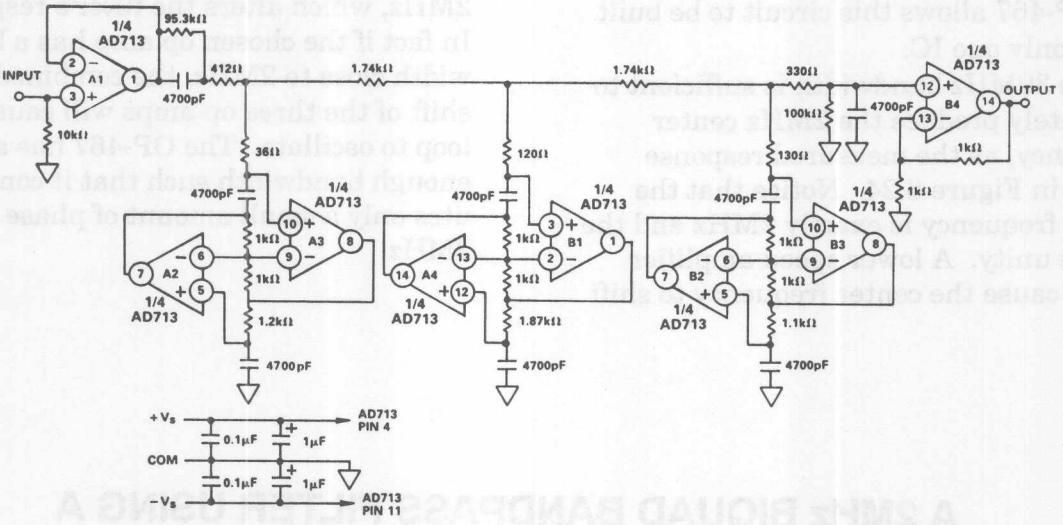


Figure 6.21

AUDIO ANTIALIASING FILTER RESPONSE

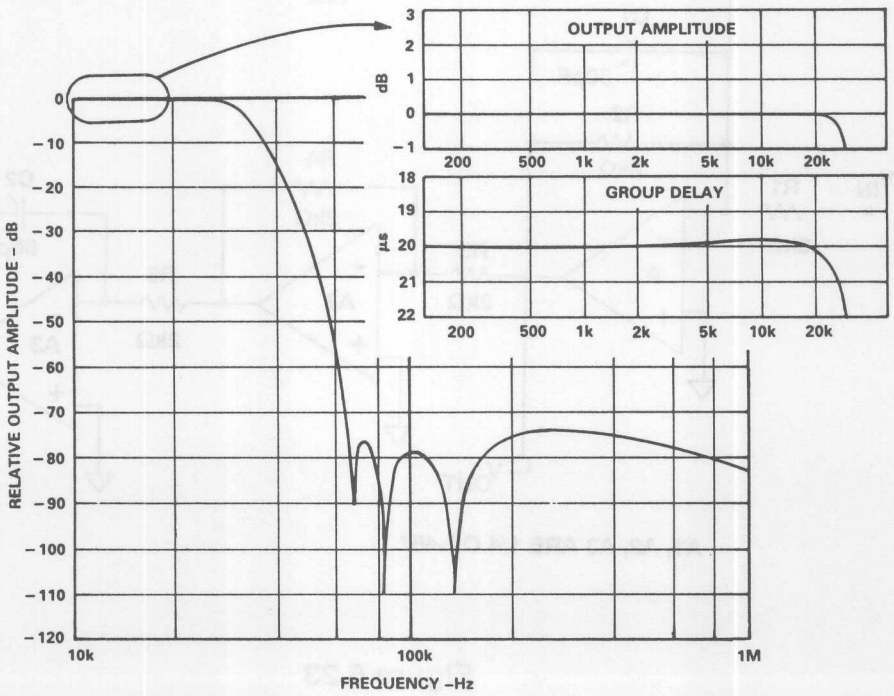


Figure 6.22

2 MHz BIQUAD BANDPASS FILTER USING A 30MHz QUAD AMPLIFIER

Figure 6.23. shows a circuit for a biquad bandpass filter with a 2MHz center frequency. This type of filter is often used in ultrasound receivers to detect a 2MHz signal while rejecting all others. The OP-467 is ideal for such an application because of its wide bandwidth and quad package. With four amplifiers, the OP-467 allows this circuit to be built using only one IC.

The 30MHz bandwidth is sufficient to accurately produce the 2MHz center frequency, as the measured response shows in Figure 6.24. Notice that the center frequency is exactly 2MHz and the gain is unity. A lower speed amplifier would cause the center frequency to shift significantly. For example, using an op amp with a 10MHz gain-bandwidth product results in 20% shift in the center frequency to 1.6MHz, even though the same component values are used. When the bandwidth is too close to the filter's center frequency, the amplifiers' internal phase shift causes excess phase shift at 2MHz, which alters the filter's response. In fact if the chosen op amp has a bandwidth close to 2MHz, the combined phase shift of the three op amps will cause the loop to oscillate. The OP-467 has a high enough bandwidth such that it contributes only a small amount of phase shift at 2MHz.

A 2MHz BIQUAD BANDPASS FILTER USING A 30MHz QUAD AMPLIFIER

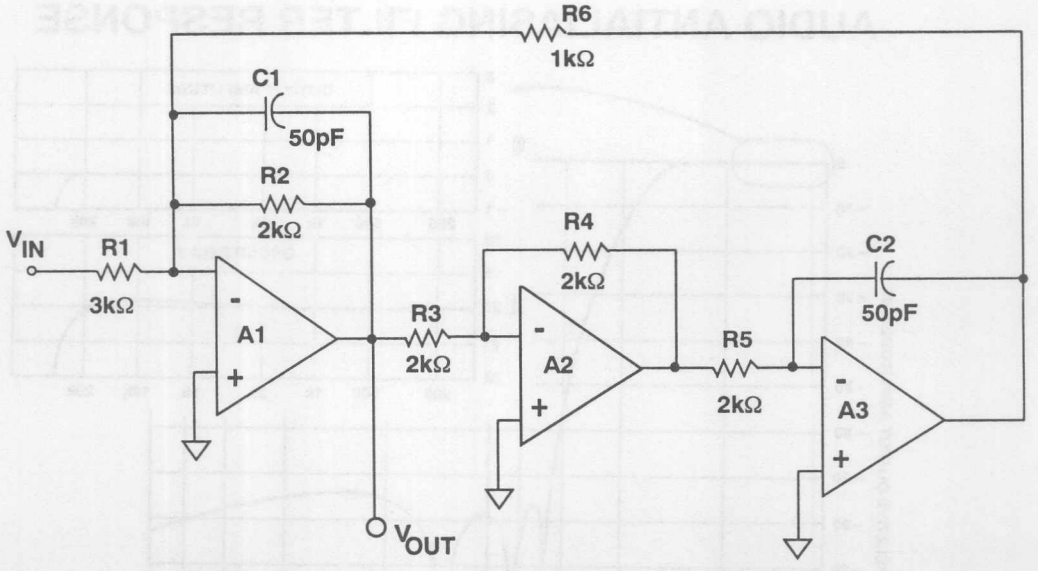


Figure 6.23

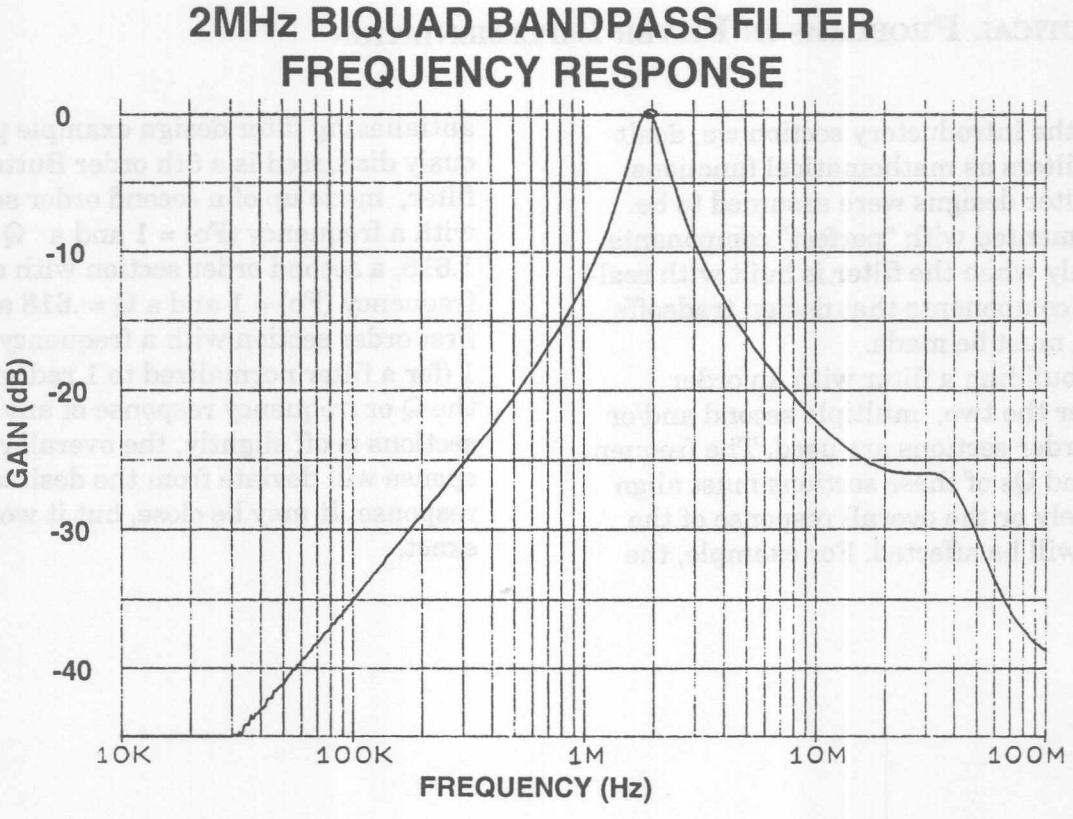


Figure 6.24

Careful consideration must be given to the layout of this circuit as with any high speed circuit. As mentioned above, if the phase shift is too large at 2MHz, the filter's response will be altered, or worse, it will oscillate. Any parasitic capacitance will cause additional phase shift. Thus care must be taken to minimize this capacitance, especially on the inverting inputs to the amplifiers. The traces connected to this node should be kept short and the ground plane removed from this area.

The OP-467 allows the entire circuit to be built with only one package, which was not possible before. Additionally, the one additional op amp in the package can be used elsewhere in the circuit to provide gain or buffering. If the op amp is not used, then it should be configure as a voltage follower with the positive input grounded and no load on the output. This ensures that it will not oscillate.

PRACTICAL PROBLEMS IN FILTER IMPLEMENTATION

In the introductory section we dealt with filters as mathematical functions. The filter designs were assumed to be implemented with "perfect" components. It's only when the filter is built with real-world components that design tradeoffs which must be made.

In building a filter with an order greater the two, multiple second and/or first order sections are used. The frequencies and Qs of these sections must align precisely or the overall response of the filter will be affected. For example, the antialiasing filter design example previously discussed is a 5th order Butterworth filter, made up of a second order section with a frequency (Fo) = 1 and a Q = 1.618, a second order section with a frequency (Fo) = 1 and a Q = .618 and a first order section with a frequency (Fo) = 1 (for a filter normalized to 1 rad/sec). If the Q or frequency response of any of the sections is off slightly, the overall response will deviate from the desired response. It may be close, but it won't be exact.

PRACTICAL CONSIDERATIONS IN FILTER IMPLEMENTATION

- **Higher Order Filters Require Accurate First and Second Order Sections: Q and Frequency Response**
- **Passive Component Inaccuracies, Parasitics, and Drift**
- **Active Component Frequency Response, Input and Output Impedance, and Distortion**

Figure 6.25

RESISTOR CONSIDERATIONS

- Accuracy (Using Standard Values) and Temperature Coefficient
- Select Values Between 100Ω and 1MΩ
- Use Metal Film if Possible

Figure 6.26

PASSIVE COMPONENTS (RESISTORS, CAPACITORS, INDUCTORS)

Passive components are the first problem. When designing filters, values of components are required that are not available commercially. Resistors, capacitors, and inductors come in standard values. While custom values can be ordered, the tolerance will still be +/- 1% at best. An alternative is to build the required value out of a series and/or parallel combination of standard values. This increases the cost and size of the filter. Not only is the cost of components increased, but so are the manufacturing costs, both for loading and for tuning the filter. Furthermore, it's success will be still limited by the number of parts that are used, their tolerance, and their tracking. A more practical way is to use a circuit analysis program to determine the response using standard values. The program can also evaluate the effects of component drift over temperature. The values of the sensitive components are adjusted using parallel combinations where needed, until the response is within the desired limits.

In addition to the initial tolerance of the components, you must also evaluate the effects of temperature drift. The temperature coefficients of the various components may be different in both magnitude and sign. Capacitors, especially, are difficult in that not only do they drift, but the temperature coefficient is also a function of temperature as shown in Figure 6.27.

Capacitors also have temperature coefficients that vary with the value of capacitance, being higher on larger values. Some of the plastic film capacitors

(notably polycarbonate) also change their nominal value permanently when heated. Again, some capacitors, mainly the plastic film types, have a limited temperature range.

CAPACITANCE CHANGE VERSUS TEMPERATURE

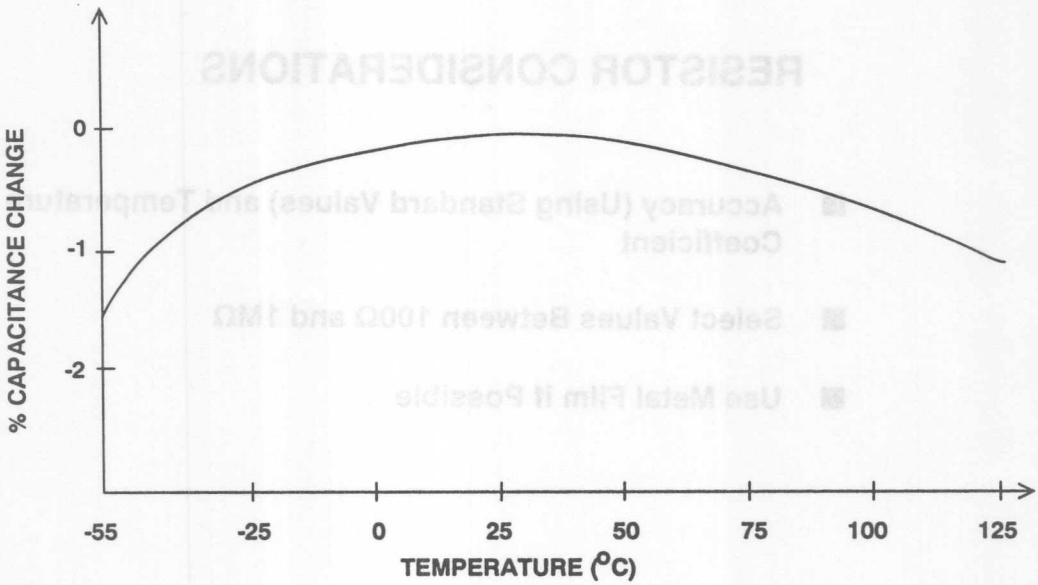


Figure 6.27

CAPACITOR CONSIDERATIONS

- Accuracy (Using Standard Values) and Temperature Coefficient
- Parasitics: Inductance, Leakage, Dielectric Absorbtion
- Select Values Between 1pF and 10μF
- Avoid Electrolytics
- Polystyrene (plastic film) is Preferable

Figure 6.28

The frequency and Q of a filter are determined by the component values. Obviously, if the component value is drifting, the frequency and the Q of the filter will drift which, in turn, will cause the frequency response to vary. This is especially true in higher order filters. Higher order means that you will have higher Q sections. Higher Q sections means that component values are more critical, since the Q is typically set by the ratio of two components, usually capacitors.

While there is infinite choice of the values of the passive components for building filters, in practice there are physical limits. Capacitor values below 1 pF and above 10 μF are not practical. Electrolytic capacitors should be avoided in circuits requiring any sort of accuracy. Electrolytic capacitors are also very leaky. If they are operated without a polarizing voltage, they become non-linear when the ac voltage reverse biases them. Even with a dc polarizing voltage, the ac signal can reduce the instantaneous voltage to 0 or below. Large values of film capacitors are physically very big.

Resistor values of less than 100 Ω should be avoided, as should values over 1 MΩ. Very low resistance values (under 100 Ω) require a great deal of drive current and dissipate a great deal of power. Both of these should be avoided. Very large values tend to be more prone to parasitics. Noise also increases with the square root of the resistor value.

Parasitic capacitances due to circuit layout and other sources affect the performance of the circuit. They can form between two traces on a PC board (on the same side or opposite side of the board), between leads of adjacent components and just about everything else you can (and in most cases can't) think of. These capacitances are usually small, so their effect is greater at high impedance nodes. Thus they can be controlled most of the time by keeping the impedance of the circuits down. Remember that the effects of stray

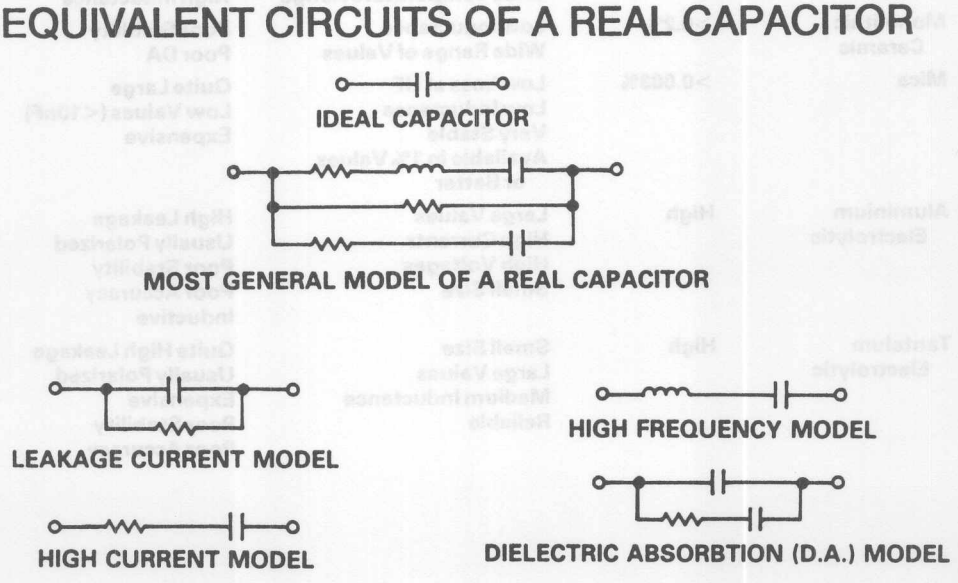


Figure 6.29

FEATURES OF COMMON CAPACITORS

TYPE	TYPICAL DIELECTRIC ABSORPTION	ADVANTAGES	DISADVANTAGES
NPO Ceramic	0.1%	Small Case Size Inexpensive Good Stability Wide Range of Values Many Vendors Low Inductance	DA too High for More than 8-Bit Applications
Polystyrene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values Good Stability	Destroyed by Temperature > +85°C Large Case Size High Inductance
Polypropylene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values	Destroyed by Temperature > +105°C Large Case Size High Inductance
Teflon	0.003% to 0.02%	Low DA Available Good Stability Operational Above +125°C Wide Range of Values	Relatively Expensive Large High Inductance
MOS	0.01%	Good DA Small Operational Above +125°C Low Inductance	Limited Availability Available only in Small Capacitance Values
Polycarbonate	0.1%	Good Stability Low Cost Wide Temperature Range	Large DA Limits to 8-Bit Applications High Inductance
Polysulfone	0.1%	Good Stability Low Cost Wide Temperature Range	Large DA Limits to 8-Bit Applications High Inductance
Monolithic Ceramic	>0.2%	Low Inductance Wide Range of Values	Poor Stability Poor DA
Mica	>0.003%	Low Loss at HF Low Inductance Very Stable Available in 1% Values or Better	Quite Large Low Values (<10nF) Expensive
Aluminium Electrolytic	High	Large Values High Currents High Voltages Small Size	High Leakage Usually Polarized Poor Stability Poor Accuracy Inductive
Tantalum Electrolytic	High	Small Size Large Values Medium Inductance Reliable	Quite High Leakage Usually Polarized Expensive Poor Stability Poor Accuracy

Figure 6.30

RESISTOR COMPARISON CHART

TYPE		ADVANTAGES	DISADVANTAGES
DISCRETE	Carbon Composition	Lowest Cost High Power/Small Case Size	Poor Tolerance (5%) Poor Temperature Coefficient (1500ppm/°C)
	Wire-Wound	Excellent Tolerance (0.01%) Excellent TC (1ppm/°C) High Power	Reactance May be a Problem Large Case Size Most Expensive
	Metal Film	Good Tolerance (0.1%) Good TC (<1 to 100ppm/°C) Moderate Cost	Must be Stabilized with Burn-In Low Power
	Bulk Metal or Metal Foil	Excellent Tolerance (to 0.005%) Excellent TC (to <1ppm/°C) Low Reactance	Low Power Very Expensive
	High Megohm	Very High Values (10^8 - $10^{14}\Omega$) Only Choice for Some Circuits	High Voltage Coefficient (200ppm/V) Fragile Glass Case Expensive
NETWORKS	Thick Film	Low Cost High Power Laser-Trimmable Readily Available	Fair Matching (0.1%) Poor TC (>100ppm/°C) Poor Tracking TC (10ppm/°C)
	Thin Film on Glass	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance	Delicate Often Large Geometry Low Power
	Thin Film on Ceramic	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance Suitable for Hybrid IC Substrate	Often Large Geometry
NETWORKS	Thin Film on Silicon	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Suitable for Monolithic IC Construction	Some Capacitance to Substrate Low Power
	Thin Film on Sapphire	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Laser-Trimmable Low Capacitance	Higher Cost Low Power

Figure 6.31

capacitance are frequency dependant, being worse at high frequencies because the impedance drops with increasing frequency.

Parasitics are not just associated with outside sources. They are also present in the components themselves.

A capacitor is more than just a capacitor in most instances. A real capacitor has inductance (from the leads and other sources) and resistance as shown in Figure 6.29. This resistance shows up in the specifications as leakage and poor power factor. Obviously, we would like capacitors with very low leakage and good power factor (see Figure 6.30). Resistors also have inductances.

In general it is best to use plastic film (preferably polystyrene) or mica capacitors and metal film resistors, both of moderate to low values in our filters.

One way to reduce component parasitics is to use surface mounted devices. Not having leads means that the lead inductance is reduced. Also, being physically smaller allows more optimal placement. A disadvantage is that not all types of capacitors are available in surface mount.

LIMITATIONS OF ACTIVE ELEMENTS (OP AMPS) IN FILTERS

The active element of the filter will also have a pronounced effect on the response.

In developing the various topologies (Multiple Feedback, Sallen-Key, State Variable, etc.), the active element was always modeled as a "perfect" operational amplifier. That is to say it has:

1) infinite gain
2) infinite input impedance
3) zero output impedance

none of which varies with frequency. While amplifiers have improved a great deal over the years, this model has not yet been realized.

The most important limitation of the amplifier has to due with its gain variation with frequency. All amplifiers are band limited. This is due mainly to the physical limitations of the devices with which the amplifier is constructed. Negative feedback theory tells us that the response of an amplifier must be first order (-6 dB per octave) when the gain falls to unity in order to be stable. To accomplish this, a real pole is usually introduced in the amplifier so the gain rolls off to < 1 by the time the phase shift reaches 180 degrees (plus some phase margin, hopefully). This roll off is equivalent to that of a single pole filter. So in simplistic terms, the transfer function of the amplifier is added to the transfer function of the filter to give a composite function. How much the frequency dependant nature of the op amp affects the filter is dependant on which topology is used.

The Sallen-Key configuration, for instance, is the least dependant on the frequency response of the amplifier. All that is required is for the amplifier response to be flat to just past the frequency where the attenuation of the filter is below the minimum attenuation required. This is because the amplifier is used as a gain block. Beyond cutoff, the attenuation of the filter is reduced by the rolloff of the gain of the op amp. This is because the output of the amplifier is phase shifted, which results in incomplete nulling when fed back to the input.

The state variable configuration uses the op amps in two modes, as amplifiers and as integrators. As amplifiers, the constraint on frequency response is the same as for the Sallen-Key, that is flat out to the minimum attenuation frequency. As an integrator, however, more is required. A good rule of thumb is that the open loop gain of the amplifier must be greater than 10 times the closed loop

CONSIDERATIONS FOR OP AMPS

- Finite Gain-Bandwidth
- Input Impedance
- Output Impedance
- Distortion

Figure 6.32

SALLEN KEY SENSITIVITY TO OP AMP

- Least Dependent on Op Amp Frequency Response. Op Amp Used As Gain Block
- Op Amp Flat to Slightly Beyond Filter Stopband Frequency
- Can Use Current Feedback Op Amps in Sallen Key Configuration

Figure 6.33

gain. This should be taken as the absolute minimum requirement. What this means is that there must be 20 dB loop gain, minimum. Therefore, an op amp with 10 MHz unity gain bandwidth can be used to make a 1 MHz integrator. What happens is that the effective Q of the circuit increases as loop gain decreases. This phenomenon is called Q enhancement. The mechanism for Q enhancement is similar to that of slew rate limitation. Without sufficient loop gain, the op amp virtual ground is no longer at ground. In other words, the op amp is no longer behaving as a op amp. Because of this, the integrator no longer behaves like an integrator.

The multiple feedback configuration also places heavy constraints on the active element. Q enhancement is a problem in this topology as well. As the loop gain falls, the Q of the circuit increases, and the parameters of the filter change. The same rule of thumb as used for the integrator apply to the multiple feedback topology (loop gain should be at least 20 dB).

In the FDNR realization, the requirements for the op amps are not as clear. To make the circuit work, we assume that the op amps will be able to force the input terminals to be the same voltage. This implies that the loop gain be a minimum of 20 dB at the resonant frequency. Also it is generally considered to be advantageous to have the two op amps in each leg matched. This is easily accomplished using dual op amps. It is also a good idea to have low bias current devices for the op amps, so FET input op amps should be used, all other things being equal.

STATE VARIABLE SENSITIVITY TO OP AMP

- Op Amps Used as Amplifiers and Integrators
- Amplifiers: Flat to Beyond Stopband Frequency
- Integrators: 20dB Minimum Loop Gain (Open Loop Gain 10 Times Closed Loop Gain), or Q Enhancement Occurs
- 10MHz Unity-Gain Bandwidth Op Amp Can Make a 1MHz Integrator

Figure 6.34

MULTIPLE FEEDBACK SENSITIVITY TO OP AMP

- **Same Rule of Thumb as for Integrators: 20dB Minimum Loop Gain to Prevent Q Enhancement**

Figure 6.35

In addition to the frequency dependant limitations of the op amp, several other of its parameters may be important to the filter designer.

One is input impedance. As we said, the filter topologies assume "perfect" amplifiers. This implies that the input impedance is infinite. This is required so that the input of the op amp does not load the network around it. This means that we probably want to use FET amplifiers with high impedance circuits. There is also a small frequency dependant term to the input impedance, since the effective impedance is the real input impedance multiplied by the loop gain. This usually is not a major source of error, since the network impedance of a high frequency filter should be low.

Similarly, the op amp output impedance affects the response of the filter. The output impedance of the amplifier is divided by the loop gain, therefore the output impedance will rise with increasing frequency. This may have an effect with high frequency filters if the output impedance of the stage driving the filter becomes a significant portion of the network impedance.

The fall of loop gain with frequency can also effect the distortion of the op amp, since there is less loop gain available for correction. In the multiple feed back configuration the feedback loop is also frequency dependant, which may further reduce the feedback correction, resulting in increased distortion. This effect is counteracted somewhat by the reduction of distortion components in the filter network (assuming a lowpass or bandpass filter).

All of the discussion so far is based on using classical voltage feedback op amps. Current feedback, or transimpedance, op

FDNR SENSITIVITY TO OP AMP

- Loop Gain Should be 20dB Minimum at Resonant Frequency
- Match Op Amps in Each Leg (Use Duals)
- Use FET Input Op Amps for Low Bias Currents

Figure 6.36

OTHER OP AMP CONSIDERATIONS IN FILTERS

- Input and Output Impedance
- Distortion at Low Loop Gains
- Noise
- Dynamic Range (Overload), Q times Gain < Loop Gain
- Current Feedback Op Amps May Only be Used in Sallen Key Configuration

If Amp does not have distortion specs look for equal +ve & -ve slew rates as an indicator

Figure 6.37

amps offer improved high frequency response but are unusable in any topology except the Sallen-Key. The problem is that capacitance in the feedback loop of a current feedback amplifier usually causes it to become unstable. Also, most current feedback amplifiers will only drive small capacitive loads. Therefore, it is difficult to build classical integrators using current feedback amplifiers. Some current feedback op amps have an external pin which may be used to configure them as a very good integrator, but this configuration does not lend itself to classical active filter designs. Current feedback integrators are non-inverting, which is not acceptable in the state variable configuration. Also, the bandwidth of a current feedback amplifier is set by its feedback resistor which would make the Multiple Feedback topology difficult to implement. Another limitation of the current feedback amplifier in the Multiple Feedback configuration is the low input impedance of the inverting terminal. This would result in loading of the filter network. Sallen-Key filters are possible with current feedback amplifiers, since the amplifier is used as a non-inverting gain block. New topologies which capitalize on the current feedback amplifiers superior high frequency performance and compensate for its limitations will have to be developed.

The last thing that you need to be aware of is exceeding the dynamic range of the amplifier. Qs over 0.707 will cause peaking in the response of the filter (see Figure 6.38). For high Qs, this could cause overload of the input or output stages of the amplifier with a large input. Note that relatively small values of Q can cause significant peaking. The Q times the gain of the circuit must stay under the loop gain (plus some margin, again 20 dB is a good starting point). This holds for multiple amplifier topologies as well. Be aware of internal node levels, as well as input and output levels. As an amplifier overloads, its effective Q decreases, so the transfer function will appear to change even if the output appears undistorted. This shows up as the transfer function changing with increasing input level.

EFFECT OF FILTER Q ON GAIN PEAKING

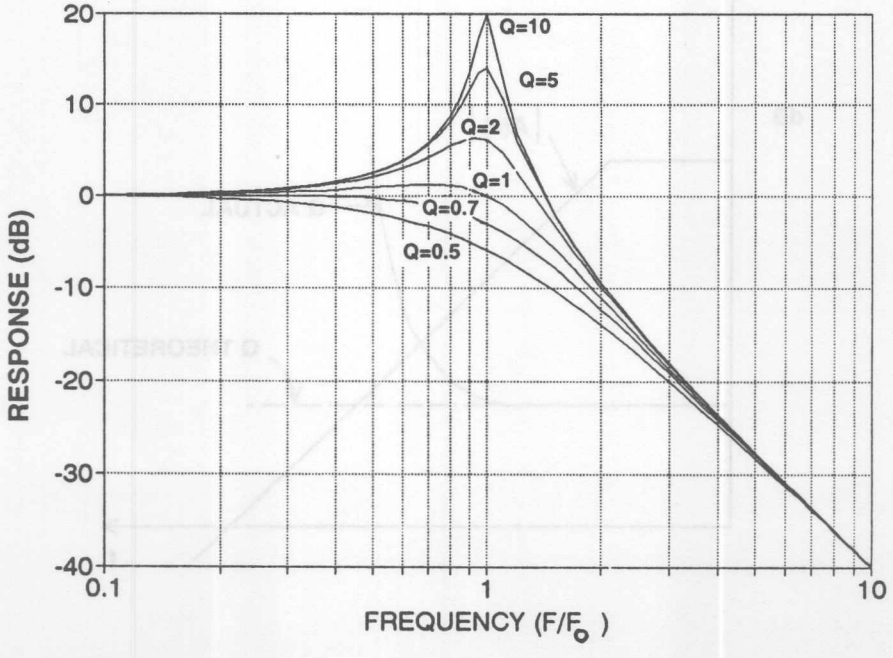


Figure 6.38

We have been dealing mostly with lowpass filters in our discussions, but the same principles are valid for highpass, bandpass, and band reject as well. In general, things like Q enhancement and limited gain/bandwidth will not effect highpass filters, since the resonant frequency will probably be low in relation to the cutoff frequency of the op amp. Remember, though, that the highpass filter will have a low pass section, by default, at the cutoff frequency of the amplifier. Bandpass and bandreject (notch) filters will be affected, especially since both tend to have high values of Q. The general effect of the op amp's frequency response on the filter Q is shown in Figure 6.39.

As an example of the Q enhancement phenomenon, consider the Spice simulation of a 10 kHz bandpass Multiple Feedback filter with Q = 10 and gain = 1, using a good high frequency amplifier (the AD847) as the active device. The circuit diagram is shown in Figure 6.40. The open loop gain of the AD847 is greater than 70 dB at 10 kHz as shown in Figure 6.41. This is well over the 20 dB minimum, so the filter works as designed as shown in Figure 6.42. We now replace the AD847 with an OP-90. The OP-90 is a dc precision amplifier and so has a limited bandwidth. In fact, its open loop gain is less than 10 dB at 10 kHz (see Figure 6.41). This is not to imply that the AD847 is in all cases better than the OP-90. It is a case of misapplying the OP-90. From the output for the OP-90, also shown in Figure 6.42, we see that the magnitude of the output has been reduced, and the center frequency has shifted downward.

Q ENHANCEMENT

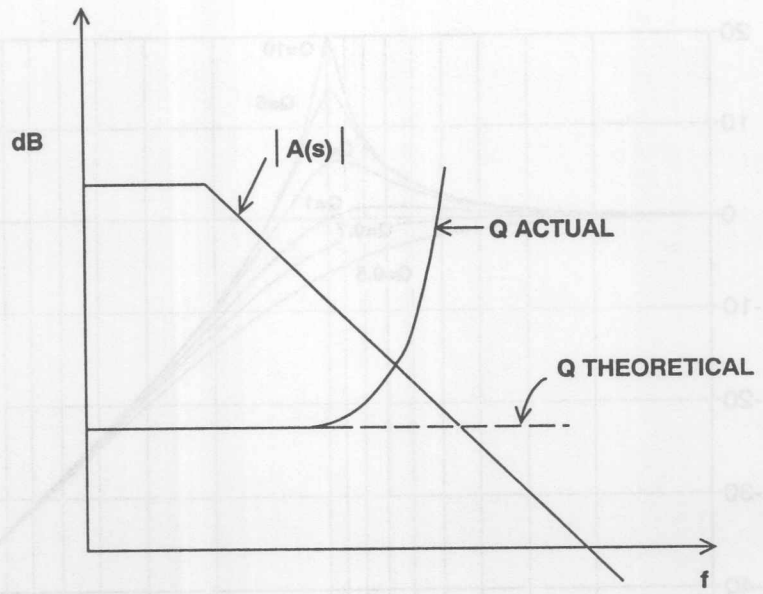


Figure 6.39

10KHz MULTIPLE FEEDBACK BANDPASS FILTER

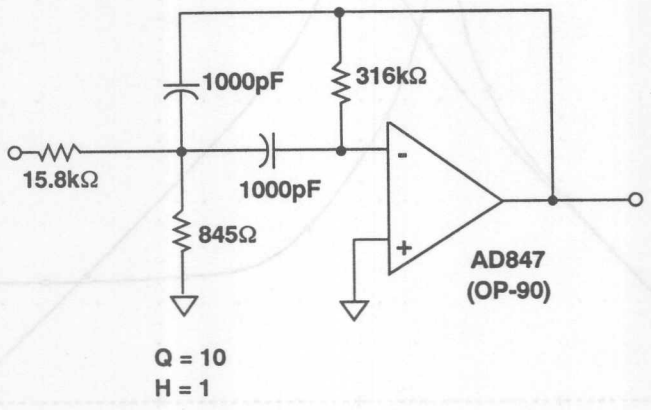
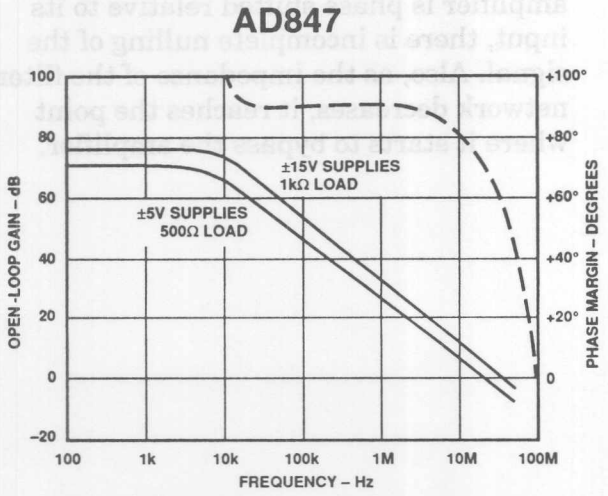


Figure 6.40

OPEN LOOP GAIN OF AD847 AND OP-90 OP AMPS



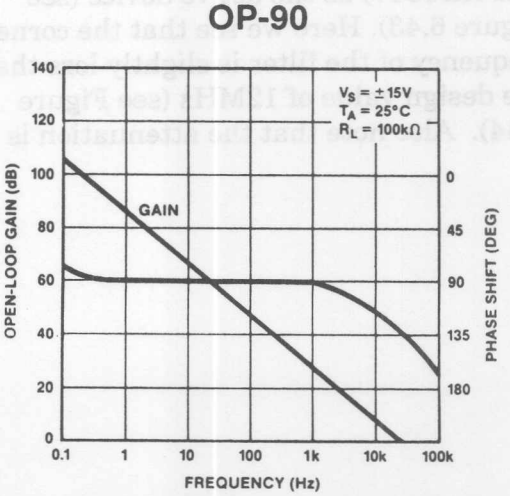


Figure 6.41

FREQUENCY RESPONSE OF 10kHz BANDPASS FILTER USING AD847 AND OP-90 OP AMPS

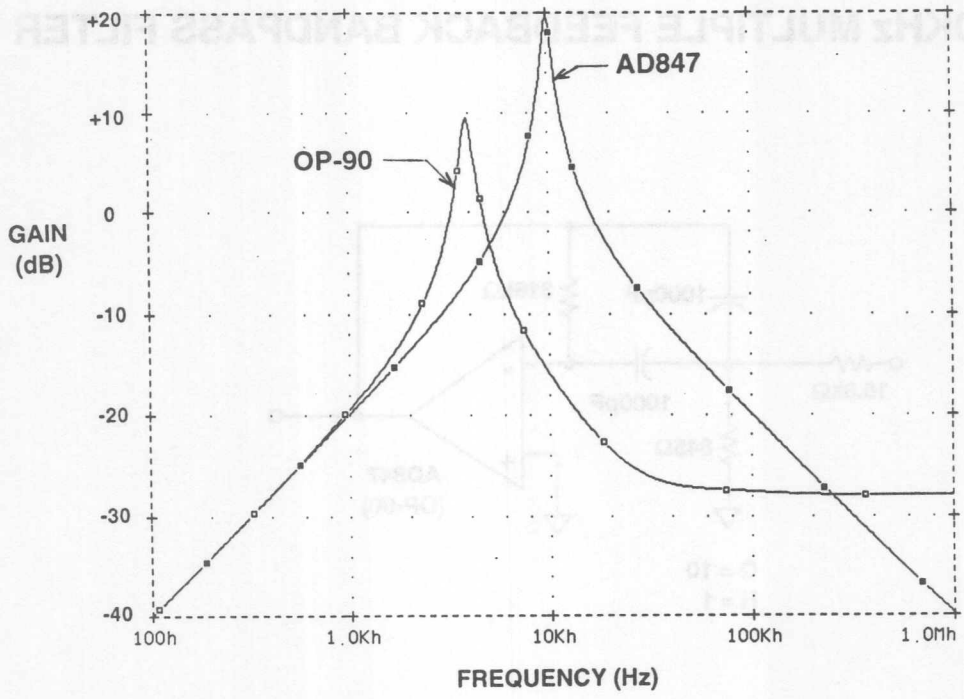


Figure 6.42

A 12MHz Sallen-Key Filter Using a Current Feedback Amplifier

As a demonstration of a high frequency filter we will design a 12 MHz Sallen-Key filter using a transimpedance amplifier (the AD9617) as the active device (see Figure 6.43). Here we see that the corner frequency of the filter is slightly less that the design value of 12MHz (see Figure 6.44). Also note that the attenuation is only good to about 100 MHz. This is where the loop gain of the amplifier starts to decrease. Now, since the output of the amplifier is phase shifted relative to its input, there is incomplete nulling of the signal. Also, as the impedance of the filter network decreases, it reaches the point where it starts to bypass the amplifier.

12 MHz SALLEN-KEY LOWPASS FILTER WITH BUTTERWORTH RESPONSE USES CURRENT FEEDBACK AMPLIFIER

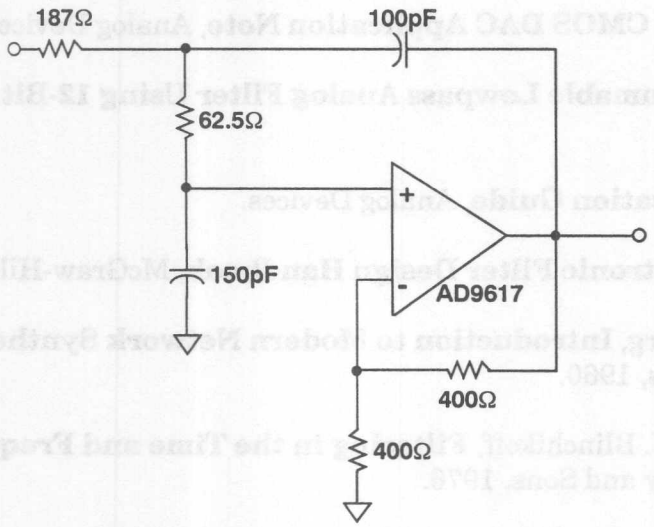


Figure 6.43

FREQUENCY RESPONSE OF 12MHz SALLEN-KEY LOWPASS FILTER

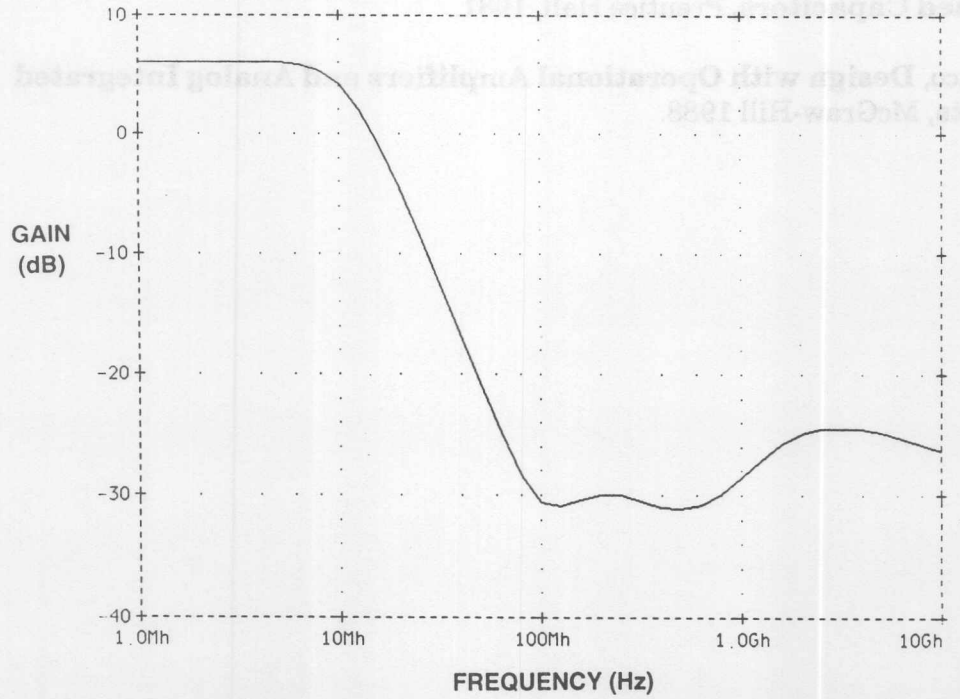


Figure 6.44

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SECTION VII
DRIVING ADCs

- ADC Performance Specifications
- Effects of Drive Amplifier on System Performance
- Specifying and Positioning the Antialiasing Filter
- Driving Non-Sampling ADCs
- Driving Sampling ADCs
- Driving Flash Converters
- Driving Precision 16-bit Sampling ADCs
- Driving Sigma-Delta Audio ADCs
- ADC Input Clamping and Protection Circuits

SECTION VII

DRIVING ADCs

WALT KESTER

INTRODUCTION

Selecting the appropriate drive amplifier for an ADC involves many tradeoffs. In order to make these tradeoffs, overall system requirements must be understood as well as how they relate to the ADC and the drive circuitry. In most real-time DSP signal processing applications (see Figure 7.1), the dynamic performance of the ADC is critical. Therefore ADCs with integral sample-and-hold functions (usually called *sampling* ADCs) are often selected. Such specifications as signal-to-noise ratio, effective number of bits, full-power bandwidth, harmonic distortion, total harmonic distortion, and spurious free dynamic range are often used as selection criteria for the ADC. It then becomes important that the op amp driving the ADC not introduce errors which will degrade the ADC performance.

The antialiasing filter must usually be considered in conjunction with the drive amplifier. This is necessary in order to calculate noise performance correctly. The filter may be passive or active, depending on the signal frequencies of interest. It must be designed based on the signal characteristics and the dynamic range required. Further discussions regarding active and passive filters will be found in Section 6.

There are many signal processing applications where both ac performance and dc precision are important. In these applications, there are even more tradeoffs to make.

In some applications the signal to be digitized is dc or changing very slowly relative to the conversion time, and a sampling ADC is not required. Even

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AMPLIFIERS AS PART OF REALTIME SIGNAL PROCESSING SYSTEMS

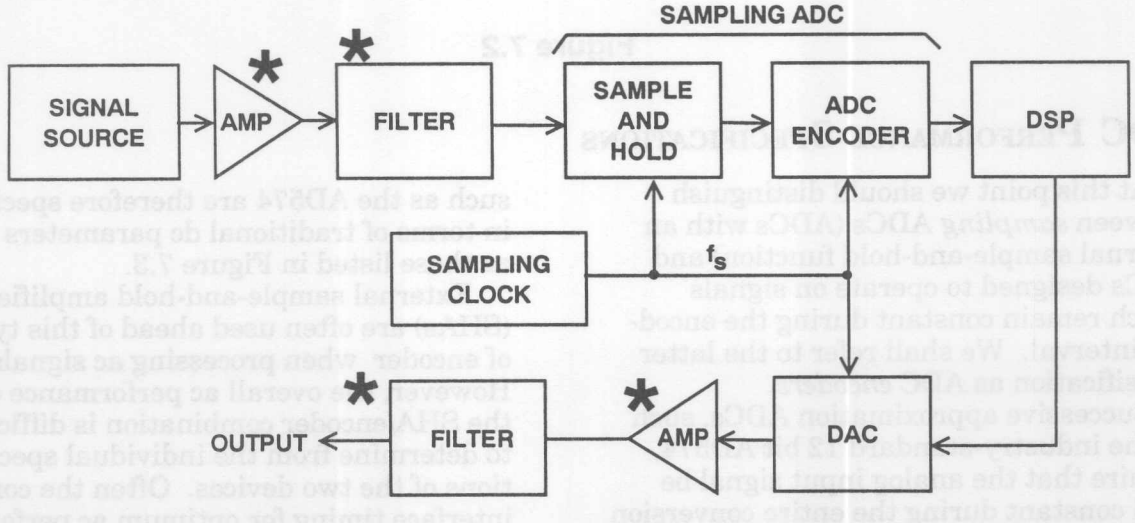


Figure 7.1 #1

these dc applications may place certain requirements on the op amp's ac performance because of the design of the ADC input circuits.

Finally, there are applications where the sample-and-hold function is performed ahead of the ADC, such as in a CCD imaging system or a multiplexed simultaneous-sampling data acquisition system as shown in Figure 7.2. In these systems, the settling time of the amplifier driving the ADC is critical to digitizing the signal accurately.

Before intelligent decisions can be made regarding the drive amplifier, it is necessary to have an understanding of the overall system performance requirements. Key to system performance is the ADC which will be discussed in the next few sections.

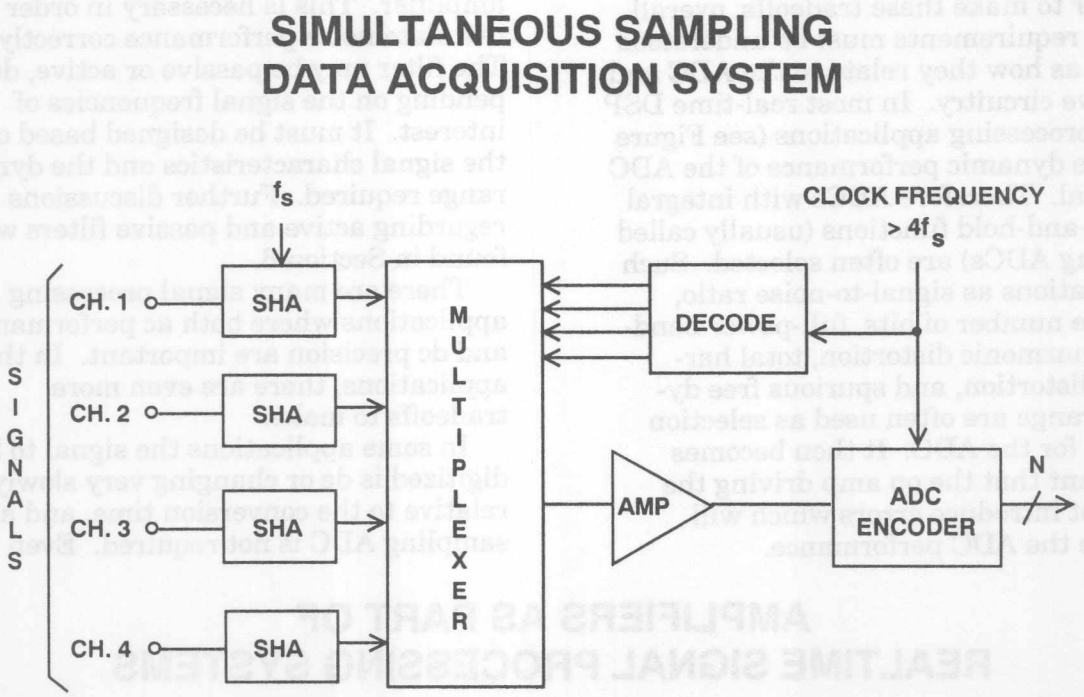


Figure 7.2

ADC PERFORMANCE SPECIFICATIONS

At this point we should distinguish between *sampling* ADCs (ADCs with an internal sample-and-hold function) and ADCs designed to operate on signals which remain constant during the encoding interval. We shall refer to the latter classification as ADC *encoders*.

Successive approximation ADCs, such as the industry-standard 12 bit AD574, require that the analog input signal be held constant during the entire conversion cycle. Otherwise, large errors in the conversion process will result. Encoders such as the AD574 are therefore specified in terms of traditional dc parameters such as those listed in Figure 7.3.

External sample-and-hold amplifiers (SHAs) are often used ahead of this type of encoder when processing ac signals. However, the overall ac performance of the SHA/encoder combination is difficult to determine from the individual specifications of the two devices. Often the correct interface timing for optimum ac performance must be determined experimentally. Another popular ADC encoder

architecture is called digitally-corrected-subranging (DCS). The conversion is made in multiple steps of several bits each, therefore, a SHA is also required for accurate sampling of ac signals using converters with this architecture.

Recent innovations in circuit design and IC process technology allow the SHA function to be included on the same chip with the ADC encoder. This type of ADC is usually referred to as a *sampling* ADC. These converters are completely specified in terms of dc and ac parameters, making their application much easier. In addition, users no longer have to concern themselves with optimizing the SHA/encoder interface.

There are many factors which go into the selection of an ADC for a system application. Most are based upon the particular characteristics of the signal to be processed. Signal bandwidth usually determines the minimum sampling rate required of the ADC. Nyquist's Criterion states that the signal must be sampled at a rate equal to at least twice the maximum signal frequency in order to avoid aliasing. As we will see later, higher sampling rates are usually chosen in order to ease the requirements placed on the antialiasing filter.

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TRADITIONAL DC SPECIFICATIONS FOR NON-SAMPLING ADC ENCODERS

- **Offset, Offset Temperature Coefficient**
- **Gain, Gain Temperature Coefficient**
- **Integral Non-Linearity**
- **Differential Non-Linearity**
- **Conversion Time**

Figure 7.3

ADCs FOR DSP APPLICATIONS

- Most are *Sampling* ADCs Containing on-chip SHA as Opposed to *Encoders*, which have no SHA
- Interface Between SHA and ADC Handled on-chip
- Complete DC and AC Specifications Usually Provided

Figure 7.4

SHANNON'S INFORMATION THEOREM AND NYQUIST'S CRITERION

- Shannon: An Analog Signal with a *BANDWIDTH* of f_a Must be Sampled at a Rate $f_S > 2f_a$ in Order to Avoid the Loss of Information
- Nyquist: If $f_S < 2f_a$, then a Phenomena Called *ALIASING* will Occur

Figure 7.5

In addition to establishing the minimum sampling rate, f_S, the resolution of the ADC must be determined. Figure 7 shows the weight of the least significant bit (relative to a 10 Volt peak-to-peak analog input range) for ADCs of various resolutions. Also shown is the theoretical rms quantization noise for an ideal N-bit ADC with no dc or ac errors. The theoretical value of the quantization noise within the Nyquist bandwidth, $f_S/2$, is , where q is the weight of the least significant bit (LSB). The resulting theoretical signal-to-noise ratio (SNR) for a perfect N bit ADC is given by SNR = 6.02N + 1.76dB. This value is also given in Figure 7.6.

BIT SIZES, THEORETICAL QUANTIZATION NOISE, AND SNR FOR 10V FULLSCALE CONVERTERS

Resolution (Bits)	1 LSB = q	%FS	ppm FS	RMS Quantization Noise, $q/\sqrt{12}$	Theoretical SNR (dB)
4	625mV	6.25	62500	180mV	25.8
6	156mV	1.56	15625	45mV	37.9
8	30mV	0.39	3906	11.2mV	50.0
10	9.76mV	0.098	977	3.46mV	62.0
12	2.44mV	0.024	244	704µV	74.0
14	610µV	0.0061	61	176µV	86.0
16	153µV	0.0015	15	44µV	98.1
18	38µV	0.0004	4	11µV	110.1
20	9.5µV	0.0001	1	2.7µV	122.2
22	2.4µV	0.000024	0.24	0.7µV	134.2
24	0.6µV	0.000006	0.06	0.2µV	146.2

Figure 7.6

SIGNAL-TO-NOISE RATIO (SNR) AND EFFECTIVE BITS (ENOB)

In testing ADCs, the SNR is usually calculated using DSP techniques while applying a pure sinewave signal to the input of the ADC. A typical test system is shown in Figure 7.7.

The Fast Fourier Transform (FFT) processes a finite number of time samples and converts them into a frequency spectrum such as the one shown in Figure 7.8 for the AD676 16 bit 100kSPS sampling ADC. The frequency spectrum is then used to calculate the SNR as well as harmonics of the fundamental input signal, a technique very similar to that of an analog spectrum analyzer.

The rms value of the signal is first computed. Then the rms value of all other frequency components over the Nyquist bandwidth (this includes not only noise but also distortion products) is computed. The ratio of these two quantities, expressed in dB is the SNR. Various error sources in the ADC cause the measured SNR to be less than the theoretical value, 6.02N + 1.76dB. These errors are due to integral and differential nonlinearities, missing codes, and internal ADC noise sources. In addition, the errors are a function of input slewrate and therefore increase as the input frequency gets higher. In calculating the rms value of the noise, it is customary to include harmonics of the fundamental signal. This is sometimes referred to as the

ADC DYNAMIC TESTING

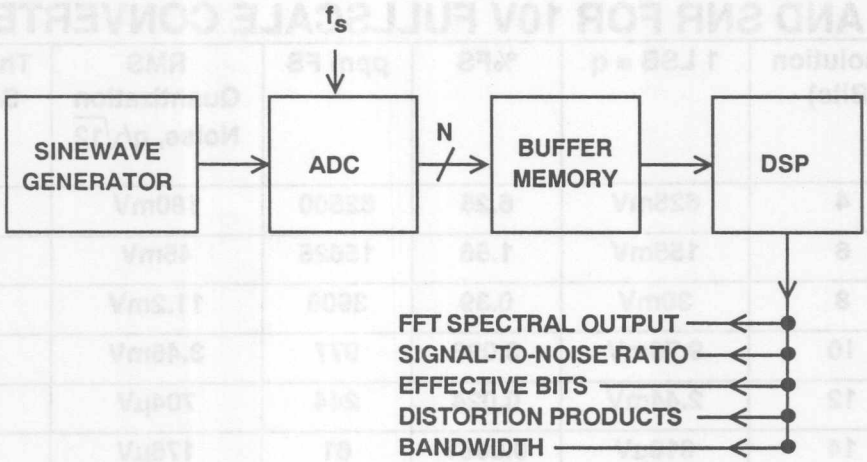


Figure 7.7

AD676 16-BIT, 100kSPS ADC FFT OUTPUT

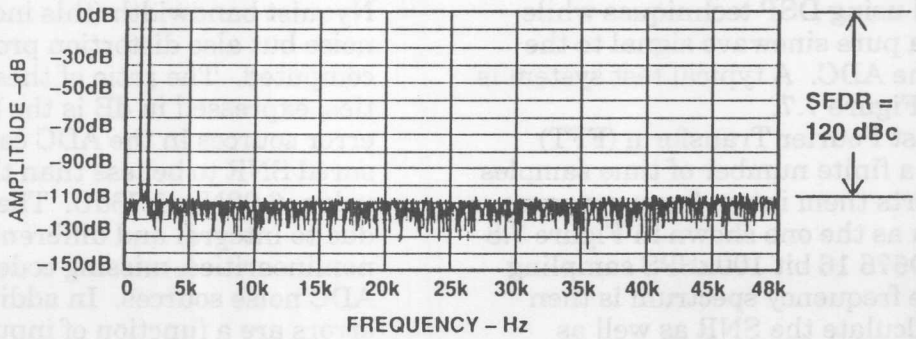


Figure 7.8

signal-to-noise-plus-distortion, S/(N+D), but is usually called simply SNR. A typical plot of S/(N+D) for the AD676 sampling ADC (16 bits, 100kSPS) is shown in Figure 7.9.

This leads to the definition of another important ADC dynamic specification, the *effective-number-of-bits*, or ENOBs. The effective bits are calculated by first measuring the SNR of an ADC with a fullscale sinewave input signal. The measured SNR (SNR_{actual})is substituted into the equation for SNR, and the equation is solved for N as shown in Figure 710. In the case of the AD676, a 16 bit ADC, an SNR of 88dB corresponds to approximately 14 effective bits. This means that the same dynamic performance will be achieved if the imperfect 16 bit ADC is replaced by a perfect 14 bit ADC.

AD676 16-BIT, 100kSPS SAMPLING ADC S/N + D AND EFFECTIVE BIT PERFORMANCE

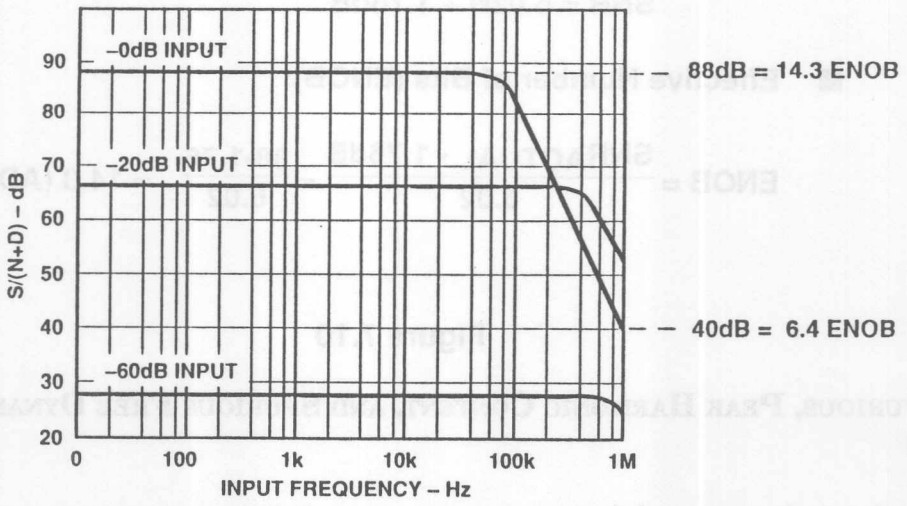


Figure 7.9

QUANTIZATION THEORY BASICS

- **RMS Quantization Noise in Nyquist Bandwidth, $f_S/2$:**

  $q/\sqrt{12}$, q = LSB Weight

- **Fullscale Sinewave RMS Signal to RMS Noise Ratio in Nyquist Bandwidth:**

  $SNR = 6.02N + 1.76dB$

- **Effective Number of Bits (ENOB):**

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB}{6.02} = \frac{88-1.76}{6.02} = 14.3 \text{ (AD676)}$$

Figure 7.10

PEAK SPURIOUS, PEAK HARMONIC CONTENT, AND SPURIOUS FREE DYNAMIC RANGE (SFDR)

The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in dB relative to the rms value of a fullscale input signal as shown in the previous Figure 7.8. The peak spurious specification is also occasionally referred to as spurious free dynamic range (SFDR). SFDR is usually measured over a wide range of input frequencies and at various amplitudes.

It is important to note that the harmonic distortion or SFDR of an ADC is not limited by its theoretical SNR value. The SFDR of a 12 bit ADC may exceed 85dB, while the theoretical SNR is only 74dB. On the other hand, the S/N+D of the ADC may be limited by poor harmonic distortion performance, since the harmonic components are included with the quantization noise when computing the rms noise level.

TOTAL HARMONIC DISTORTION (THD)

Total harmonic distortion (THD) is the ratio of the rms sum of the harmonic components to the rms value of a input signal and is expressed in a percentage or in dB. For input signals or harmonics that are above the Nyquist frequency, the aliased components are used in making the calculation. THD is usually measured at several input signal frequencies and amplitudes.

FULL-POWER BANDWIDTH

The full-power bandwidth (FPBW) of an ADC is that input frequency at which the amplitude of the reconstructed FFT *fundamental* is reduced by 3dB for a fullscale input. Full-power bandwidth must be examined in conjunction with SNR, ENOB, and THD in order to determine the dynamic performance of the ADC at the FPBW frequency. For example, the FBBW of the AD676 ADC is 1MHz, but at 1MHz, the SNR is only 40dB, or 6.4 effective bits.

The FPBW specification is important when selecting the ADC drive amplifier. The output noise spectral density of the amplifier must be integrated over the entire small-signal bandwidth of the ADC if there is no filter between the amplifier and the ADC. The small signal ADC bandwidth is approximately equal to the FPBW if there is no slew rate limiting. In cases where the FPBW is significantly less than the small signal bandwidth, the small signal bandwidth should be used in noise calculations.

ADC FULL-POWER BANDWIDTH

- The Frequency at Which the Amplitude of the *Fundamental* Component in the FFT Output is Down 3dB
- FPBW Usually > f_S (Except for ΣΔ ADCs)
- Must Examine ENOB and THD at FPBW Frequency
- Example: AD676 FPBW = 1MHz, But Only 6.4 ENOB @ 1MHz
- Use FPBW or Small Signal BW (if Greater Than FPBW) for Noise Calculations

Figure 7.11

EFFECTS OF ADC DRIVE AMPLIFIER ON SYSTEM PERFORMANCE

Because the ADC drive amplifier is in the signal path to the ADC, its error sources (both dc and ac) must be considered in calculating the total error budget. Ideally, the ac and dc performance of the amplifier should be such that there is no degradation of the ADC performance. It is rarely possible to achieve this, however; and therefore, the effects of each amplifier error source on system performance should be evaluated individually.

Evaluating and selecting op amps based on the dc requirements of the system is a relatively straightforward matter. For many applications it is common for the amplifier to be selected first on the basis of ac performance (bandwidth, THD, noise, etc.). If the ac perfor-

mance is satisfactory for the application, then the dc specifications are examined in light of system requirements.

The primary functions of the ADC drive amplifier are to provide signal buffering, gain (if required), and level shifting (if required) as shown in Figure 7.12.

The amplifier output drive capability must match the ADC input requirements. ADCs usually present both a resistive and a reactive load to the amplifier. The amplifier must be stable under the required gain and load conditions. The input circuits of the ADC may inject high frequency current spikes into the op amp output. This places a requirement on the op amp settling time and ac output impedance which will be discussed shortly.

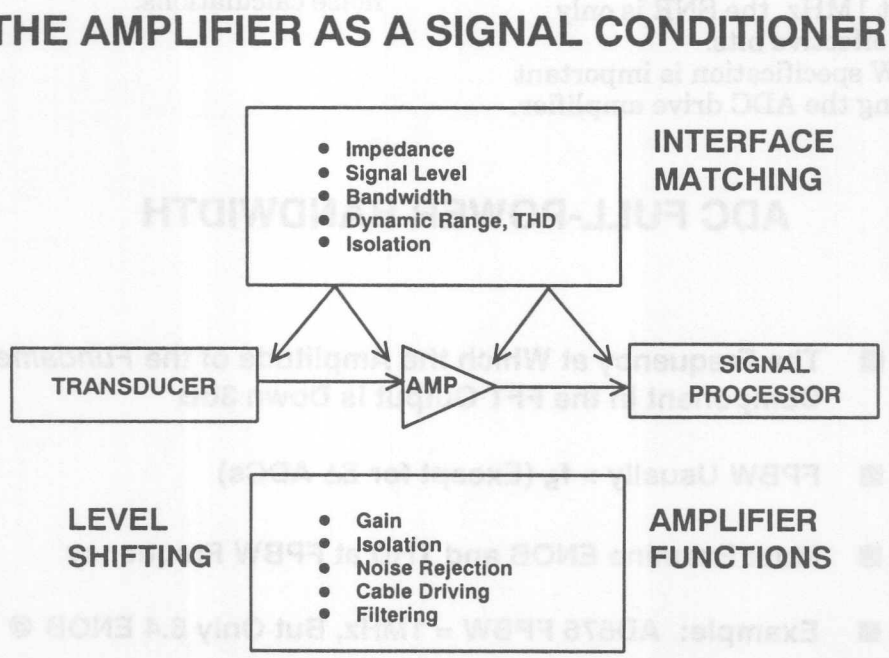


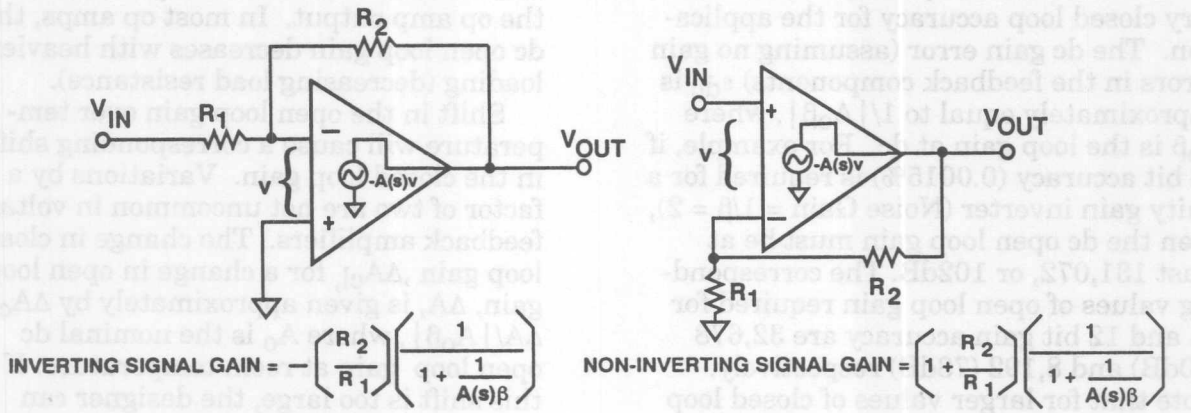
Figure 7.12

VOLTAGE FEEDBACK AMPLIFIERS

The equivalent circuit for a voltage feedback amplifier is given in Figure 7.13. The input voltage is multiplied by the open loop gain A(s) to yield the output voltage. The feedback attenuation factor is β. The equations relating the input and output voltage for the inverting and the non-inverting mode are also given in Figure 7.13.

The term $A(s)\beta$ is referred to as the *loop gain*. It is the value of the loop gain at any frequency which will determine the overall accuracy of the op amp. The so-called *curative* effects of feedback at any frequency are determined by the available amount of loop gain at that frequency. Loop gain affects gain accuracy and stability, linearity, distortion, input, and output impedance. (For further discussions see Reference 3, pp. 26-29). The corresponding Bode plot for a single pole rolloff with fixed compensation is shown in Figure 7.14. Notice that the product of the closed loop gain, $1/\beta$, and the closed loop bandwidth, A_{cl}, is constant over a wide range of frequencies. The frequency f_u is referred to as the unity gain bandwidth frequency.

VOLTAGE FEEDBACK OP AMP EQUIVALENT CIRCUITS



A(s) = OPEN LOOP VOLTAGE GAIN

β = FEEDBACK FACTOR = $\frac{R_1}{R_1+R_2}$

$\frac{1}{\beta}$ = NOISE GAIN = $1+\frac{R_2}{R_1}$

LOOP GAIN = $A(s)\beta$

Figure 7.13

LOG-LOG BODE PLOT FOR VOLTAGE FEEDBACK OP AMP

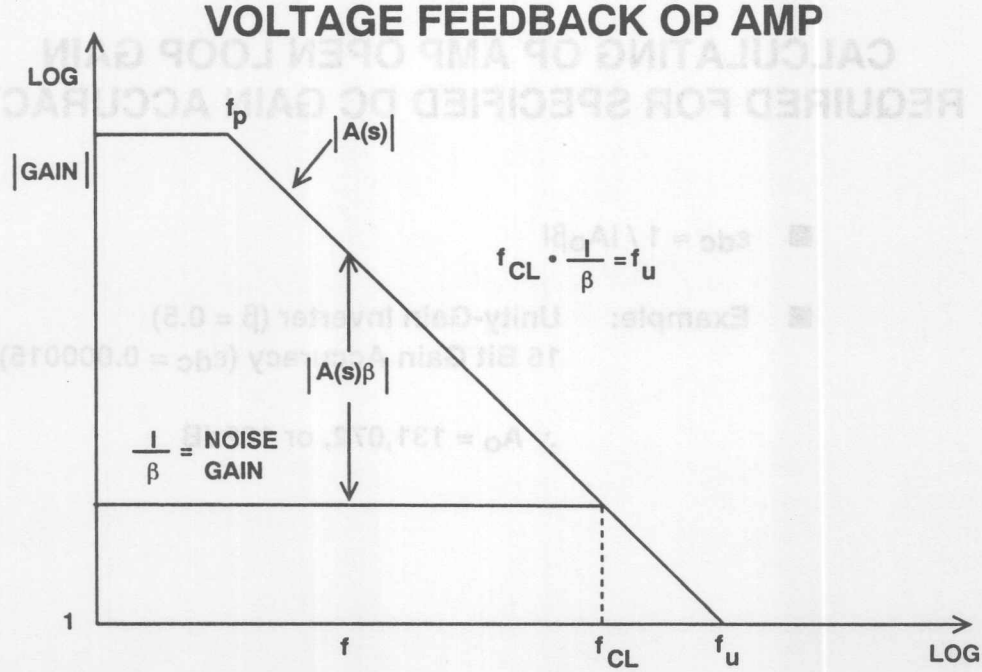


Figure 7.14

DC GAIN ACCURACY OF VOLTAGE FEEDBACK AMPLIFIERS

The dc open loop gain of the op amp must be sufficient to provide the necessary closed loop accuracy for the application. The dc gain error (assuming no gain errors in the feedback components) ε_{dc} is approximately equal to $1/|A_o\beta|$, where $A_o\beta$ is the loop gain at dc. For example, if 16 bit accuracy (0.0015%) is required for a unity gain inverter (Noise Gain = $1/\beta = 2$), then the dc open loop gain must be at least 131,072, or 102dB. The corresponding values of open loop gain required for 14 and 12 bit gain accuracy are 32,678 (90dB) and 8,192 (78dB) respectively. Note that for larger values of closed loop gain, correspondingly larger values of open loop gain are required to maintain the same amount of gain accuracy. The dc open loop gain specification of the amplifier should always be checked under the dc load conditions the ADC presents to the op amp output. In most op amps, the dc open loop gain decreases with heavier loading (decreasing load resistance).

Shift in the open loop gain over temperature will cause a corresponding shift in the closed loop gain. Variations by a factor of two are not uncommon in voltage feedback amplifiers. The change in closed loop gain ,ΔA_{cl}, for a change in open loop gain, ΔA, is given approximately by $\Delta A_{cl} = \Delta A/|A_o\beta|$, where A_o is the nominal dc open loop gain at room temperature. If this shift is too large, the designer can increase the feedback factor, β, select an op amp with better dc open loop gain stability, or select an op amp with a higher nominal dc open loop gain.

CALCULATING OP AMP OPEN LOOP GAIN REQUIRED FOR SPECIFIED DC GAIN ACCURACY

- $\varepsilon_{dc} \approx 1 / |A_o\beta|$
- **Example:** Unity-Gain Inverter ($\beta = 0.5$)
  16 Bit Gain Accuracy ($\varepsilon_{dc} = 0.000015$)

  $\therefore A_o = 131{,}072$, or 102dB

Figure 7.15

CALCULATING CHANGE IN CLOSED LOOP GAIN FOR CHANGE IN OPEN LOOP GAIN

- $\Delta A_{Cl} \approx \Delta A / |A_O \beta|$
- ΔA = Change in Open Loop Gain
- A_O = Nominal Open Loop Gain
- β = Feedback Factor
- ΔA_{Cl} = Change in Closed Loop Gain

Figure 7.16

VOLTAGE FEEDBACK OP AMP (G = -1, β = 0.5) DC LOOP GAIN, CLOSED LOOP BANDWIDTH, GAIN ACCURACY, AND GAIN STABILITY

Model Number	Closed Loop Bandwidth (MHZ)	Typical DC Loop Gain	Absolute Gain Accuracy (Bits)	Gain Stability Over Temperature (Bits)
AD829	50	25000	14.7	16.7
AD847	25	2000	10	12
AD841	20	20000	14.3	16.3
AD843	16	12000	13.6	15.6
AD845	8	125000	17	19
AD744	6.5	200000	17.7	19.7
OP-27	4	500000	19	21
AD711	1.5	100000	16.7	18.7

Note: $\pm$ 25% DC Loop Gain Variation Over Temperature Assumed

Figure 7.17

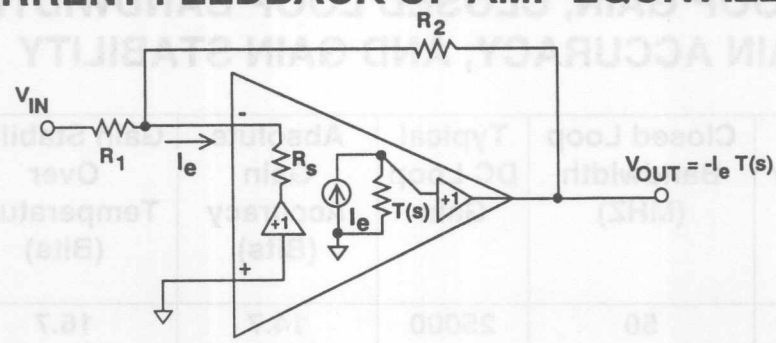
The dc loop gain, absolute gain accuracy (in bits), and closed loop bandwidth for a number of popular voltage feedback amplifiers are given in Figure 7.17 for the unity gain inverting mode.

It is also important that op amp open-loop gain be stable with output signal level. Changes in open-loop gain with signal level produce closed-loop nonlinearity. Amplifiers which have lower initial open loop gains are obviously more sensitive to this effect.

CURRENT FEEDBACK AMPLIFIERS

The equivalent circuit for a current feedback amplifier is shown in Figure 7.18. The signal at the non-inverting input is applied to the inverting input through a unity-gain buffer with an output impedance R_S (usually between 10 and 100Ω). The current entering the inverting input is multiplied by the *transimpedance open loop gain*, T(s), to yield the output voltage. The feedback attenuation factor the current feedback amplifier is different than for the voltage feedback amplifier because of the low inverting input impedance, R_S). Solving the feedback equation yields the transfer function shown in Figure 7.18 The expression for the current feedback amplifier loop gain is different from that for a voltage feedback amplifier, however, it can be used in exactly the same manner in determining the amplifier closed loop accuracy at any frequency.

CURRENT FEEDBACK OP AMP EQUIVALENT CIRCUIT



$$\text{INVERTING SIGNAL GAIN} = -\left(\frac{R_2}{R_1}\right)\left(\frac{1}{1+\frac{1}{LG}}\right) \qquad \text{NON-INVERTING SIGNAL GAIN} = \left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{1+\frac{1}{LG}}\right)$$

T(s) = OPEN LOOP TRANSIMPEDANCE GAIN

$$\beta_{cf} = \text{FEEDBACK FACTOR} = \frac{R_S \| R_1}{R_S \| R_1 + R_2}$$

$$A_{cf}(s) = \text{OPEN LOOP VOLTAGE GAIN} = \frac{T(s)}{R_S}$$

$$\text{LOOP GAIN} = LG = A_{cf}(s)\,\beta_{cf} = \frac{T(s)\{R_S \| R_1\}}{R_S\{R_S \| R_1 + R_2\}}$$

Figure 7.18

DC GAIN ACCURACY OF CURRENT FEEDBACK AMPLIFIERS

Further examination of the equivalent circuit of the current feedback amplifier reveal that the small error current, I_e, flows into the low impedance (R_S) inverting input of the amplifier and is multiplied by the open loop transimpedance gain, T_O (expressed in ohms), to give the output voltage. The feedback attenuation factor for the current feedback amplifier is given by $\beta_{cf} = R_S||R_1/\{R_S||R_1 + R_2\}$. The open loop dc voltage gain is given by $A_{cfo} = T_O/R_S$. Notice that if $R_S \rightarrow \infty$, the expression for β_{cf} reduces to $R_1/\{R_1 + R_2\}$ which is the same as for a voltage feedback amplifier. The expression for loop gain shown in Figure 7.18 can be used in exactly the same manner as with a voltage feedback amplifier in determining the gain accuracy and the gain drift.

The dc loop gain, absolute gain accuracy (in bits), and closed loop bandwidth for a number of popular current feedback amplifiers are given in Figure 7.19 for the unity gain inverting mode. The use of the recommended feedback resistor for optimum performance is assumed.

Although the loop gain of the AD9617 is only 2000, the circuit was designed to be extremely stable with signal level as shown in Figure 7.20, where the maximum deviation in dc closed loop gain across the 4V span is only 0.0009% (equivalent to 17 bits linearity).

7

CURRENT FEEDBACK OP AMP (G = -1) DC LOOP GAIN, CLOSED LOOP BANDWIDTH, GAIN ACCURACY, AND GAIN STABILITY

Model Number	Closed Loop Bandwidth (MHZ)	Typical DC Loop Gain	Absolute Gain Accuracy (Bits)	Gain Stability Over Temperature (Bits)
AD9617	190	2000	11	13
AD846	80	182000	17	19
OP-260	55	2600	11.4	13.4
AD844	20	2700	11.4	13.4

Note: ± 25% DC Loop Gain Variation Over Temperature Assumed

Figure 7.19

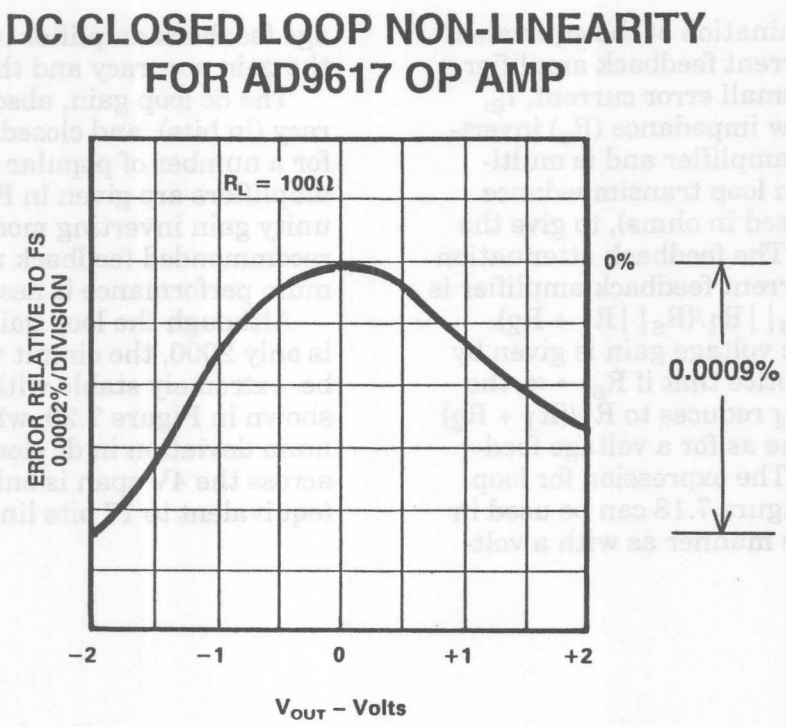


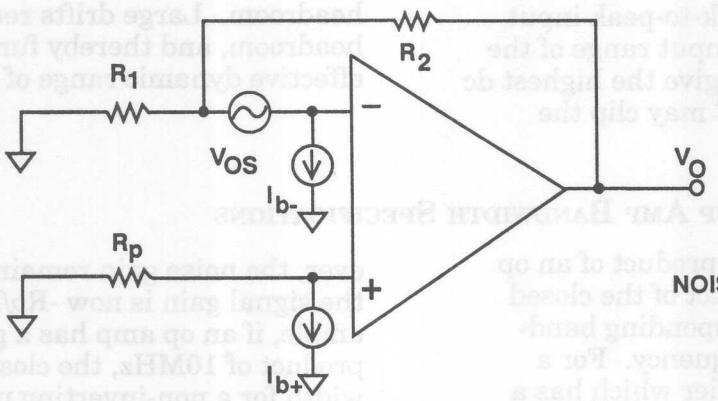
Figure 7.20

CALCULATING TOTAL OUTPUT VOLTAGE OFFSET AND DRIFT OF AN OP AMP

Calculating the dc error components which make up the output voltage offset and drift can be facilitated with the equations shown in Figure 7.21. These equations are applicable for either voltage feedback amplifiers or current feedback amplifiers. However, the inputs of a voltage feedback amplifier are symmetrical; therefore, the input bias currents are approximately equal. Due to the non-symmetrical input structure of the current feedback amplifier, however, the bias currents are usually different, and therefore, appropriate values as given in the data sheet must be used in the equation for I_{b+} and I_{b-}.

The total amplifier output offset voltage and offset voltage drift may then be summed with the dc errors of the ADC to obtain the total dc error. The equations assume that the op amp has infinite open loop gain, and that there is no error created by tolerances or drift in the components comprising the feedback network. In practice, it is common to provide small adjustments for gain and offset to eliminate the need for extremely tight resistor tolerances. Nevertheless, metal film resistors should be used in order to provide good ratio tracking and stability over time and temperature.

OP AMP OUTPUT OFFSET VOLTAGE MODEL



$$V_O = \pm V_{OS}\left[1+\frac{R_2}{R_1}\right] \pm I_{b+}R_p\left[1+\frac{R_2}{R_1}\right] \pm I_{b-}R_2$$

Figure 7.21

LARGE OFFSET SHIFTS REQUIRE GAIN REDUCTION TO PREVENT ADC CLIPPING

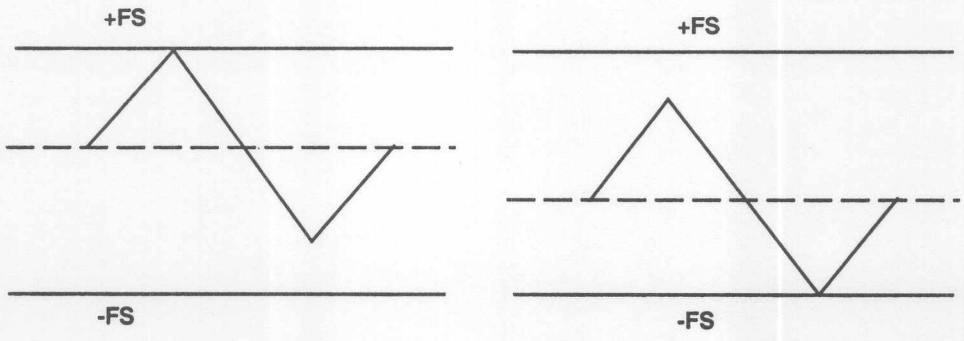


Figure 7.22

EFFECTS OF DC DRIFT ON SYSTEM DYNAMIC RANGE

DC drift in the op amp and the ADC limit the system dynamic range as shown in Figure 7.22. Ideally, the effective gain of the system should be set such that the maximum expected peak-to-peak input signal exactly fills the input range of the ADC. This setting will give the highest dc resolution, but the ADC may clip the fullscale signal if there is sufficient offset and/or gain drift. In order to prevent clipping, therefore, the signal gain is reduced slightly to provide sufficient headroom. Large drifts require more headroom, and thereby further reduce the effective dynamic range of the system.

VOLTAGE FEEDBACK OP AMP BANDWIDTH SPECIFICATIONS

The gain-bandwidth product of an op amp is simply the product of the closed loop gain and the corresponding bandwidth at a specified frequency. For a voltage feedback amplifier which has a single-pole frequency response, this product is constant over a wide range of frequencies (see Figure 7.23). If the op amp is stable at unity gain, the frequency at which the open loop response crosses unity gain is called the unity gain bandwidth frequency. The gain-bandwidth specification may thus be used to calculate the closed-loop bandwidth for various values of closed-loop gain.

A key point often confused in selecting voltage feedback op amps based on bandwidth is that the closed loop gain, A_{cl}, refers to the *noise gain,* $1/\beta$, and not the signal gain (see Figure 7.24). For instance, in the non-inverting mode, the dc signal gain ($1+R_2/R_1$) is equal to the dc noise gain. In the inverting mode, however, the noise gain remains $1+R_2/R_1$, but the signal gain is now $-R_2/R_1$. For example, if an op amp has a gain-bandwidth product of 10MHz, the closed loop bandwidth for a non-inverting unity gain configuration is 10MHz, while that of a unity-gain inverter is only 5MHz.

Another important point is that some op amps are optimized to operate at high gains, and are not stable under low- or unity-gain conditions. With these op amps, the gain-bandwidth product is meaningful only over the region of stable closed loop gains. This type of amplifier can, however, be used at low inverting signal gains by the addition of a shunt resistor to ground as shown in Figure 7.25. The extra resistor is chosen such that the noise gain is greater than the minimum value required for stability. The penalty is increased sensitivity to input offset voltage and input noise voltage as well as lower signal bandwidth.

LOG-LOG BODE PLOT FOR VOLTAGE FEEDBACK OP AMP

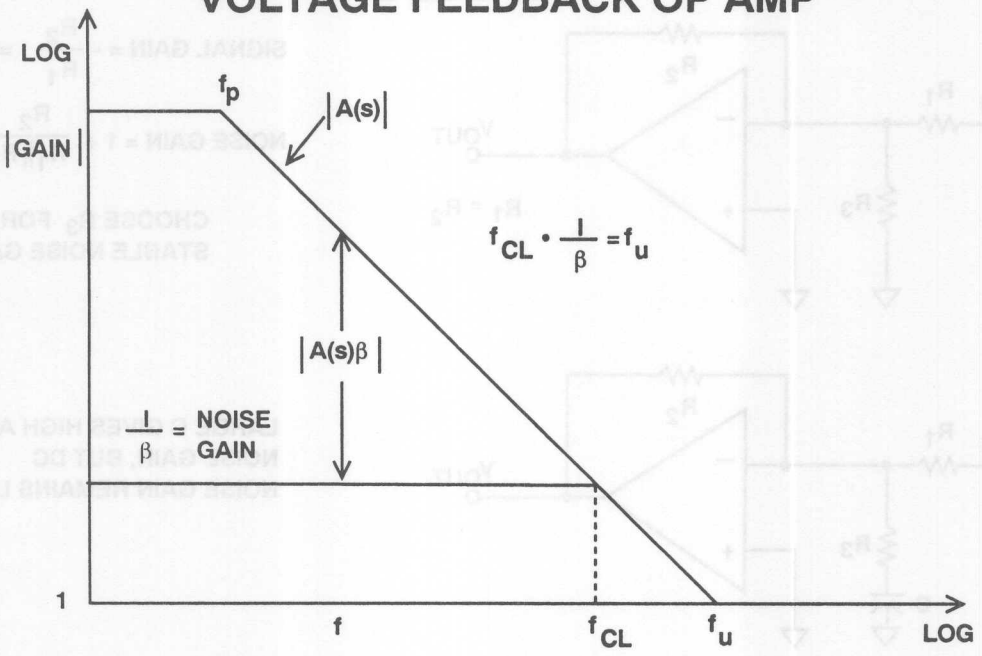
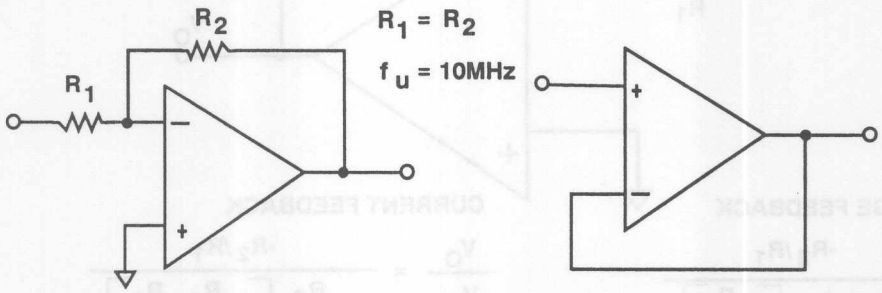


Figure 7.23

7

RELATIONSHIP BETWEEN NOISE GAIN, SIGNAL GAIN, AND BANDWIDTH FOR OP AMP WITH UNITY GAIN BW OF 10MHz



NOISE GAIN = $\frac{1}{\beta} = 1 + \frac{R_2}{R_1} = 2$

SIGNAL BW = 5MHz

SIGNAL GAIN = -1

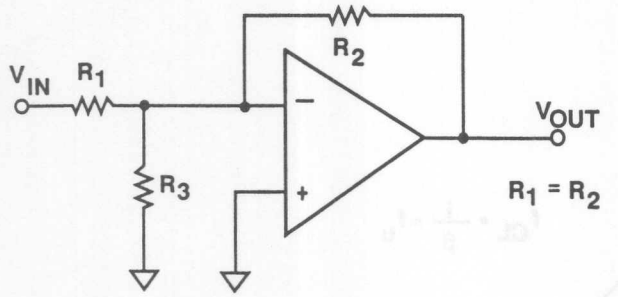
NOISE GAIN = 1

SIGNAL BW = 10MHz

SIGNAL GAIN = +1

Figure 7.24

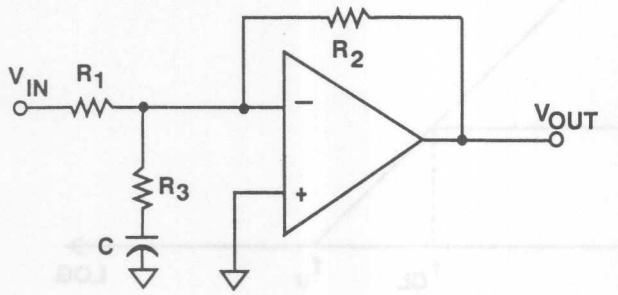
OPERATING NON-UNITY GAIN STABLE OP AMPS AT UNITY GAIN IN THE INVERTING MODE



$$\text{SIGNAL GAIN} = -\frac{R_2}{R_1} = -1$$

$$\text{NOISE GAIN} = 1 + \frac{R_2}{R_1 \| R_3}$$

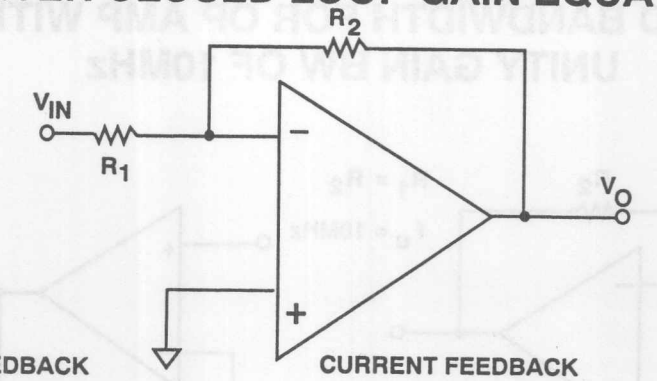
CHOOSE R_3 FOR MINIMUM STABLE NOISE GAIN



LARGE C GIVES HIGH AC NOISE GAIN, BUT DC NOISE GAIN REMAINS LOW

Figure 7.25

VOLTAGE FEEDBACK AND CURRENT FEEDBACK INVERTER CLOSED LOOP GAIN EQUATIONS



VOLTAGE FEEDBACK

$$\frac{V_O}{V_{IN}} = \frac{-R_2/R_1}{1 + \frac{1}{A(s)}\left[1 + \frac{R_2}{R_1}\right]}$$

CURRENT FEEDBACK

$$\frac{V_O}{V_{IN}} = \frac{-R_2/R_1}{1 + \frac{R_2}{T(s)}\left[1 + \frac{R_s}{R_1} + \frac{R_s}{R_2}\right]}$$

ASSUME $R_s << R_1$ AND R_2 NOTE: R_2 FIXED

$$\frac{V_O}{V_{IN}} \sim \frac{-R_2/R_1}{1 + \frac{R_2}{T(s)}}$$

Figure 7.26

CURRENT FEEDBACK OP AMP BANDWIDTH SPECIFICATIONS

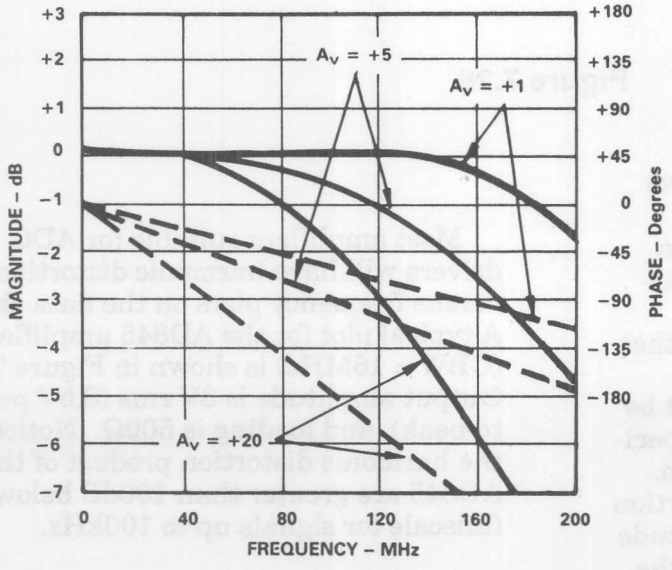
The inverting mode transfer functions for the voltage feedback amplifier and the current feedback amplifier are compared in Figure 7.26. Notice that for the voltage feedback amplifier, the frequency-dependent term, 1/A(s), is multiplied by the noise gain, $(1 + R_2/R_1)$. This implies that the closed loop bandwidth is approximately inversely proportional to the noise gain, hence, the product of the noise gain and the closed loop bandwidth is constant.

In the current feedback amplifier, however, if $R_S << R_1$ and R_2, the closed loop bandwidth is independent of the gain, R_2/R_1, and depends only upon the feedback resistor R_2. Furthermore, most current feedback amplifiers are optimized for best performance for a fixed value of R_2. This implies that the closed loop bandwidth of a current feedback amplifier will remain fairly constant regardless of closed loop gain, provided the gain is changed by varying only R_1.

Current feedback (or transimpedance) op amps therefore have bandwidths which are relatively independent of closed loop gains (assuming a the feedback resistor value remains constant). Therefore, it is inappropriate to refer to the gain-bandwidth product of this type of amplifier. For instance, the signal bandwidth of the AD9617 with a 400Ω feedback resistor is approximately 190MHz for a closed loop signal gain of -1, and approximately 165MHz for a closed loop-signal gain of -5 (see Figure 7.27). In the first case, the so-called gain-bandwidth product would be 190MHz (1 x 190MHz), while in the second case it would be 825MHz (5 x 165MHz). In addition, current feedback amplifiers are usually optimized for a fixed value of feedback resistor. Increasing the feedback resistor lowers the bandwidth proportionally, while decreasing the value may lead to instability. The closed loop signal bandwidth for current feedback amplifiers should therefore be determined from curves on the data sheet.

7

GAIN AND PHASE RESPONSE FOR AD9617 CURRENT FEEDBACK OP AMP



GAIN	BW	PRODUCT
-1	190MHz	190MHz
-5	165MHz	825MHz

Figure 7.27

CALCULATING GAIN ERRORS FOR OP AMPS AS A FUNCTION OF FREQUENCY

Gain error for various input frequencies can be approximated by the useful formula $f_{max} = f_c\sqrt{2\varepsilon}$, where f_c is the op amp (single-pole response assumed) closed loop signal bandwidth, and ε is the amplitude error at frequency f_{max} (Reference 1, p.101). For example, in order for a signal be remain flat within 0.1dB ($\varepsilon = 0.01$) up to a frequency of 50kHz, a minimum closed loop signal bandwidth of 353kHz is required. If an amplitude flatness of 0.1dB is required up to a frequency of 30MHz, a closed loop signal bandwidth of 212MHz is needed.

CALCULATING GAIN ERRORS OVER FREQUENCY

- $f_{max} = f_{cl}\sqrt{2\varepsilon}$
- f_{max} = Maximum Input Frequency for Gain Error < ε
- f_{cl} = Single-Pole Closed-Loop Bandwidth
- Example: For ε = 0.1dB @ f_{max} = 30MHz,

  f_{cl} = 212MHz

Figure 7.28

OP AMP DISTORTION SPECIFICATIONS

In selecting a drive amplifier for an ADC, it is most important that the harmonic distortion performance of the amplifier exceed that of the ADC, so that the op amp does not limit the system SFDR. Distortion specifications must be examined in addition to bandwidth specifications in making the right selection. Ideally, the amplifier harmonic distortion should be measured under the amplitude and loading conditions presented by the ADC.

Most amplifiers suitable for ADC drivers will have harmonic distortion versus frequency plots on the data sheet. A typical plot for the AD845 amplifier (GBW = 16MHz) is shown in Figure 7.29. Output amplitude is 3V rms (8.5V peak-to-peak), and loading is 500Ω. Notice that the harmonic distortion product of the AD845 are greater than 100dB below fullscale for signals up to 100kHz.

AD845 HARMONIC DISTORTION
Vout = 3V rms, Rload = 500Ω

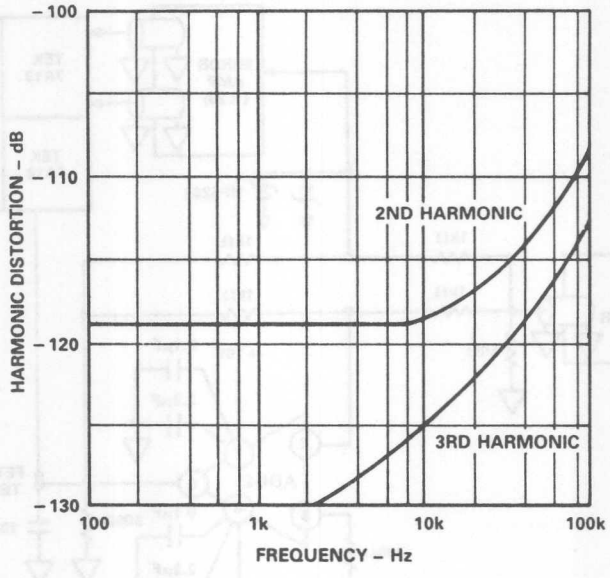


Figure 7.29

7

OP AMP SETTLING TIME SPECIFICATIONS

Settling time is especially important in applications such as pulse-height analysis where the amplitude of pulses must be measured accurately. Other applications requiring fast settling time are in multiplexer output buffering and CCD Imaging. Measuring settling time directly with a standard oscilloscope is difficult because the scope is severely overdriven. Therefore, settling time measurements in the inverting mode usually utilize a circuit such as that shown in Figure 7.30 for measuring the settling time of the AD845 (see Figure 7.31). The error signal generated at the false summing junction is much less likely to overdrive the scope.

Special digital sampling oscilloscopes such as the Data Precision mainframe with the 640 digitizing plug-in can be used to measure settling time directly as shown in Figure 7.32 for the AD9617 current feedback amplifier.

SETTLING TIME TEST SETUP FOR AD845

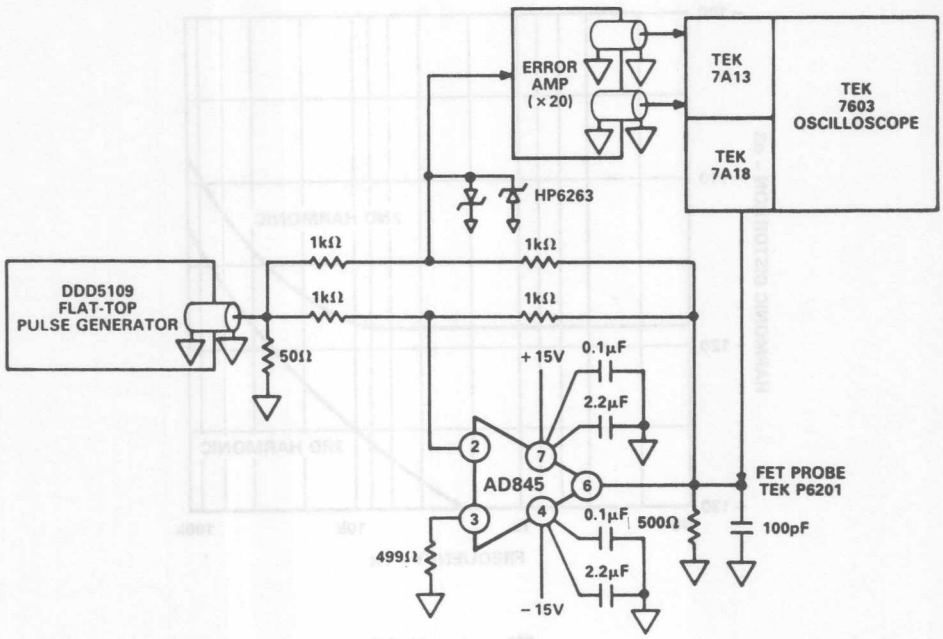


Figure 7.30

AD845 OP AMP SETTLING TIME

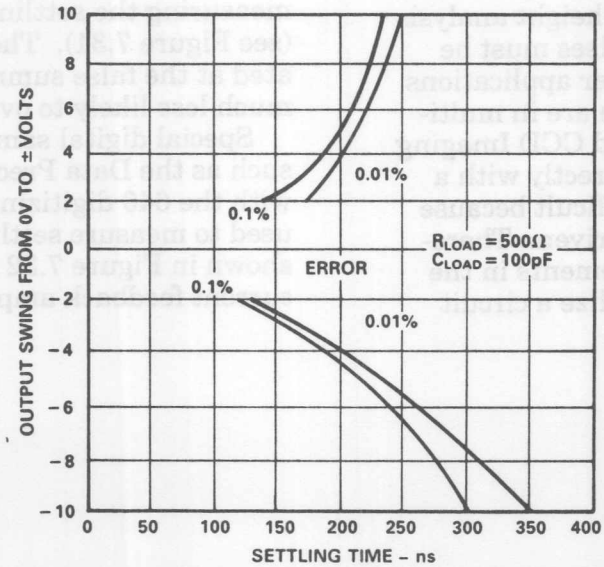


Figure 7.31

AD9617 SETTLING TIME MEASURED WITH DATA PRECISION 640 DIGITIZING PLUG-IN

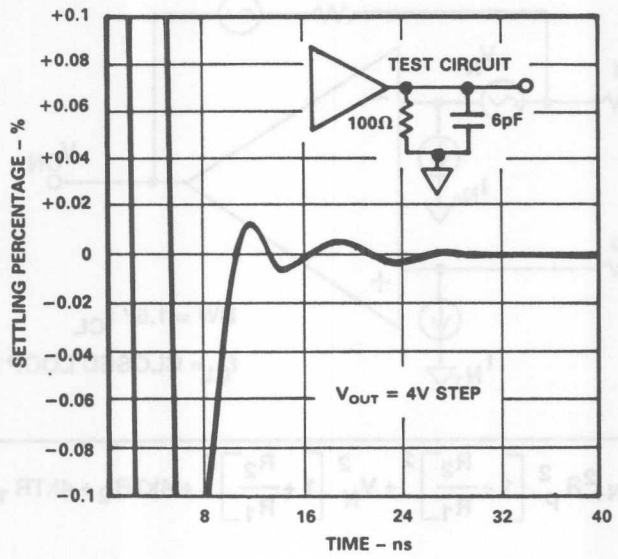


Figure 7.32

7

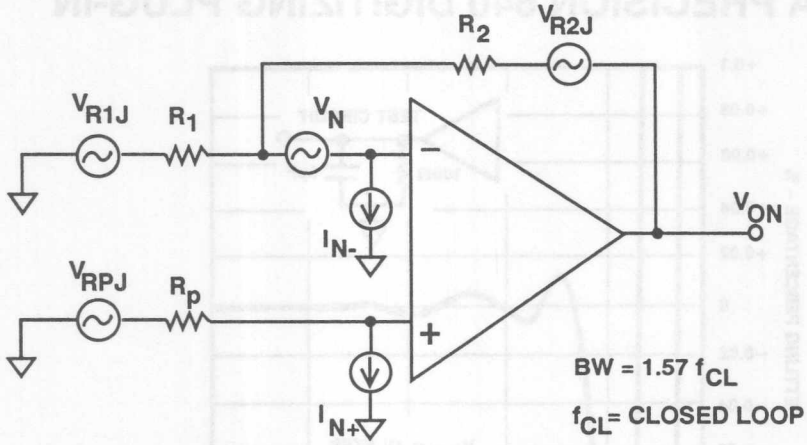
OP AMP NOISE SPECIFICATIONS

Op amp noise performance is usually specified in terms of input voltage noise spectral density and input current noise spectral density. The other source of noise in the op amp circuit is the thermal noise, or Johnson noise, generated by the external resistors. A general model showing all the noise sources is shown in Figure 7.33 along with the equations which reflect these noise components to the op amp output.

Although voltage and current noise spectral densities are not constant across the frequency band, specifically in the 1/f region (see Figure 7.34 for the AD OP-27), reasonable estimates of output noise can be made be made by assuming a nominal value across the entire frequency band of integration (the spectral density values at 1kHz are often used, for example). This assumption is especially true in most ADC applications, where the bandwidth of integration extends over several decades of frequency.

The bandwidth for integration depends on the feedback network and the noise component of interest. In the case of the voltage feedback op amp circuit shown in Figure 7.35, the signal bandwidth is limited by the addition of C_2. The input voltage noise, V_n, the Johnson noise contributed by the resistor R_p, and the non-inverting input current noise, I_{n+}, are multiplied by the circuit ac noise gain $(1 + C_1/C_2)$ and integrated over the entire closed loop noise bandwidth, f_{cl}. However, the output noise generated by resistors R_1 and R_2, and the inverting input current noise, I_{n-}, is integrated only over the signal bandwidth f_2 which is equal to $1/2\pi R_2 C_2$.

OP AMP NOISE MODEL

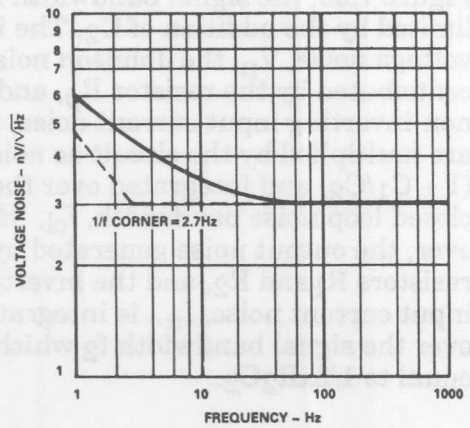


$$V_{ON} = \sqrt{BW}\sqrt{I_{N-}^2 R_2^2 + I_{N+}^2 R_p^2 \left[1+\frac{R_2}{R_1}\right]^2 + V_N^2 \left[1+\frac{R_2}{R_1}\right]^2 + 4kTR_2 + 4kTR_1\left[\frac{R_2}{R_1}\right]^2 + 4kTR_p\left[1+\frac{R_2}{R_1}\right]^2}$$

Figure 7.33

INPUT NOISE SPECTRAL DENSITIES FOR ADOP-27 BIPOLAR 8MHz OP AMP

VOLTAGE NOISE



CURRENT NOISE

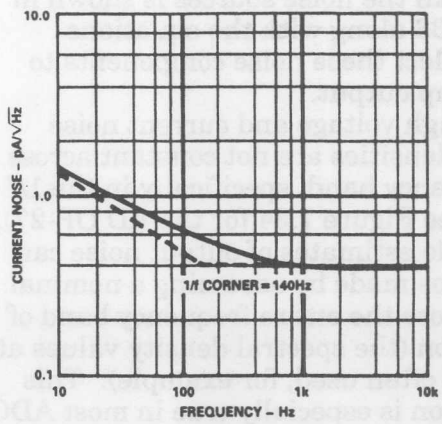
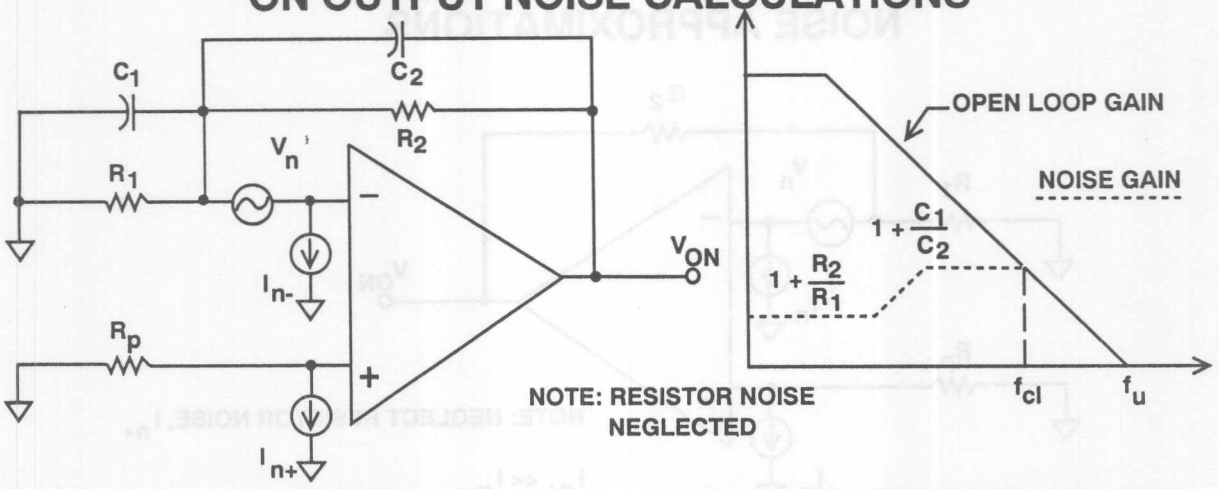


Figure 7.34

EFFECTS OF NOISE GAIN ON OUTPUT NOISE CALCULATIONS



$$V_{ON} \sim \sqrt{V_n^2 \left[1 + \frac{C_1}{C_2}\right]^2 (1.57\, f_{cl}) + I_{n-}^2 R_2^2 (1.57 f_2) + I_{n+}^2 R_p^2 \left[1 + \frac{C_1}{C_2}\right]^2 (1.57 f_{cl})}$$

Where f_u = Op Amp Unity Gain Bandwidth Frequency

$$f_{cl} = \text{Closed Loop Bandwidth} = \frac{f_u}{1 + \frac{C_1}{C_2}}, \quad f_2 = \text{Signal Bandwidth} = \frac{1}{2\pi R_2 C_2}$$

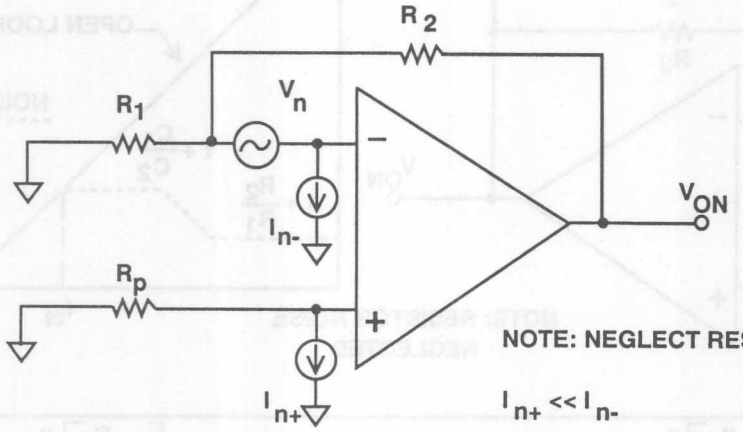
Figure 7.35

The Bode plots of the output noise spectral densities for this circuit are shown in Figure 7.35. The factor of 1.57 in the equations is necessary to convert the single-pole corner frequency to the equivalent noise bandwidth. The total output voltage noise is then obtained by combining each output contributor on an rms basis. Notice that the Johnson resistor noise has been neglected in the equations. This is a valid assumption when working with impedances of less than approximately 10kΩ.

The inverting and non-inverting input current noise for voltage feedback amplifiers is usually equal due to their symmetrical input structure. With current feedback amplifiers, however, the terms are usually different, with the inverting input current noise being the most significant of the two.

With wide bandwidth current feedback amplifiers, the capacitor C_2 is not used, and the bandwidth of integration for all the noise components is the closed loop signal bandwidth. The approximate equations for the calculation of the output noise of a current feedback amplifier are given in Figure 7.36.

CURRENT FEEDBACK OP AMP OUTPUT NOISE APPROXIMATIONS



NOTE: NEGLECT RESISTOR NOISE, I_{n+}

$I_{n+} << I_{n-}$

$$V_{ON} = \sqrt{1.57\, f_{cl}} \sqrt{V_n^2 \left[1 + \frac{R_2}{R_1}\right]^2 I_{n-}^2 R_2^2}$$

f_{cl} = Op Amp Closed Loop Bandwidth

Figure 7.36

INPUT BANDWIDTH OF ADCs

ADC	Resolution	Maximum Sampling Rate	Input Bandwidth
AD9006	6	500MSPS	550MHz
AD9028/9038	8	300MSPS	250MHz
AD9060	10	75MSPS	175MHz
AD1674	12	100kSPS	1MHz
AD7886	12	750kSPS	20MHz
AD1671	12	1MSPS	2MHz
AD9005A	12	10MSPS	40MHz
AD9032	12	25MSPS	150MHz
AD7871	14	83kSPS	3MHz
AD679	14	100kSPS	1MHz
AD9014	14	10MSPS	60MHz
AD676	16	100kSPS	1MHz
AD7874	16	166kSPS	3MHz
AD1382	16	500kSPS	2.2MHz

Figure 7.37

EFFECTS OF ADC INPUT BANDWIDTH ON AMPLIFIER OUTPUT NOISE

Most of todays sampling ADCs have input bandwidths which far exceed the Nyquist bandwidth, $f_S/2$. This is illustrated in Figure 7.37 for a number of popular sampling ADCs. For a first order approximation, assume that the input bandwidth of the ADC is a single pole filter. This filter may therefore limit the bandwidth of integration for the op amp total output noise voltage.

SPECIFYING THE ANTIALIASING FILTER

Properly specifying the antialiasing filter requires a knowledge of the signal's spectral characteristics as well as the system dynamic range requirements. Consider the case of a signal which has a maximum fullscale frequency content of f_a = 35kHz sampled at a rate of f_S=100kSPS. Assume the signal has the spectrum shown in Figure 7.38 and is attenuated by 30dB at 65kHz (f_S- f_a). Observe that the system dynamic range is limited to 30dB at 35kHz because of the aliased components.

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ANTIALIASING FILTER EFFECTS ON DYNAMIC RANGE

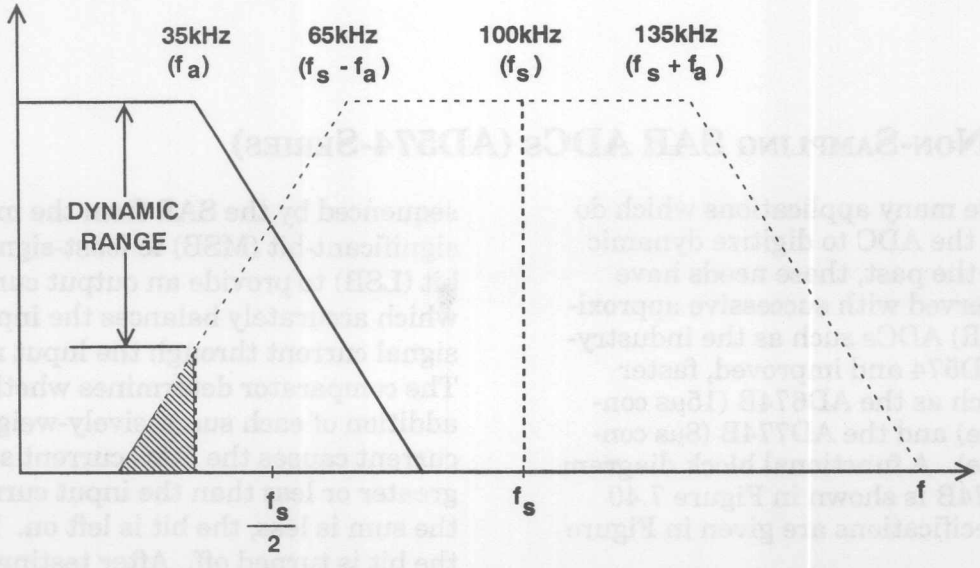


Figure 7.38

If additional dynamic range is required, an antialiasing filter must be provided to provide more attenuation at 65kHz). If a dynamic range of 74dB (12 bits) at 35kHz is desired, then the antialiasing filter attenuation must go from 0dB at 35kHz to 44dB at 65kHz. This is an attenuation of 44dB in approximately one octave, therefore, a 7 pole filter is required. (Each filter pole provides approximately 6dB attenuation per octave).

One must also consider that broadband noise may be present with the signal which can also alias within the bandwidth of interest. This is especially true with wideband op amps which provide low distortion levels.

POSITIONING THE ANTIALIASING FILTER FOR OPTIMUM SYSTEM NOISE PERFORMANCE

For lower frequency antialiasing filters (up to about 200kHz), active filters offer an attractive alternative to traditional passive filters (See Section 6 for further discussions of active filter design). The output of an active filter is usually taken from the final stage op amp in the filter. This final stage should be capable of driving the ADC at the appropriate level and at an acceptable noise and distortion level. Remember that the output noise spectral density of the final stage driving the ADC must be integrated over the entire front-end ADC bandwidth. In most cases, the ADC bandwidth is considerably more than that of the maximum signal of interest.

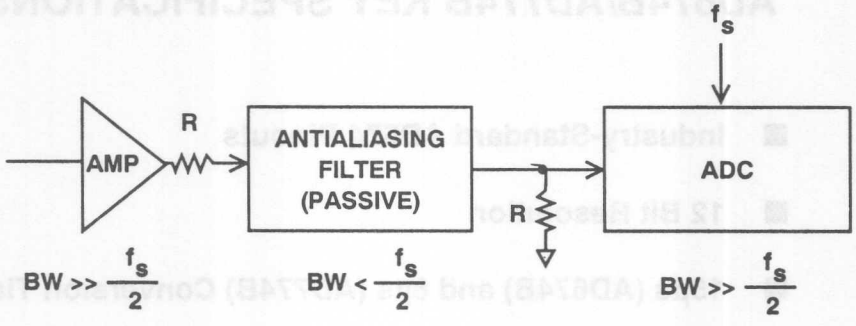
Higher frequency passive filters are usually designed to have impedances between 50 and 100Ω. The input characteristics of the ADC must be fully understood in order to correctly place these filters. If the input of the ADC is a fairly high impedance with low capacitance (relative to the filter impedance), it is better to place the antialiasing filter directly ahead of the ADC as shown in Figure 7.39. This configuration is advantageous because the output noise of the drive amplifier is now bandlimited by the filter.

DRIVING NON-SAMPLING SAR ADCS (AD574-SERIES)

There are many applications which do not require the ADC to digitize dynamic signals. In the past, these needs have been well-served with successive approximation (SAR) ADCs such as the industry-standard AD574 and improved, faster versions such as the AD674B (15μs conversion time) and the AD774B (8μs conversion time). A functional block diagram of the AD774B is shown in Figure 7.40 and key specifications are given in Figure 7.41.

A simplified block diagram of the SAR ADC and the drive amp is shown in Figure 7.42. During the conversion cycle, the internal 12 bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current. If the sum is less, the bit is left on. If more, the bit is turned off. After testing all the bits, the SAR contains a 12 bit binary code which accurately represents the input signal to within ± 1/2 LSB. The ADC input current is thereby modulated by the

ANTIALIASING FILTER REDUCES OP AMP OUTPUT NOISE WHEN DRIVING ADCs WITH LARGE BANDWIDTHS



OP AMP OUTPUT NOISE INTEGRATED OVER FILTER BW, NOT ADC BW

Figure 7.39

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AD674B/AD774B SAR ADC ENCODER BLOCK DIAGRAM

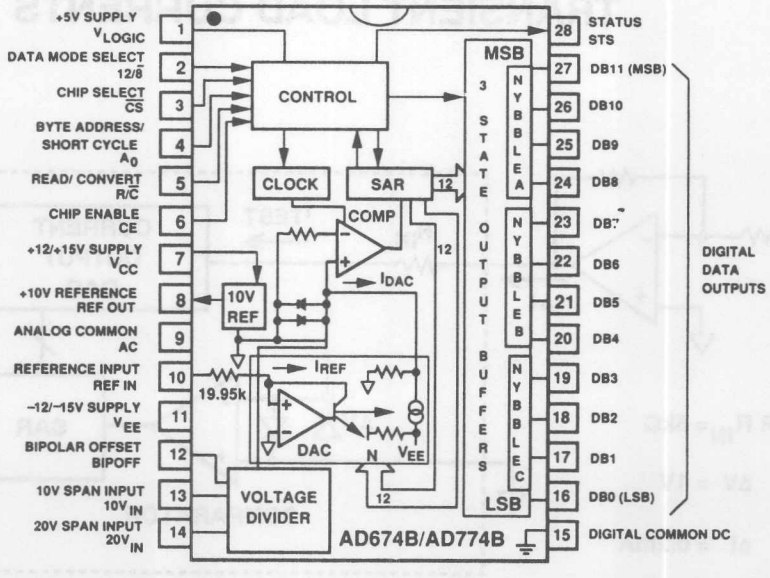


Figure 7.40

AD674B/AD774B KEY SPECIFICATIONS

- Industry-Standard AD574 Pinouts
- 12 Bit Resolution
- 15μs (AD674B) and 8μs (AD774B) Conversion Time
- 375mW Power Dissipation (±15 Volt Supplies)

Figure 7.41

SAR ADC ENCODER INPUT TRANSIENT LOAD CURRENTS

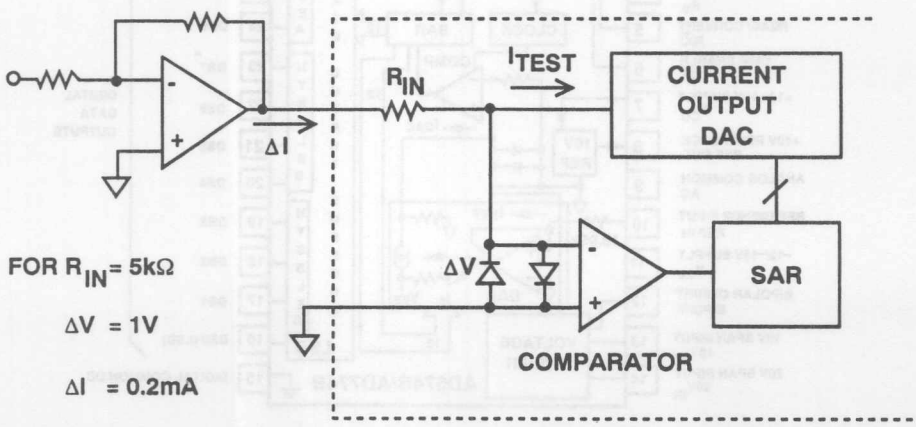


Figure 7.42

DAC test current at a frequency which is equal to the internal clock rate. Each time the internal DAC is switched, transient voltages of a few hundred millivolts may occur across the clamping diodes. For example, a 1V transient across the 5kΩ input resistance produces a transient load current of 0.2mA which must be supplied by the drive op amp.

The 12 bit AD774B has a total conversion time of 8μs. The internal SAR clock frequency is approximately 1.5MHz corresponding to a period of 670ns. Therefore, the output of the drive amp must settle to better than12 bit accuracy (± 1/2 LSB = ±1.2mV for a 10V input range) in less than 670ns after the application of the transient load current. The following discussion will aid in estimating the settling time of op amps to these transient load currents.

The closed loop output impedance of op amps increases with frequency (as shown in Figure 7.43 for the AD845) and may be as great as several hundred ohms at high frequencies due to the equivalent output inductance of the complementary emitter follower output stage. The transient load current will develop a transient voltage across this impedance at the op amp output. This small-signal voltage perturbation will exponentially decay with a time constant equal to $1/2\pi f_{cl}$ (f_{cl} = closed loop bandwidth) if the op amp exhibits single pole response (see Figure 7.44). The simple exponential decay formula can be used to determine the settling to any desired accuracy.

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AD845 CLOSED LOOP OUTPUT IMPEDANCE

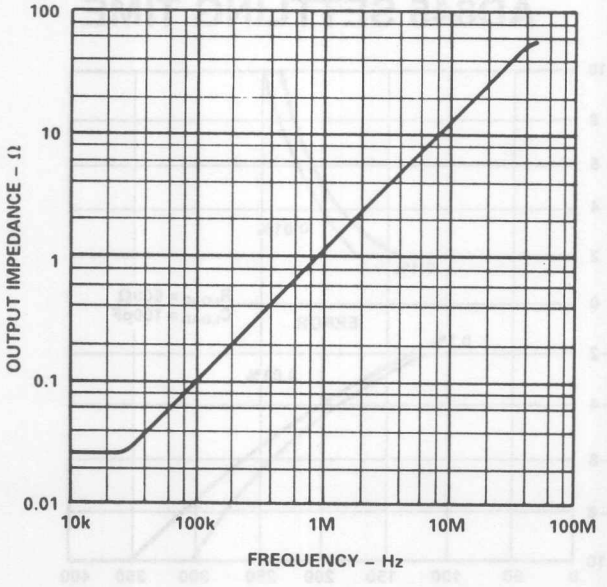


Figure 7.43

SMALL SIGNAL MODEL ALLOWS YOU TO ESTIMATE OP AMP SETTLING TIME DUE TO TRANSIENT LOAD CURRENT

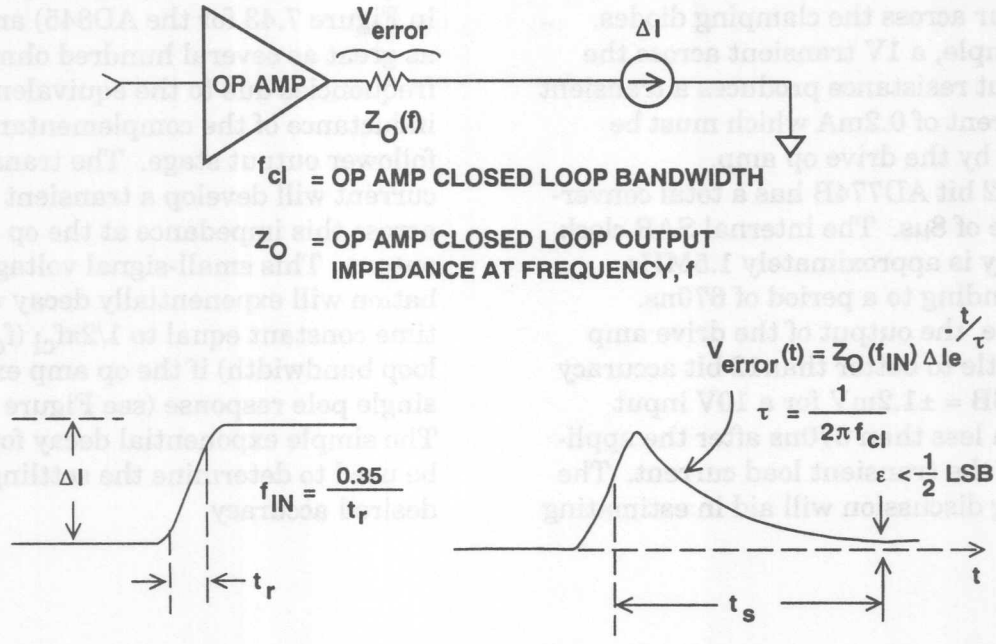


Figure 7.44

AD845 SETTLING TIME

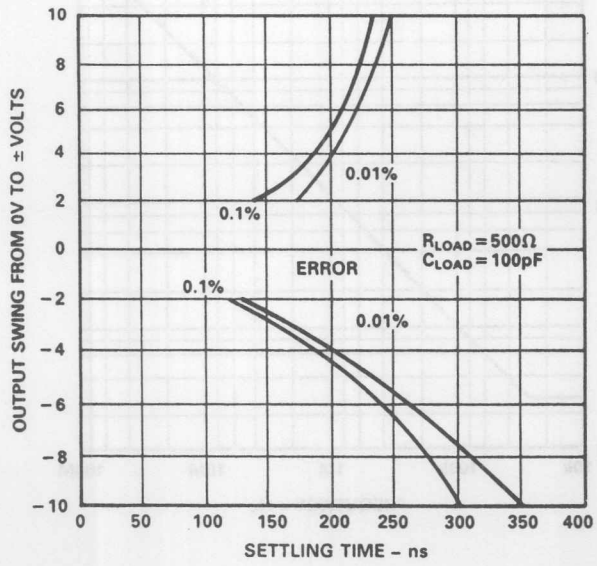


Figure 7.45

A more conservative approach is to examine the actual small signal settling time of the op amp with respect to the internal SAR clock period. Settling times for various output pulse amplitudes to various accuracies for the AD845 is shown in Figure 7.45. Curves such as these may be used to evaluate the amplifier response to transient load currents, and are particularly useful if the transient load currents are large.

The AD845 is a precision CBFET op amp which has a bandwidth of 16MHz, a small signal settling time of less than 200ns to 0.01%, and an open loop gain of 250,000. It is therefore ideally suited to driving precision ADCs with resolutions up to 16 bits. Key specifications for the AD845 are shown in Figure 7.46.

A much less attractive alternative to selecting the proper precision fast-settling op amp is to heavily bypass the ADC input heavily as shown in Figure 7.47. The capacitor must be large enough that the transient current causes its voltage to change by less than 1/2 LSB (1.2mV for a 12 bit ADC with a 10V input range) during the 670ns clock period. For the example shown, a 0.22μF capacitor or greater is required. This implies that the driving op amp must be stable for large capacitive loads. Bandwidth is also severely limited by the large capacitor. Selecting a drive amp with sufficient settling time to the transient load current is usually the preferred solution.

There are many cases where a sufficiently accurate model of the SAR ADC input circuit can be derived from data sheet information as in the above example. This simple model may then be used with the op amp Spice macromodel in to evaluate the effects of the ADC transient load currents on the input signal.

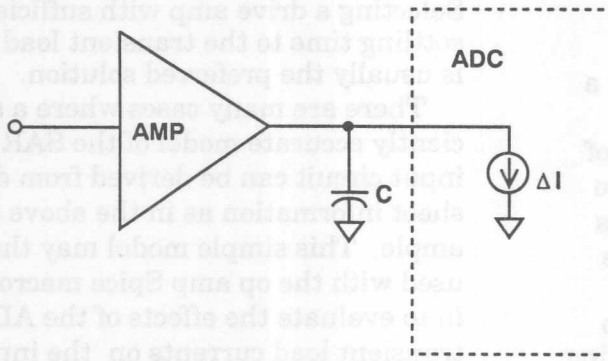
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AD845 CBFET KEY SPECIFICATIONS

- 0.25mV Max Input Offset Voltage
- 5μV/°C Max Offset Voltage Drift
- 0.5nA Input Bias Current
- 350ns Settling Time to 0.01%
- 16MHz Unity-Gain Bandwidth
- 25nV/$\sqrt{Hz}$, 2pA/$\sqrt{Hz}$ Noise at 1kHz

Figure 7.46

BYPASSING ADC INPUT TO ABSORB TRANSIENT LOAD CURRENTS



$$C > \frac{\Delta I \bullet \Delta T}{\Delta V}$$

FOR AD774B SAR ADC:

ΔI = 0.2mA

ΔT = 670 ns

ΔV = 0.6mV (1/4 LSB)

THEN C > 0.22μF

Figure 7.47

DRIVING NON-SAMPLING SUBRANGING ADCS (AD671)

Another popular ADC architecture is called *subranging*. Digital correction is often used to correct for errors made in some of individual conversions required to achieve the total required conversion accuracy. A block diagram of the AD671 subranging 12 bit 500ns ADC is shown in Figure 7.48 and key specifications are given in Figure 7.49.

The analog to digital conversion in the AD671 takes place in four independent steps or flashes. The analog input signal is subranged to an intermediate residue voltage for the final 12 bit result by utilizing multiple flashes with subtraction DACs. Overlap bits correct errors made in the first three steps.

A simplified diagram of the input circuit of the AD671 is shown in Figure 7.50. The signal source driving the ADC must be capable of maintaining the input voltage constant under dynamically-changing load conditions. When the AD671 starts its conversion cycle, the subtraction DAC will sink up to 5mA from the source driving the analog input. The source must respond to this current step by settling the input voltage back to a fraction of an LSB before the final 12 bit decision is made. Unlike SAR ADCs, where the input voltage must settle to a fraction of an LSB before each successive bit decision is made, the AD671 requires the analog input voltage to settle to within 12 bits before the third flash conversion, approximately 200ns. Op amps such as the AD841, AD843, AD845, or the AD847 are suitable for this application.

Figure 7.51 shows a four-channel high-speed data acquisition system utilizing the AD684 quad sample-and-hold (1μs acquisition time to 12 bits), the ADG201HS CMOS Multiplexer (50ns switching time), an AD841 buffer amplifier (110ns settling to 0.01%), an AD588 Reference, and the AD671 ADC (200ns conversion time). The AD684 is config-

AD671 12-BIT, 500ns SUBRANGING ADC ENCODER BLOCK DIAGRAM

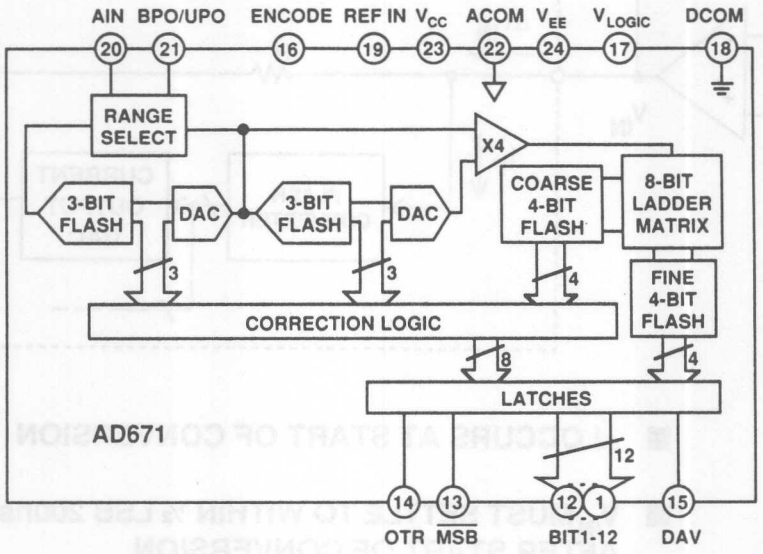


Figure 7.48

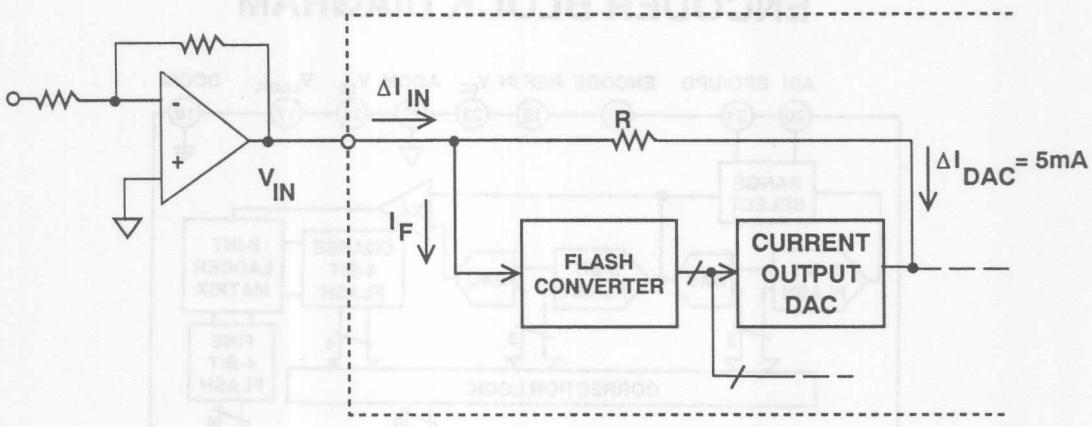
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AD671 ADC KEY SPECIFICATIONS

- 12 Bit Resolution
- 500ns Conversion Time
- Digitally Corrected Subranging Architecture
- Low Power: 475mW
- 24-Pin Skinny DIP Package

Figure 7.49

AD671 EQUIVALENT INPUT CIRCUIT



- ΔI OCCURS AT START OF CONVERSION
- V_{IN} MUST SETTLE TO WITHIN ½ LSB 200ns AFTER START OF CONVERSION

Figure 7.50

500kSPS DATA ACQUISITION SYSTEM

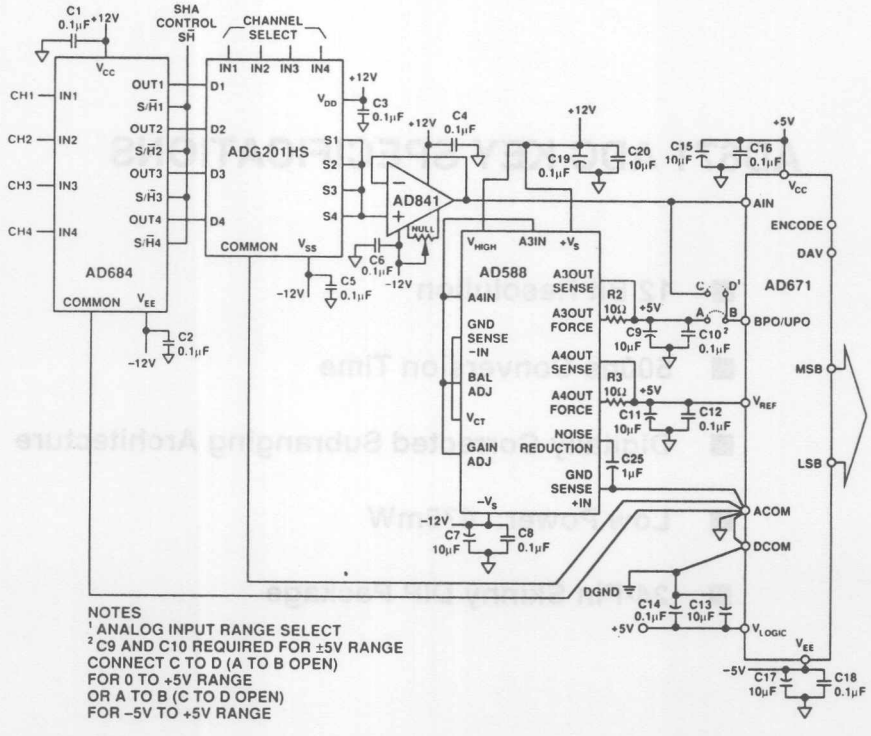


Figure 7.51

ured to sample four analog inputs simultaneously. Each held analog input voltage is then selected by the multiplexer and buffered by the AD841. The multiplexer can be switched between channels every 250ns, therefore the four analog inputs may be simultaneously sampled in a period of approximately 1μs. The minimum total sampling interval is therefore the sum of the SHA acquisition time (1μs) and the total conversion time for the four channels (1μs), or approximately 2μs. This corresponds to a simultaneous input sampling rate of approximately 500kHz.

DRIVING 12-BIT SAMPLING ADCs (AD1674, AD1671)

Before selecting the drive amplifier for a sampling ADC, the characteristics of the particular ADC under consideration must be examined. There are many different possible input architectures. Some produce more transient load current than others. AC performance specifications may differ considerably. For these reasons, it is somewhat difficult to generalize the amplifier selection process. There is, however, an underlying principle that the amplifier should not degrade either the DC or the AC specifications of the sampling ADC significantly.

The AD1674 is a complete 12 bit 100kSPS sampling ADC with user-transparent on-board SHA, reference, and clock. The device is pin-compatible with the industry standard AD574A and AD674A and is fully specified for ac parameters. It is ideal for use in both signal processing as well as traditional dc measurement applications. A block diagram of the AD1674 is shown in Figure 7.53, and key specifications are summarized in Figure 7.54.

7

SELECTING DRIVE AMP BASED ON SAMPLING ADC CHARACTERISTICS

- Analog Input Internal Buffering, Isolation, and Impedance
- Transient Load Currents Injected Into Analog Input
- AC Specifications: S/(N+D), Harmonic Distortion, THD
- Noise Within ADC Bandwidth
- DC Specifications

Figure 7.52

AD1674 12-BIT, 100kSPS SAMPLING ADC BLOCK DIAGRAM

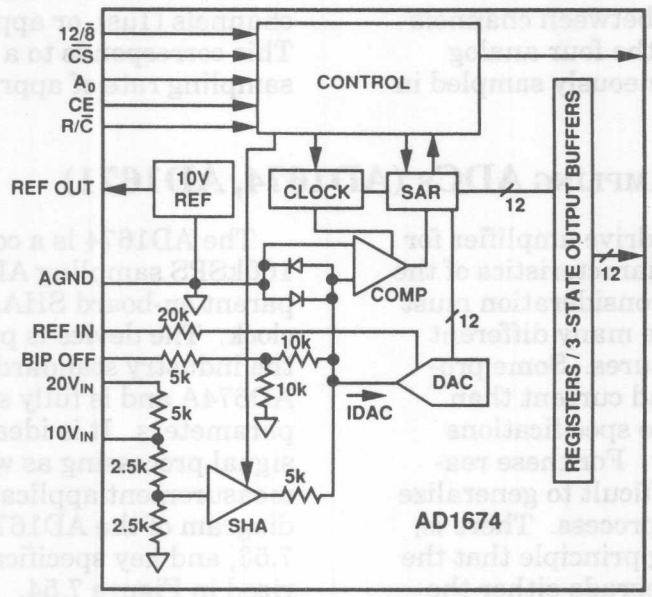


Figure 7.53

AD1674 SAMPLING ADC KEY SPECIFICATIONS

- 12 Bits, 100kSPS Sampling ADC
- Full Power Bandwidth: 1MHz
- 70dB S/(N+D), 90dB THD
- Industry-Standard AD574A Pinouts
- AC and DC Specified and Tested

Figure 7.54

AD1674 12-BIT, 100kSPS SAMPLING ADC DYNAMIC PERFORMANCE

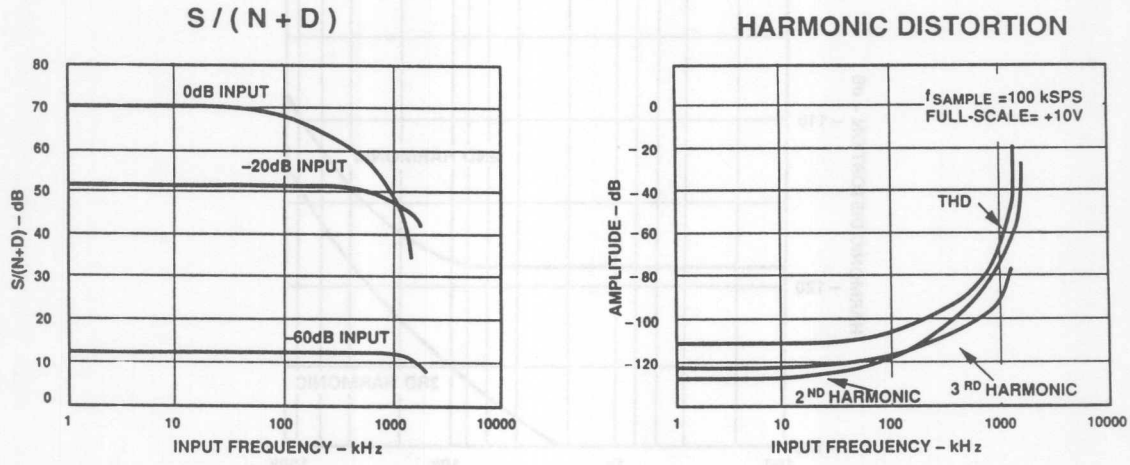


Figure 7.55

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In selecting the appropriate drive amplifier for a sampling ADC such as the AD1674, it is important that the amplifier does not degrade either the AC or the DC specifications of the ADC significantly. Signal-to-Noise plus Distortion, S/(N+D), and harmonic distortion for the AD1674 are shown in Figure 7.55.

These curves can be used as a minimum criterion in establishing the AC performance of the drive op amp. Figure 7.56 shows the harmonic distortion of the AD845 amplifier which is a good choice (but certainly not the only choice!) for driving the AD1674. A simplified block diagram of the internal sample-and-hold circuit is shown in Figure 7.57. This circuit is typical of most SHAs used in sampling ADCs. Because of the high input impedance of the AD1674 internal SHA (5kΩ for 10V range, and 10kΩ for 20V range), SHA switching transients are well-buffered from the drive amplifier.

The AD1671 is a 12 bit 1.25MSPS sampling ADC which is basically an AD671 with an on-board SHA. The device is completely specified in terms of both AC and DC parameters. The AD1671 is fabricated on Analog Devices' ABCMOS process and uses high speed, low noise bipolar circuitry in the linear sections and low power CMOS for the logic sections. Laser trimmed thin film resistors are used to provide accuracy and temperature stability. A functional block diagram of the AD1671 is shown in Figure 7.58, and key specifications are summarized in Figure 7.59.

Because of its high impedance buffered input, the AD1671 presents only a minimal transient current load to the drive amplifier. The AD845 performance is compatible with the S/(N+D) and THD of the AD1671.

AD845 OP AMP HARMONIC DISTORTION
Vout = 3V rms, Rload = 500Ω

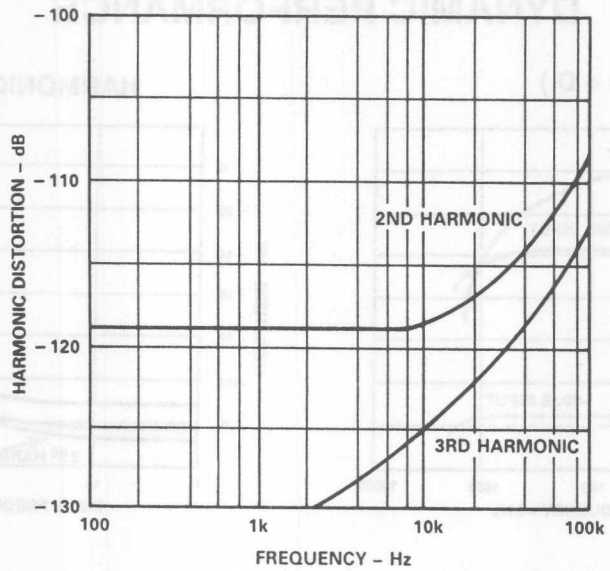


Figure 7.56

AD1674 SAMPLING ADC INPUT CIRCUIT

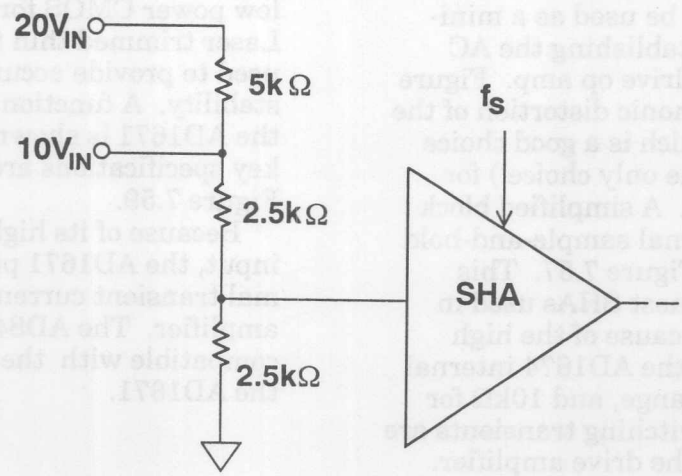


Figure 7.57

AD1671 12-BIT, 1 MSPS DIGITALLY CORRECTED SUBRANGING ADC

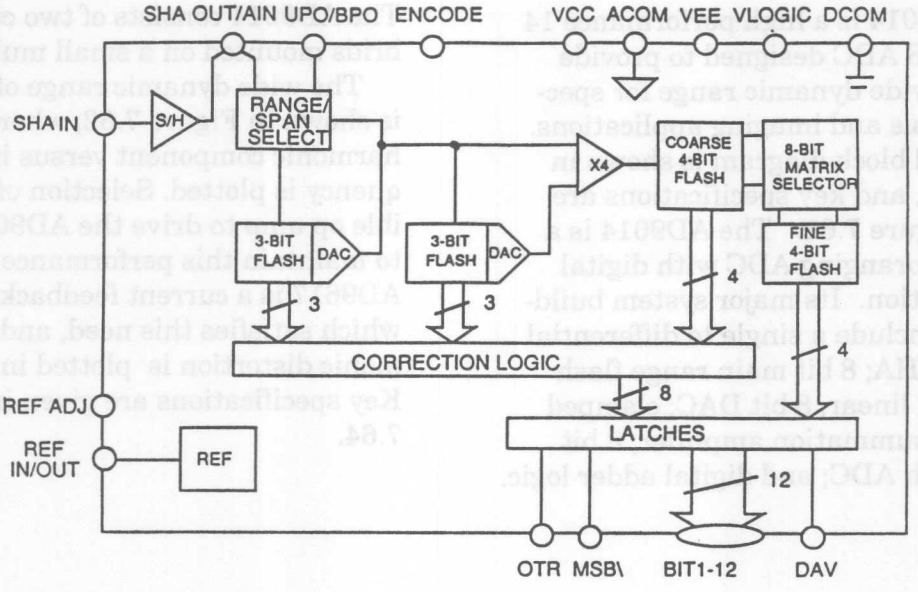


Figure 7.58

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AD1671 SAMPLING ADC KEY SPECIFICATIONS

- 12 Bits, 1.25MSPS
- On-Chip SHA and Voltage Reference
- Full-Power Bandwidth: 2MHz
- 70dB S/(N+D), 80dB THD
- Input Impedance: 10kΩ||10pF, or 10MΩ||10pF
- Low Power Dissipation: 570mW

Figure 7.59

DRIVING A WIDE DYNAMIC RANGE 14 BIT, 10MSPS SAMPLING ADC (AD9014)

The AD9014 is a high performance 14 bit, 10MSPS ADC designed to provide extremely wide dynamic range for spectrum analysis and imaging applications. A simplified block diagram is shown in Figure 7.60, and key specifications are given in Figure 7.61. The AD9014 is a two-step subranging ADC with digital error correction. Its major system building blocks include a single to differential amplifier; SHA; 8 bit main range flash ADC; 16-bit linear, 8 bit DAC; clamped monolithic summation amplifier; 8 bit residue flash ADC; and digital adder logic. The AD9014 consists of two custom hybrids mounted on a small multilayer PCB.

The wide dynamic range of the AD9014 is shown in Figure 7.62, where the largest harmonic component versus input frequency is plotted. Selection of a compatible op amp to drive the AD9014 is critical to maintain this performance level. The AD9617 is a current feedback amplifier which satisfies this need, and its harmonic distortion is plotted in Figure 7.63. Key specifications are given in Figure 7.64.

AD9014 14-BIT, 10MSPS SAMPLING ADC BLOCK DIAGRAM

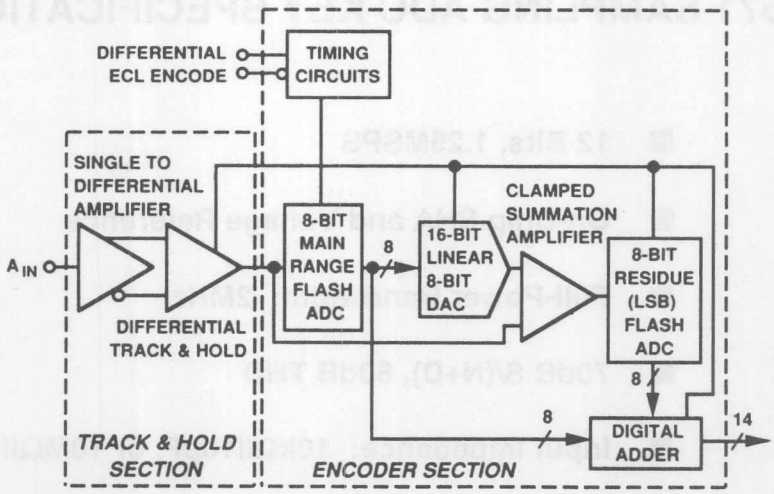


Figure 7.60

AD9014 SAMPLING ADC KEY SPECIFICATIONS

- 14 Bits, 10MSPS Sampling ADC
- 60MHz Full Power Bandwidth
- 92dB Spurious Free Dynamic Range @ 2.3MHz Input, 88dB @ 4.3MHz Input, 72dB @ 10MHz Input
- SNR: 75dB
- 2V p-p Input Range
- Input Impedance: 75Ω||7pF

Figure 7.61

AD9014 HARMONIC DISTORTION

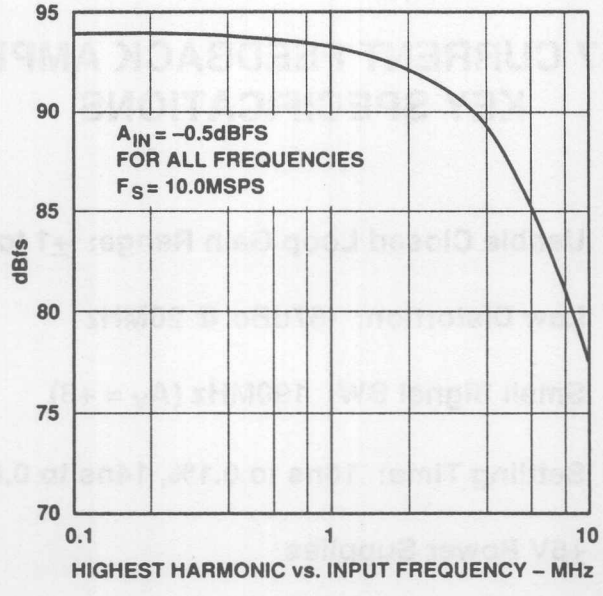


Figure 7.62

AD9617 CURRENT FEEDBACK OP AMP HARMONIC DISTORTION PERFORMANCE

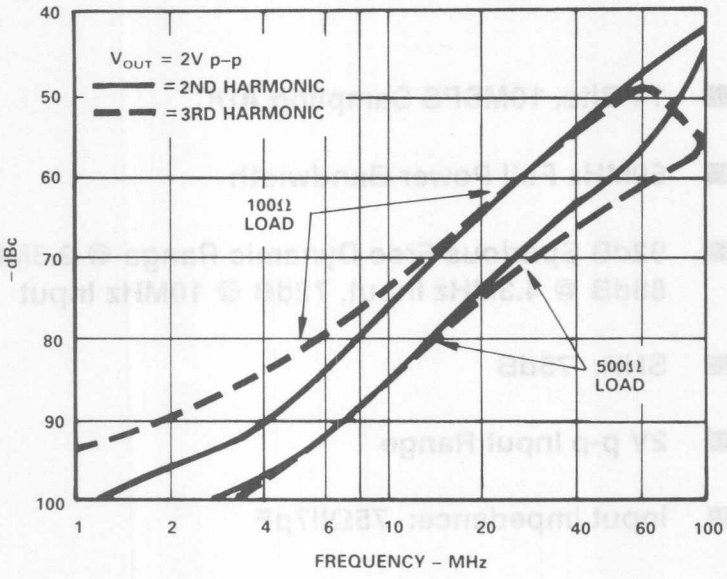


Figure 7.63

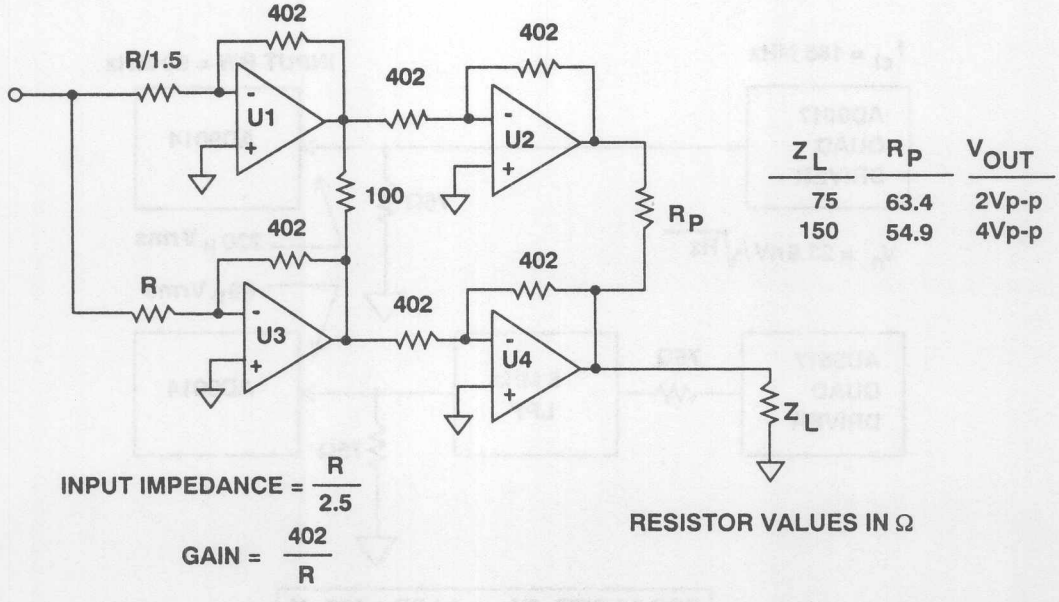
AD9617 CURRENT FEEDBACK AMPLIFIER KEY SPECIFICATIONS

- Usable Closed Loop Gain Range: ±1 to ±40
- Low Distortion: -67dBc @ 20MHz
- Small Signal BW: 190MHz (A_V = +3)
- Settling Time: 10ns to 0.1%, 14ns to 0.02%
- ±5V Power Supplies

Figure 7.64

When gain is required ahead of the AD9014, the circuit shown in Figure 7.65 is recommended in order to give ultra-low distortion levels. This configuration works well for analog input frequencies through 10MHz without introducing spurs that degrade the ADC's dynamic range. At 2.3MHz and 2V p-p output, all spurs generated in the drive circuit are less than -100dBc. The signal path is through U3 and U4, which are set up in a series inverting configuration to cancel even-order harmonics that are generated as the loop gain diminishes with frequency. U1 and U2 reduce the drive current of U3 and U4, respectively. Since U1 and U2 are set up in gains twice that of U3 and U4, the net effect is that the output stages of U3 and U4 are unloaded. This minimizes the odd-order harmonics generated in the output stages of U3 and U4. The gain of the overall block is +402Ω/R, and the input impedance is R/2.5. The output of the amplifier circuit is set up to drive either 2V p-p into 75Ω or 4V p-p into 150Ω by properly selecting R_p.

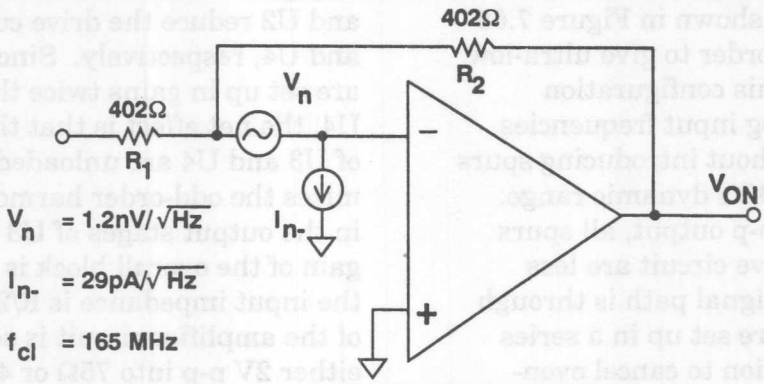
LOW DISTORTION DRIVE CIRCUIT (>100dBc) FOR AD9014 USING AD9617 OP AMPS



Z_L	R_P	V_{OUT}
75	63.4	2Vp-p
150	54.9	4Vp-p

Figure 7.65

AD9617 OUTPUT NOISE SPECTRAL DENSITY



$$V_{ON} = \sqrt{BW}\sqrt{V_n^2\left[1+\frac{R_2}{R_1}\right]^2 I_{n-}^2 R_2^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{(1.2 \times 10^{-9})^2 (2)^2 + (29 \times 10^{-12})^2 (402)^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{5.76 \times 10^{-18} + 136 \times 10^{-18}}$$

$$V_{ON} = \sqrt{BW}\ (11.9nV/\sqrt{Hz})$$

Figure 7.66

REDUCING DRIVER NOISE USING ANTIALIASING FILTER

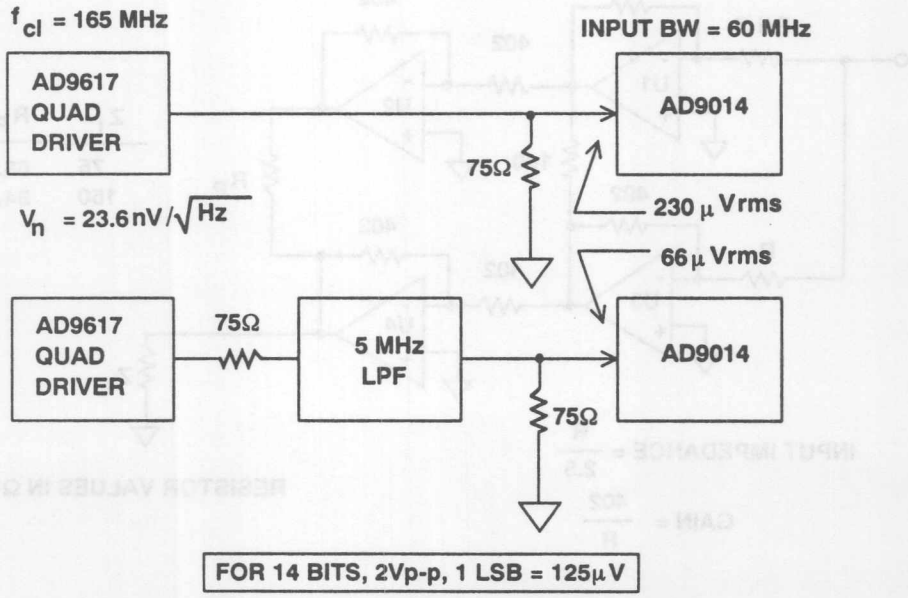


Figure 7.67

The output voltage noise spectral density calculations for a single AD9617 op amp are shown in Figure 7.66. Notice that the inverting input current noise dominates. The equivalent noise bandwidth for integration is the input bandwidth of the AD9014 (60MHz) multiplied by 1.57, or approximately 100MHz. The output voltage noise of the AD9617 integrated over this bandwidth is 119μV rms. The SNR of the AD9617 for a 2V p-p output is therefore 75.5dB, compared to the SNR of the AD9014 of 75dB. The approximate output rms noise of the four op amp drive circuit shown in Figure 7.67 is 230μV rms over the 100MHz equivalent noise bandwidth. This reduces the total SNR to approximately 69dB.

The noise contribution of the op amp drive circuit can be significantly reduced by placing a 75Ω antialiasing filter between the quad driver and the AD9014 as shown in the lower half of Figure 7.67. The gain of the driver circuit must be increased by a factor of two to account for the total attenuation of the filter series and load terminations. If the antialiasing filter is single-pole, and the cutoff frequency is 5MHz, then the output noise of the AD9617 quad driver circuit is reduced by an amount equal to $\sqrt{60/5}$, or 3.46. The rms output noise of the filter is now only 66μV, corresponding to an SNR of 80.6dB. This example dramatically illustrates the noise reduction advantages of placing the antialiasing filter as close to the ADC as possible.

DRIVING HIGH SPEED FLASH CONVERTERS

Driving high speed flash converters presents another set of unique challenges. Most flash converters are designed on bipolar digital processes which makes the addition of low-distortion on-chip buffers difficult. In addition, most flash converters have a fairly large input capacitances which may also be signal-dependent (non linear). The input capacitance is primarily due to the large number of comparators.

A block diagram of the AD9028/AD9038 8-bit, 300MSPS flash converter is shown in Figure 7.69. Notice that the analog input is applied to each of 256 comparators. In reality, the input stage of each comparator is a differential pair. The analog input is applied to one base, and the reference ladder voltage to the other base. The input circuit of the flash converter can be modelled as shown in Figure 7.70. The signal-dependent capacitance is modelled as a reverse-biased diode. The total input capacitance as a function of signal level is also shown in Figure 7.70.

Wideband, low-distortion current feedback amplifiers such as the AD9617 are ideal for driving this type of flash converter. However, a series resistor of approximately 50Ω is required to isolate the amplifier from the flash input capacitance in order to prevent peaking and to maintain stability. Because of the series resistor and the signal-dependent capacitance, harmonic distortion will result as shown in Figure 7.71. The series isolation resistor should therefore be as low as possible in order to maintain op amp stability. Large resistor values will increase the distortion and limit the input bandwidth. Applications information provided on both the amplifier and the flash converter data sheet should be of assistance in selecting the proper resistor value.

DRIVING FLASH CONVERTERS

- **Process Limitations Prevent On-Chip Buffering**
- **Large Input Capacitance May Be Signal-Dependent**
- **Wideband, Low Distortion Amplifiers May Be Unstable With Large Capacitive Loads**
- **Sampling Clock Noise Coupling to Input**

Figure 7.68

AD9028/AD9038 8-BIT, 300MSPS FLASH CONVERTER BLOCK DIAGRAM

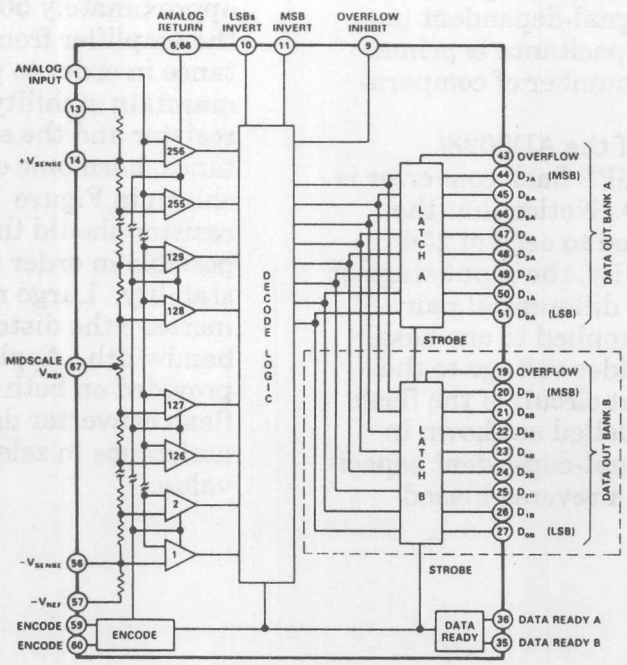


Figure 7.69

AD9028/AD9038 EQUIVALENT INPUT CIRCUIT AND SIGNAL-DEPENDENT CAPACITANCE

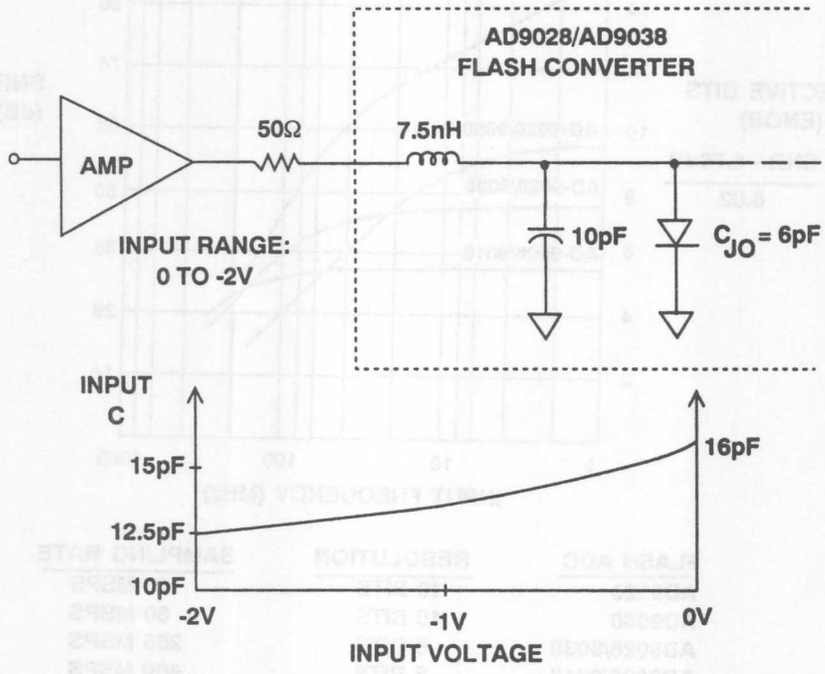


Figure 7.70

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SIMULATED THD DUE TO SIGNAL-DEPENDENT INPUT CAPACITANCE

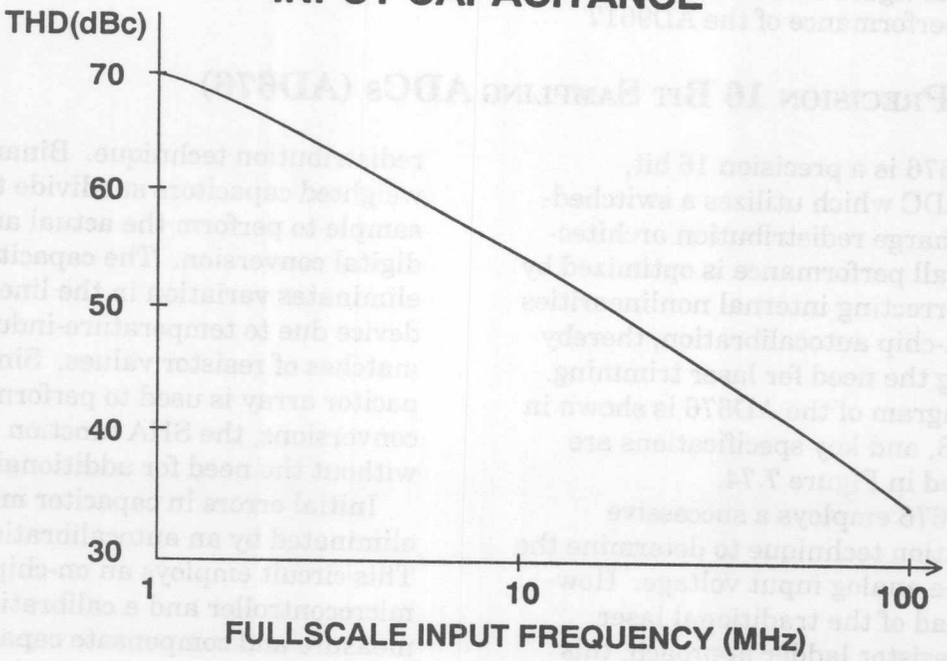
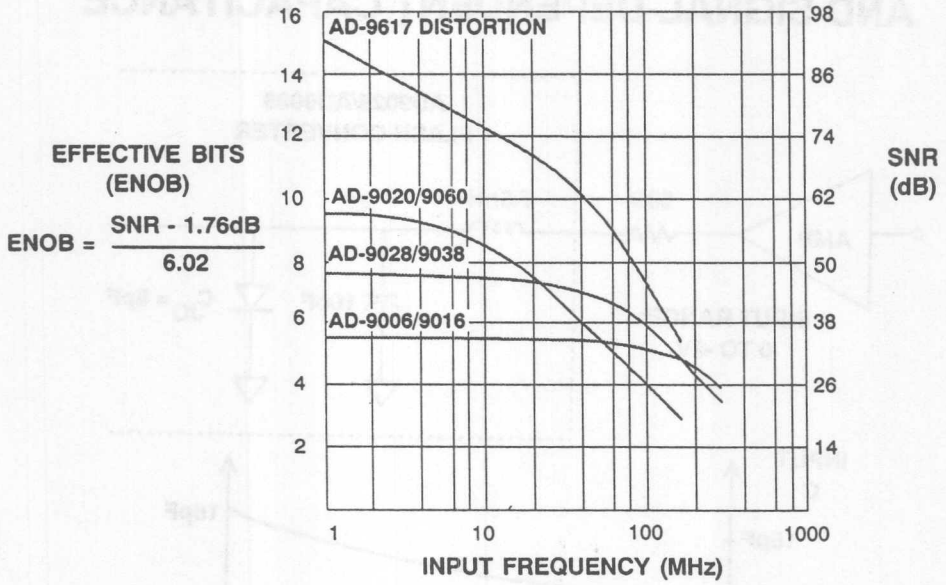


Figure 7.71

FLASH ADC AND OP AMP DYNAMIC PERFORMANCE



FLASH ADC	RESOLUTION	SAMPLING RATE
AD9020	10 BITS	40 MSPS
AD9060	10 BITS	60 MSPS
AD9028/9038	8 BITS	250 MSPS
AD9006/9016	6 BITS	400 MSPS

Figure 7.72

Figure 7.72 shows the SNR and ENOB performance of several flash converters including the AD9028/AD9038. Also shown on the figure is the harmonic distortion performance of the AD9617 current feedback amplifier. Note that the amplifier performance is better than that of the ADCs over a wide range of input frequencies.

DRIVING PRECISION 16 BIT SAMPLING ADCS (AD676)

The AD676 is a precision 16 bit, 100kSPS ADC which utilizes a switched-capacitor charge redistribution architecture. Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration, thereby eliminating the need for laser trimming. A block diagram of the AD676 is shown in Figure 7.73, and key specifications are summarized in Figure 7.74.

The AD676 employs a successive approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser trimmed resistor ladder approach, this device uses a capacitor array, charge redistribution technique. Binary-weighted capacitors subdivide the input sample to perform the actual analog to digital conversion. The capacitor array eliminates variation in the linearity of the device due to temperature-induced mismatches of resistor values. Since a capacitor array is used to perform the data conversions, the SHA function is included without the need for additional circuitry.

Initial errors in capacitor matching are eliminated by an autocalibration circuit. This circuit employs an on-chip microcontroller and a calibration DAC to measure and compensate capacitor mismatch errors. As each error is deter-

AD676 16-BIT, 100kSPS SAMPLING ADC BLOCK DIAGRAM

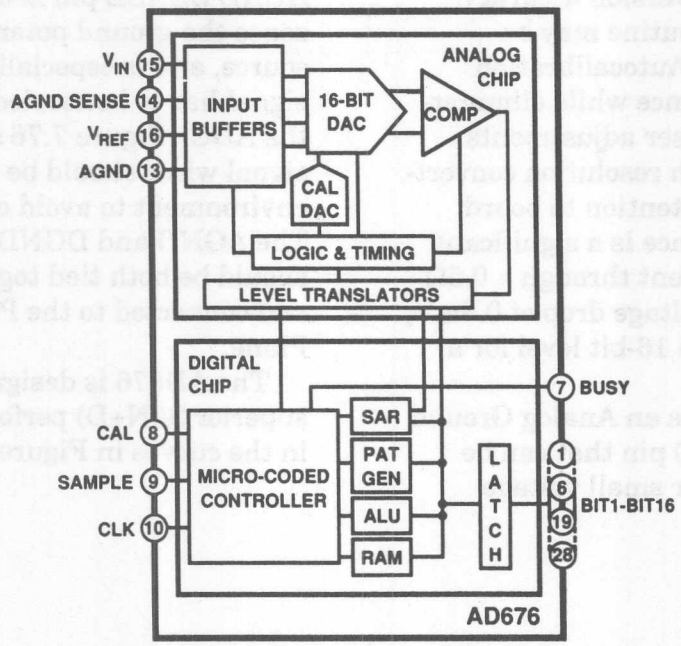


Figure 7.73

7

AD676 ADC KEY SPECIFICATIONS

- 16 Bits, 100kSPS Sampling SAR ADC
- Switched-Capacitor, Charge-Redistribution Architecture
- On-Chip Autocalibration Circuits
- AC and DC Specifications
- ±1 LSB INL
- 90dB S/(N+D)
- 1MHz Full Power Bandwidth
- 95dBc THD

Figure 7.74

mined, its value is stored in on-chip RAM. Subsequent conversions use these RAM values to improve conversion accuracy. The autocalibration routine may be invoked at any time. Autocalibration insures high performance while eliminating the need for any user adjustments.

Designing with high resolution converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22mA current through a 0.5Ω trace will develop a voltage drop of 0.6mV, which is 4 LSBs at the 16-bit level for a 10V fullscale span.

The AD676 provides an Analog Ground Sense (AGND SENSE) pin that can be used to compensate for small voltage drops (<100mV) in the analog input signal return line as shown in Figure 7.75. The AGND SENSE pin is used to remotely sense the ground potential of the signal source, and is especially useful if the signal has to be carried some distance to the ADC. Figure 7.76 shows how the signal wires should be shielded in a noisy environment to avoid capacitive coupling. The AGND and DGND of the AD676 should be both tied together at the device and connected to the PCB Analog Ground Plane.

The AD676 is designed to provide superior S/(N+D) performance as shown in the curves in Figure 7.77.

AD676 AGND SENSE PIN CONNECTIONS

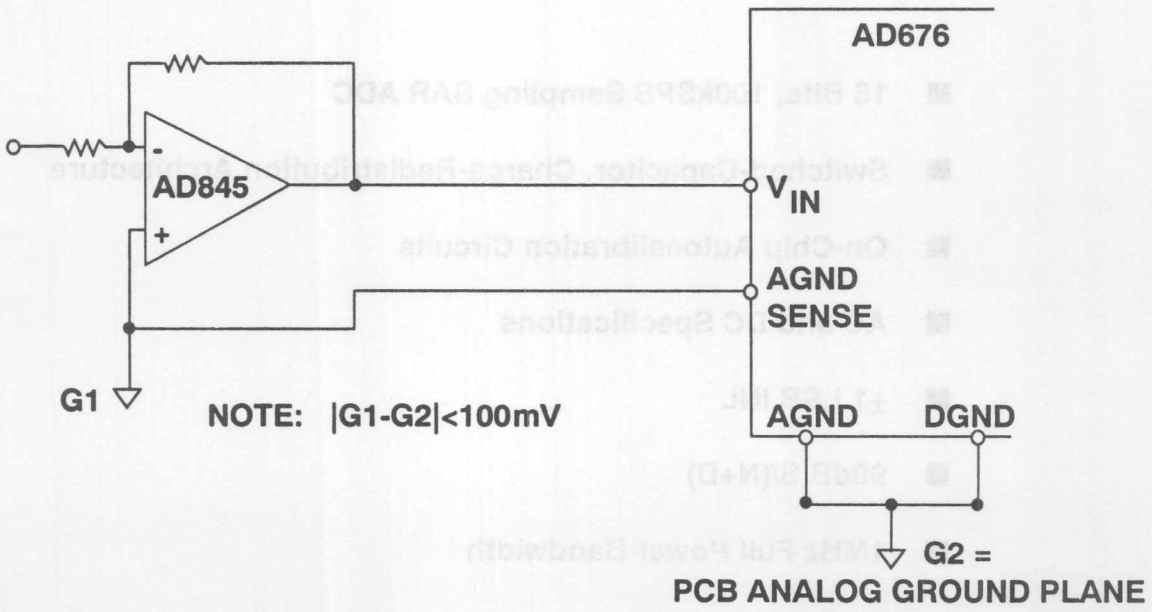


Figure 7.75

AD676 AGND SENSE PIN CONNECTIONS FOR SHIELDED TWISTED PAIR CABLE

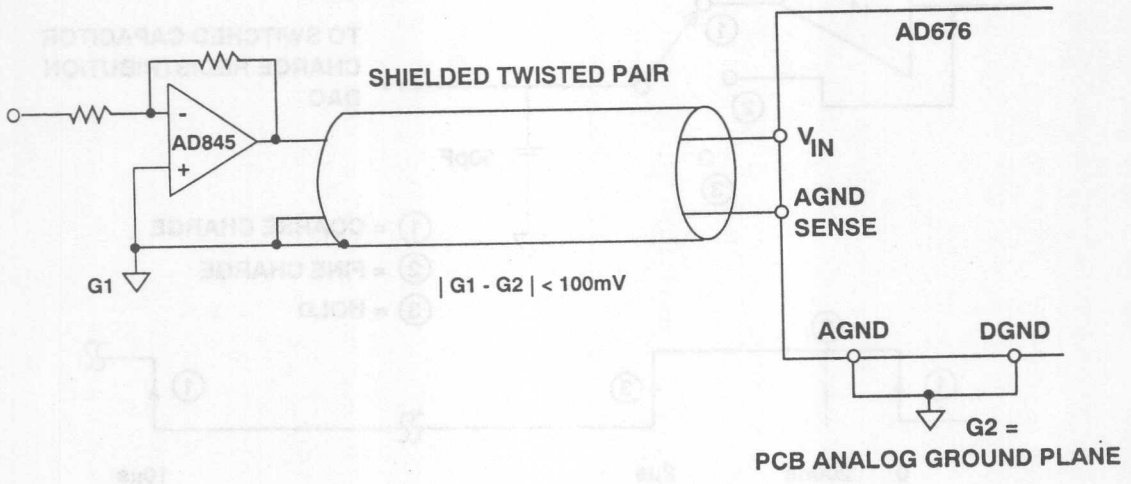


Figure 7.76

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AD676 16-BIT, 100kSPS SAMPLING ADC S/N + D AND EFFECTIVE BIT PERFORMANCE

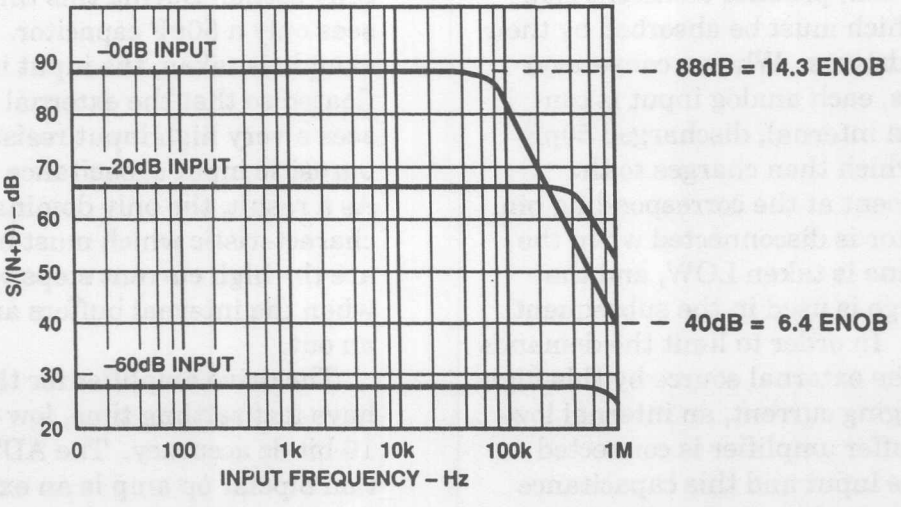


Figure 7.77

AD676 EQUIVALENT INPUT CIRCUIT

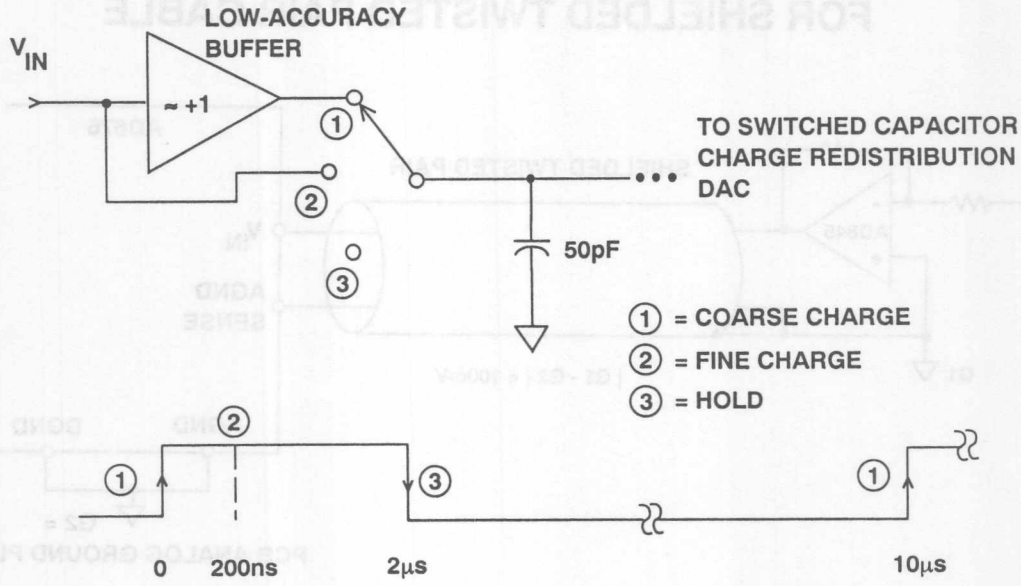


Figure 7.78

A simplified schematic of the input circuit of the AD676 is shown in Figure 7.78. All of the inputs (V_{in}, V_{ref}, and AGND SENSE) produce transient load currents which must be absorbed by their respective drivers. When a conversion cycle begins, each analog input is connected to an internal, discharged 50pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when the SAMPLE line is taken LOW, and the stored charge is used in the subsequent conversion. In order to limit the demands placed on the external source by this high initial charging current, an internal low-accuracy buffer amplifier is connected between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20kΩ | | 10pF and ±40mA bias current. Next, the input is switched directly to the now precharged capacitor and allowed to fully settle. During this time, the input sees only a 50pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of only 2pF. As a result, the only dominant input characteristic which must be considered is are the high current steps which occur when the internal buffers are switched in an out.

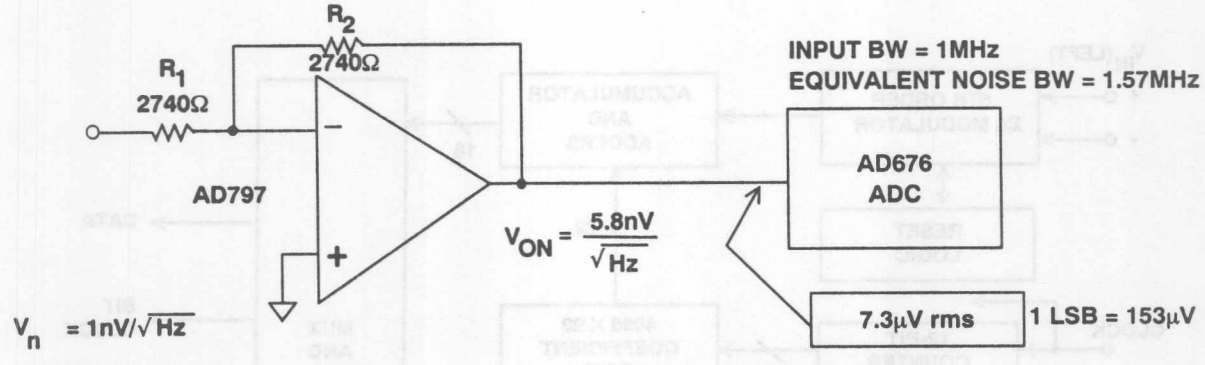
The drive amplifier for the AD676 must have fast settling time, low distortion and 16-bit dc accuracy. The AD797 low distortion bipolar op amp is an excellent choice for this application. Key specifications are summarized in Figure 7.79.

AD797 PRECISION LOW DISTORTION BIPOLAR OP AMP KEY SPECIFICATIONS

- 0.1mV Input Offset Voltage
- 0.2μV/°C Offset Voltage Drift
- 100nA Input Offset Current
- 1,000,000 dc Open Loop Gain
- 100MHz Gain Bandwidth Product
- 110dB THD @ 20kHz, 3Vrms into 600Ω
- 0.9nV/$\sqrt{Hz}$, 2pA/$\sqrt{Hz}$ Input Noise at 1kHz

Figure 7.79

AD797 DRIVING AD676 16 BIT, 100kSPS ADC



$$V_{ON} = \sqrt{BW}\sqrt{V_n^2\left[1+\frac{R_2}{R_1}\right]^2 I_{n-}^2 R_2^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{(1\times10^{-9})^2(2)^2 + (2\times10^{-12})^2(2740)^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{4\times10^{-18} + 30\times10^{-18}}$$

$$V_{ON} = \sqrt{BW}\,(5.8nV/\sqrt{Hz}) = \sqrt{1.57\times10^6}(5.8nV/\sqrt{Hz}) = 7.3\mu V\ rms$$

Figure 7.80

Figure 7.80 shows the calculations for the total output noise of the AD797 over the 1MHz input bandwidth of the AD676. The total noise is computed to be only 7μV rms compared to the theoretical 16-bit quantization noise (10V fullscale range) of 44μV rms.

For less demanding applications, the AD845 may be used as a drive amplifier for the AD676 yielding a total output noise of 63μV rms.

DRIVING SIGMA-DELTA AUDIO ADCs (AD1879)

The AD1879 is a state-of-the-art dual 18 bit sigma-delta ADC designed to meet the stringent requirements of professional digital audio. A block diagram of the device is shown in Figure 7.81, and performance specifications are summarized in Figure 7.82. The input sigma-delta modulator is a fifth-order differential switched capacitor design which performs the quantization noise shaping function. The oversampling ratio is 64x, which places the oversampling frequency at 3.072MHz for the standard audio sampling rate of 48kSPS. Because of the high oversampling ratio, a single-pole analog antialiasing filter is sufficient at the input of the ADC.

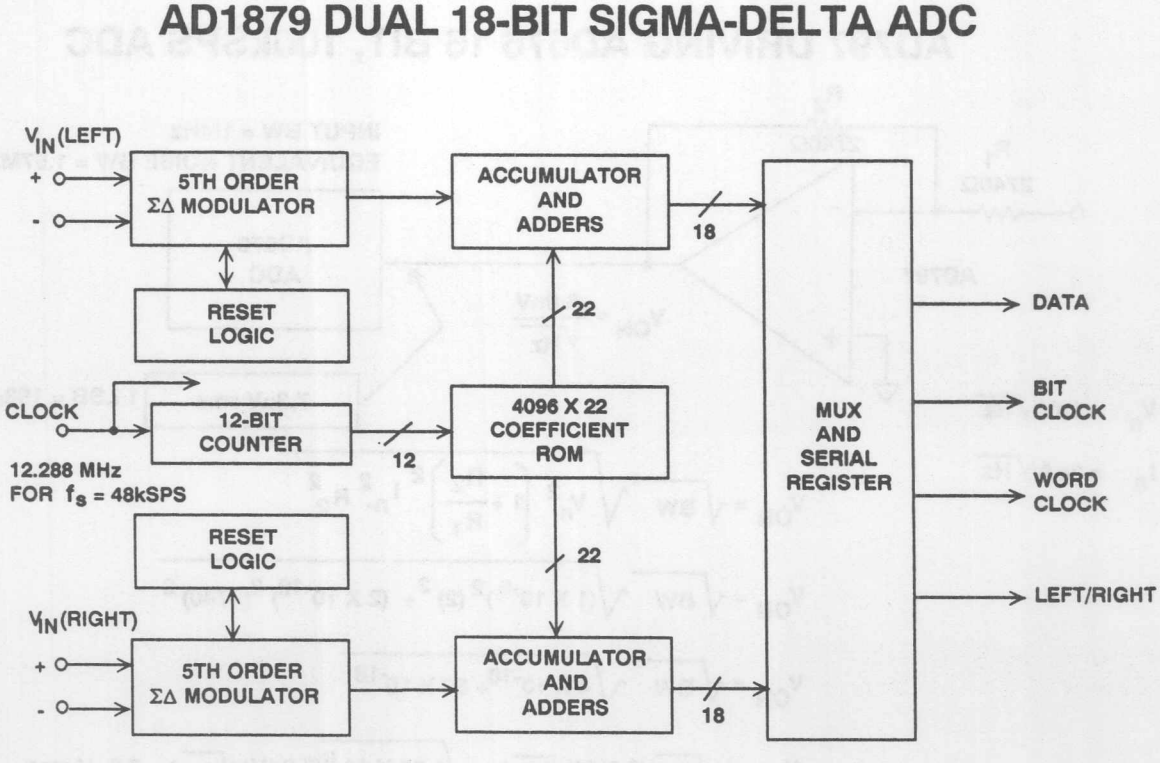


Figure 7.81

AD1879 18 BIT SIGMA-DELTA ADC KEY SPECIFICATIONS

- Two 18 Bit Channels for Stereo Digital Audio
- Interchannel Crosstalk: -110dB @ 1kHz
- SNR: 103dB
- THD: 98dB
- Oversampling Ratio: 64x
- Output Word Rate: 55kHz Maximum
- Linear Phase Digital Filter: 4095 Taps, 0.0004dB Passband Ripple, 115dB Stopband Attenuation
- Power: 600mW
- Package: 28 Pin, 600-mil Plastic

Figure 7.82

A switched capacitor input circuit presents a special set of problems for the drive amplifier because of signal-dependent transient input currents. In order to understand the phenomenon better, Figure 7.83 shows the basic circuit for a single-ended switched capacitor integrator. The capacitor is switched at the oversampling rate, f_S, and acts as a resistor having a resistance equal to $1/Cf_S$.

The integrator time constant is therefore determined by capacitance *ratios* which can be accurately controlled in a CMOS process. The switched capacitor is implemented in CMOS using the T-switch circuit shown in Figure 7.84. Because the input signal to the switch modulates the FET bias voltages, the charge injected into the drive amplifier is signal dependent.

SINGLE-ENDED SWITCHED CAPACITOR INTEGRATOR

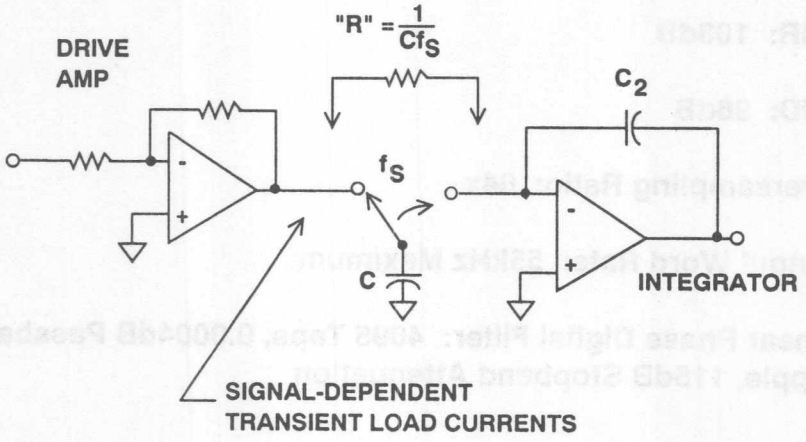
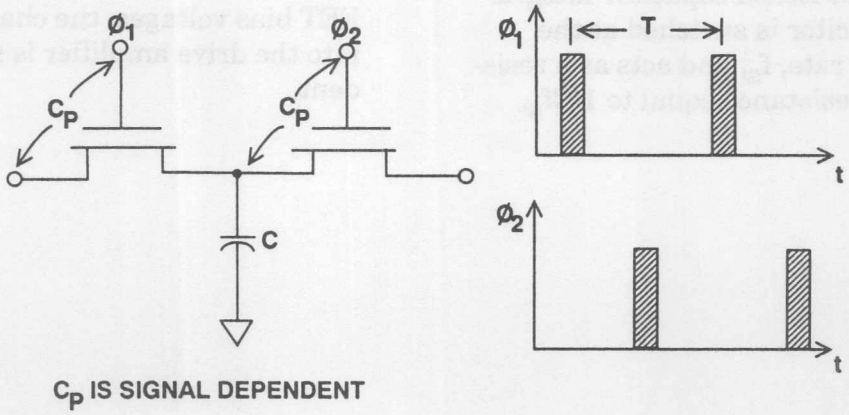


Figure 7.83

CMOS IMPLEMENTATION OF SWITCHED CAPACITOR



C_P IS SIGNAL DEPENDENT

Figure 7.84

DIFFERENTIAL DRIVER (ONE CHANNEL) FOR AD1879 SIGMA-DELTA AUDIO ADC

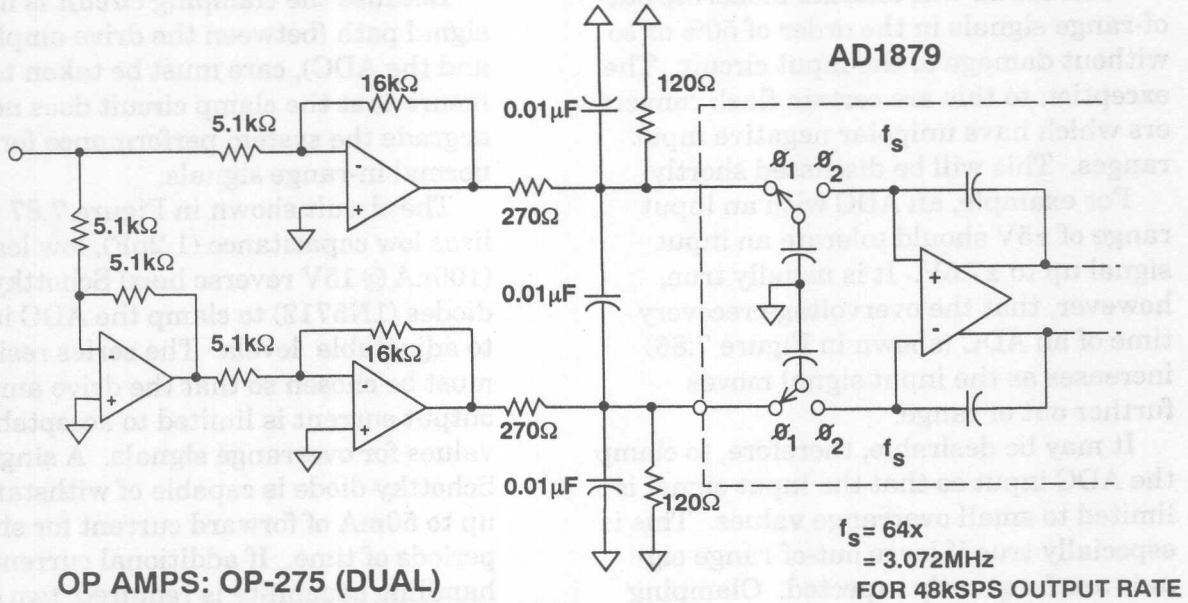


Figure 7.85

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The sigma-delta modulator in the AD1879 is fully differential and has the equivalent input circuit shown in Figure 7.85 (only one input channel shown). For optimum common mode rejection of transient load currents, the input should be driven differentially. The differentially connected 0.01µF capacitor supplies most of the differential-mode transient currents, while the 0.01µF capacitors connected to ground absorb spike currents which are common mode. The 270Ω series resistors isolate the remaining transient current from the drive amplifiers as well as isolate the capacitive loads from the op amp outputs. These resistors must be small, however, in order to avoid distortion because of the signal-dependent transients caused by charge injection. The OP-275 (dual) op amp is recommended as precision low-distortion drive amplifier for demanding professional audio applications.

ADC INPUT CLAMPING AND PROTECTION CIRCUITS

Most ADCs will tolerate moderate out-of-range signals in the order of 50% or so without damage to the input circuit. The exception to this are certain flash converters which have unipolar negative input ranges. This will be discussed shortly.

For example, an ADC with an input range of ±5V should tolerate an input signal up to ±7.5V. It is usually true, however, that the overvoltage recovery time of an ADC (shown in Figure 7.86) increases as the input signal moves further out of range.

It may be desirable, therefore, to clamp the ADC input so that the input signal is limited to small overrange values. This is especially true if large out-of-range signals are frequently expected. Clamping therefore not only protects the internal ADC input circuits from damage, but also reduces the overvoltage recovery time.

Because the clamping circuit is in the signal path (between the drive amplifier and the ADC), care must be taken to insure that the clamp circuit does not degrade the system performance for normal in-range signals.

The circuit shown in Figure 7.87 utilizes low capacitance (1.2pF), low leakage (100nA @ 15V reverse bias) Schottky diodes (1N5712) to clamp the ADC input to adjustable levels. The series resistor must be chosen so that the drive amplifier output current is limited to acceptable values for overrange signals. A single Schottky diode is capable of withstanding up to 50mA of forward current for short periods of time. If additional current-handling capability is required, two diodes may be paralleled at the expense of additional capacitance and reverse leakage current.

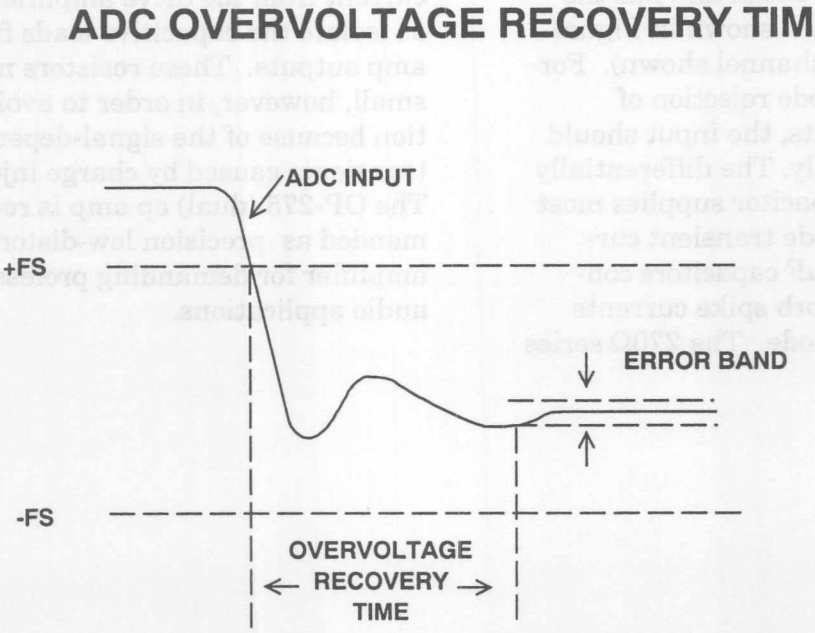


Figure 7.86

ADJUSTABLE POSITIVE AND NEGATIVE CLAMP CIRCUIT

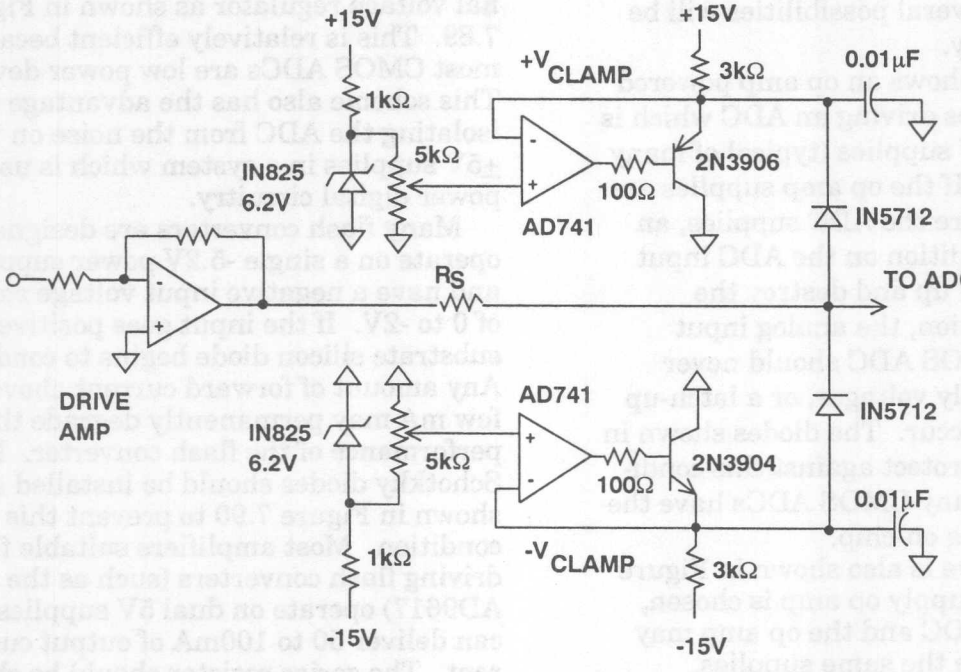


Figure 7.87

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PROTECTION AGAINST LATCH-UP AND DAMAGE DUE TO SUPPLY SEQUENCING

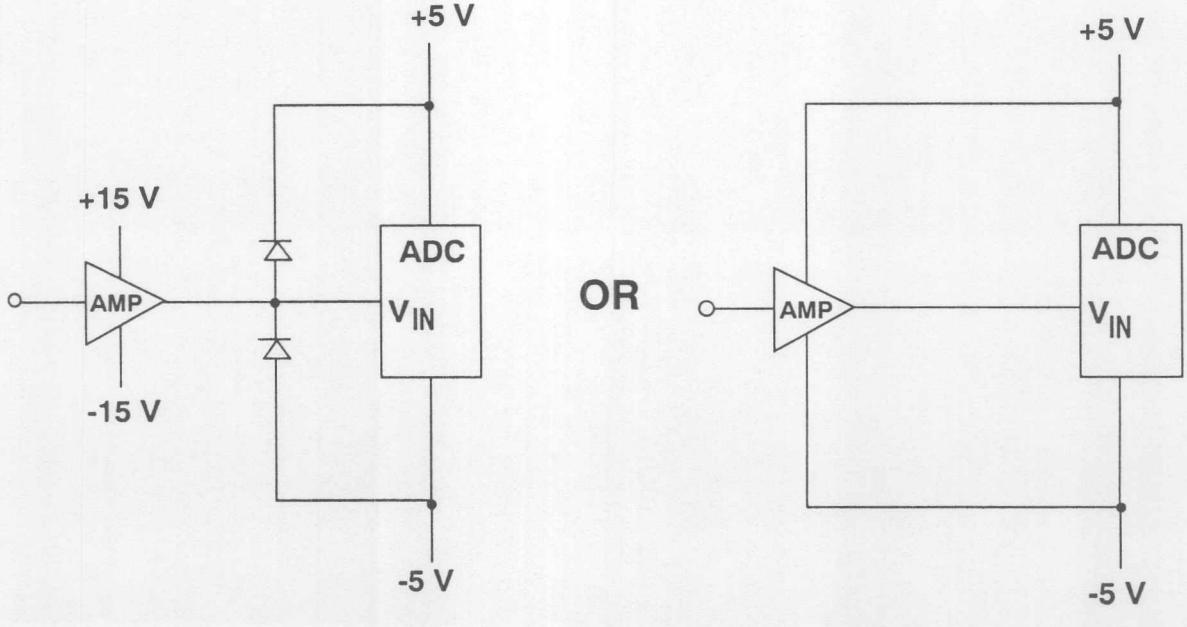


Figure 7.88

Other conditions of temporary overvoltage may occur because of power supply sequencing. Several possibilities will be discussed briefly.

Figure 7.88 shows an op amp powered by ±15V supplies driving an ADC which is powered by ±5V supplies (typical of many CMOS ADCs). If the op amp supplies are brought up before the ADC supplies, an overvoltage condition on the ADC input may cause latch up and destroy the device. In addition, the analog input voltage to a CMOS ADC should never exceed the supply voltages, or a latch-up condition may occur. The diodes shown in the figure will protect against this condition. In fact, many CMOS ADCs have the protection diodes on-chip.

An alternative is also shown in Figure 7.88. If a ±5V supply op amp is chosen, then both the ADC and the op amp may be powered from the same supplies, thereby eliminating the potential latch-up problem. It should be noted that many op amps have specifications for both ±15V and ±5V supply operation. If a ±15V op amp must be used, the ±5V for the CMOS ADC may be derived from a three-terminal voltage regulator as shown in Figure 7.89. This is relatively efficient because most CMOS ADCs are low power devices. This scheme also has the advantage of isolating the ADC from the noise on the ±5V supplies in a system which is used to power digital circuitry.

Many flash converters are designed to operate on a single -5.2V power supply and have a negative input voltage range of 0 to -2V. If the input goes positive, the substrate silicon diode begins to conduct. Any amount of forward current above a few mA may permanently degrade the performance of the flash converter. Input Schotkky diodes should be installed as shown in Figure 7.90 to prevent this condition. Most amplifiers suitable for driving flash converters (such as the AD9617) operate on dual 5V supplies and can deliver 50 to 100mA of output current. The series resistor should be chosen to limit this current to an acceptable level. Two diodes should be paralleled if more than 50mA current is expected from the drive amplifier.

USING 3-TERMINAL REGULATORS AS ADC SUPPLIES

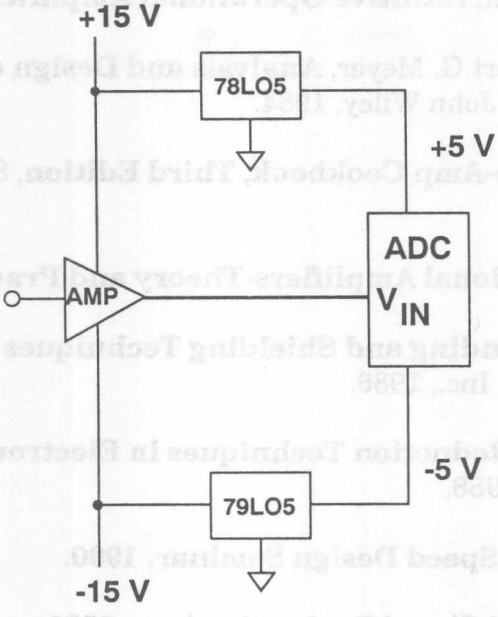


Figure 7.89

PROTECTING FLASH CONVERTER INPUTS WITH SCHOTTKY DIODES

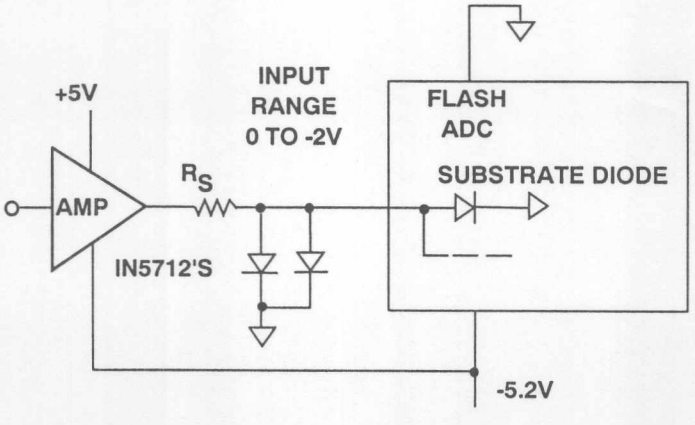


Figure 7.90

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SECTION VIII
VIDEO AND OTHER HIGH SPEED OP AMP APPLICATIONS

- Introduction to Broadcast Video
- Video Applications:
  Video Cable Driving, A Composite Video Sync Tip DC Restorer, A Video Sync Stripper Circuit, A High Performance Video ADC Differential Input Buffer
- Applying Ultra High Speed Op Amps:
  A Low Distortion Drive Circuit for Precision Wide Dynamic Range ADCs, Ultra High Speed Buffers, High Speed Differential Line Drivers and Receivers, A High Speed Three Op Amp Instrumentation Amplifier

SECTION VIII

VIDEO AND OTHER HIGH SPEED OP AMP APPLICATIONS

WALT KESTER, WALT JUNG, DAVE WHITNEY, CHRIS HYDE

INTRODUCTION TO BROADCAST VIDEO

WALT KESTER

Before discussing a few professional video applications, we will review some basics regarding the video signal. The standard video format is the specification of how the video signal looks from an electrical point of view. Light strikes the surface of an image sensing device within the camera and produces a voltage level corresponding to the amount of light hitting a particular spatial region of the surface. This information is then placed into the standard format and sequenced out of the camera. Along with the actual light and color information, synchronization pulses are added to allow the receiving device - a television monitor, for instance - to identify where the sequence is in the frame data.

A standard video format image is read out on a line-by-line basis from left to right, top to bottom. A technique called *interlacing* refers to the reading of all even numbered lines, top to bottom, followed by all odd lines as shown in Figure 8.1.

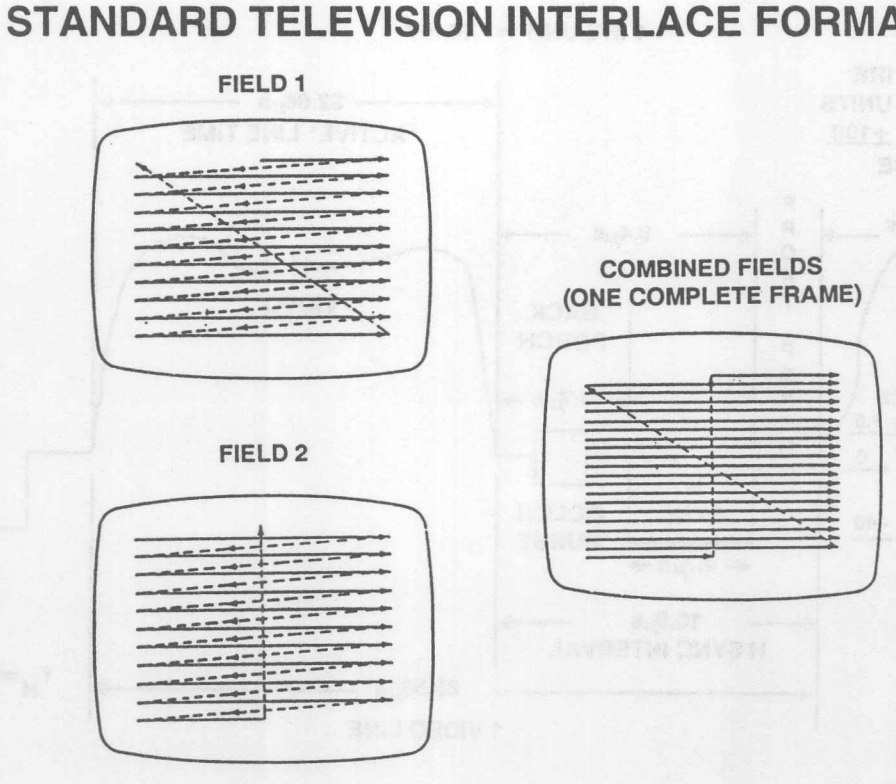


Figure 8.1

The television picture *frame* is thus divided into even and odd *fields*. Interlacing is used to produce an apparent update of the entire frame in half the time that a full update actually occurs. This results in a television image with less apparent flicker. Typical broadcast television frame update rates are 30 and 25 Hz, depending upon the line frequency.

The original black and white, or *monochrome*, television specification is the EIA RS-170 specification which prescribes all timing and voltage level requirements for standard commercial broadcast video signals. The standard specification for color signals, NTSC, modifies RS-170 to work with color signals by adding color information to the signal which otherwise contains only brightness information.

A video signal comprises a series of analog television lines. Each line is separated from the next by a synchronization pulse called the *horizontal sync*. The fields of the picture are separated by a longer synchronization pulse called the *vertical sync*. In the case of a monitor receiving the signal, its electron beam scans the face of the display tube with the brightness of the beam controlled by the amplitude of the video signal. Whenever a horizontal sync pulse is detected, the beam is reset to the left side of the screen and moved down to the next line position. A vertical sync pulse, indicated by a horizontal sync pulse of longer duration, resets the beam to the top left point of the screen to a line centered between the first two lines of the previous scan. This allows the current field to be displayed between the previous one. A single line for the NTSC color video signal is shown in Figure 8.2, and the field timing diagram in Figure 8.3.

NTSC COLOR VIDEO LINE

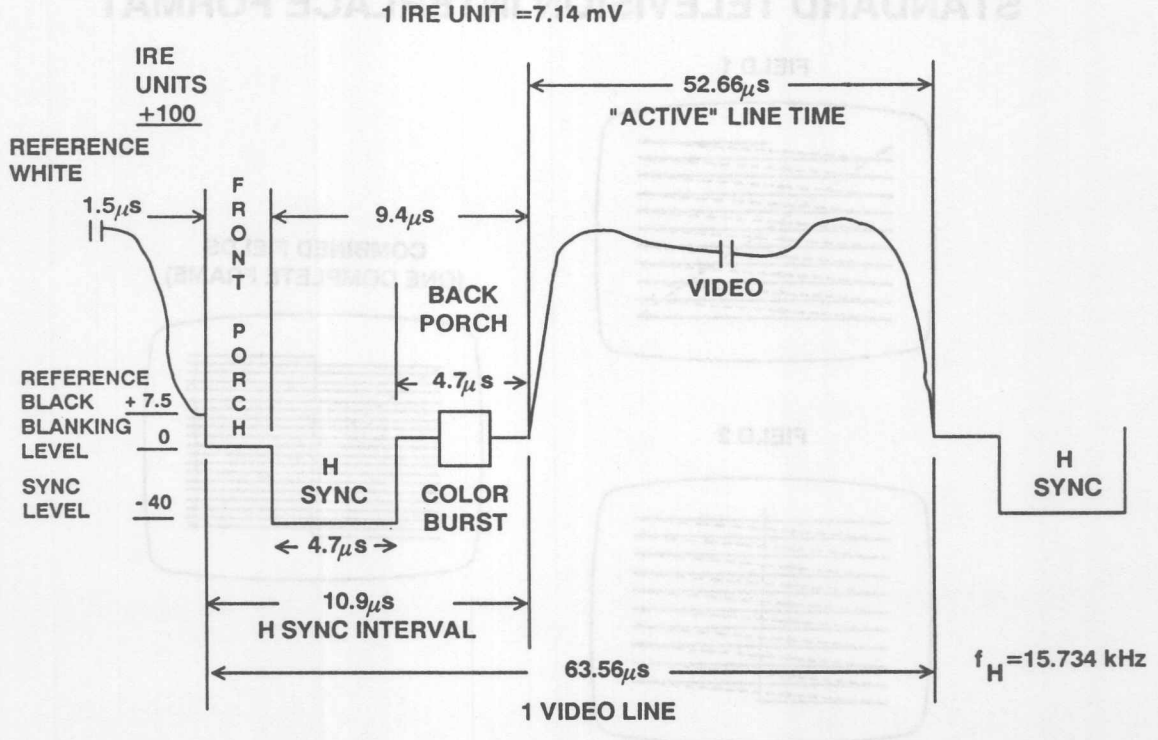


Figure 8.2

NTSC FIELD TIMING DIAGRAM

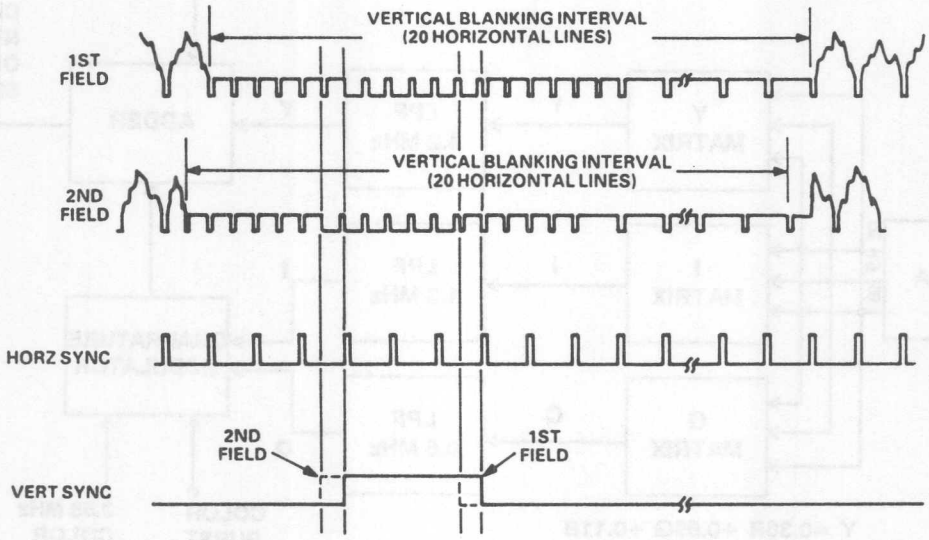


Figure 8.3

A simplified block diagram of the NTSC color processing system is shown in Figure 8.4. The three color signals (RGB: red, green, and blue) from the color camera are combined in a *matrix* unit to produce what is called the *luminance* signal (Y) and two color difference signals (I and Q). These *components* are further combined to produce what is called the *composite* color signal.

In the NTSC system (used in the U.S. and Japan), the color subcarrier frequency is 3.58MHz. The PAL system (used in the U.K. and Germany) and SECAM system (used in France), use a 4.43MHz color subcarrier. Comparisons between the NTSC system and the PAL system are given in Figure 8.5

GENERATING THE COMPOSITE NTSC COLOR SIGNAL

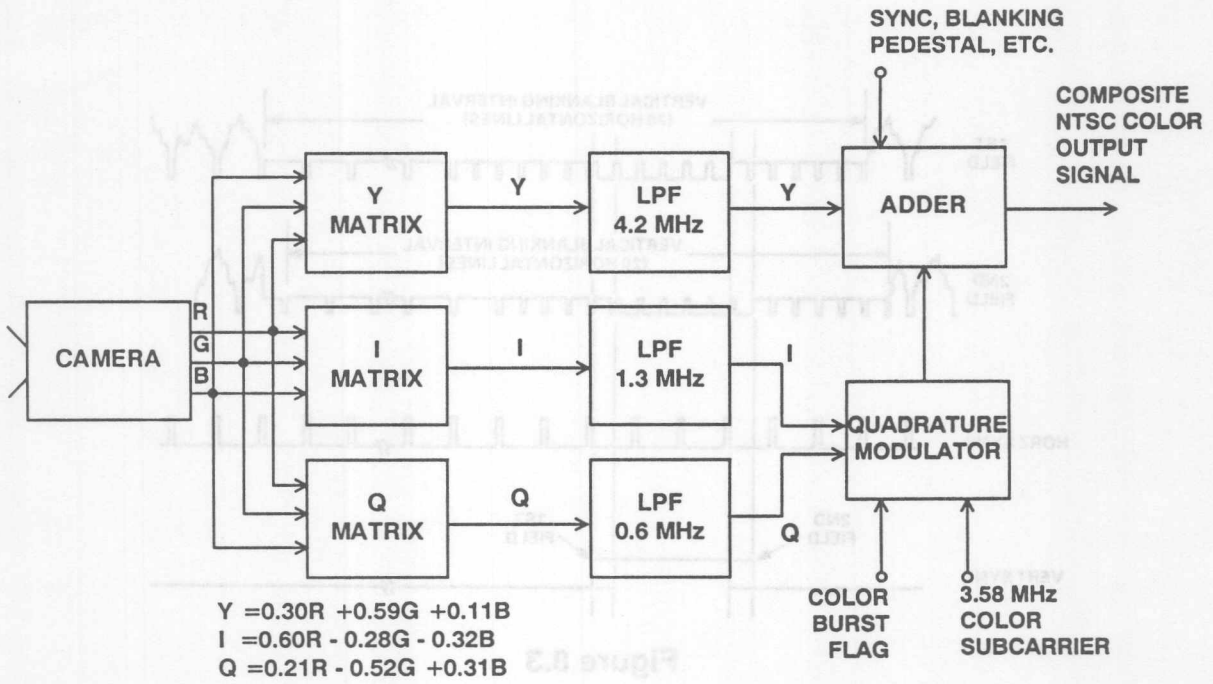


Figure 8.4

NTSC AND PAL SIGNAL CHARACTERISTICS

	NTSC	PAL
Horizontal Lines	525	625
Color Subcarrier Frequency	3.58MHz	4.43MHz
Frame Frequency	30Hz	25Hz
Field Frequency	60Hz	50Hz
Horizontal Sync Frequency	15.734kHz	15.625kHz

Figure 8.5

The color (or *chrominance*) information in the composite video signal is contained in the amplitude and phase of the subcarrier. The intensity of the color is determined by the amplitude of the subcarrier signal, and the color is determined by the phase of the subcarrier signal with respect to the color burst.

The chrominance signal modulates the luminance signal which determines the relative blackness or whiteness of the color. Therefore, in order to preserve color fidelity, it is important that the amplitude and phase of a constant-amplitude and phase color subcarrier remain constant across the entire range from black to white. Any variation of the *amplitude* of the color subcarrier from black to white levels is called *differential gain* (expressed in %), and any variation in phase with respect to the color subcarrier is called *differential phase* (expressed in degrees). Although several percent differential gain and several degrees differential phase is acceptable for home viewing purposes, individual components in the signal path (such as amplifiers, switches, etc.) must meet much tighter specifications. This is because the signal must pass through many circuits from the camera to the home. Individual professional video systems therefore have stringent requirements for differential gain and phase, usually limiting changes to less than 0.1% and 0.1°. These system specifications mandate even more stringent standards for individual components, with the differential gain and differential phase requirements for op amps approaching 0.01% and 0.01°.

Figure 8.6 shows a high resolution setup that uses a HP3314A arbitrary waveform generator and a HP8753A network analyzer to measure differential gain and phase to better than 0.01% and 0.01° accuracy. The arbitrary waveform generator generates a staircase that simulates the luminance (picture level) portion of the video waveform. The network analyzer supplies the color subcarrier waveform, in this case a 4.43MHz color subcarrier. The network analyzer also measures the differences in the color subcarrier's phase and gain by comparing the output of the DUT and the reference signal returned by the HP11850 signal splitter. Note that the 4.43MHz color subcarrier and the staircase signal are summed at the input to the op amp. This summing action superimposes the color subcarrier on the staircase, thus generating the standard video test waveform. The differential phase and gain is defined as the maximum difference in the phase or gain between any of the steps in the staircase waveform. Actual measurements taken on an op amp are shown in Figure 8.7.

The op amp under test is shown connected as a gain-of-two amplifier driving a 75Ω reverse-terminated line. The 75Ω series termination resistor both absorbs reflections from the line and isolates the op amp from the capacitive load presented by the line. The 75Ω termination resistor and the 75Ω load form a voltage divider, so the net gain from the input to the DUT circuit to the load is unity.

PRECISION MEASUREMENT OF DIFFERENTIAL GAIN AND PHASE

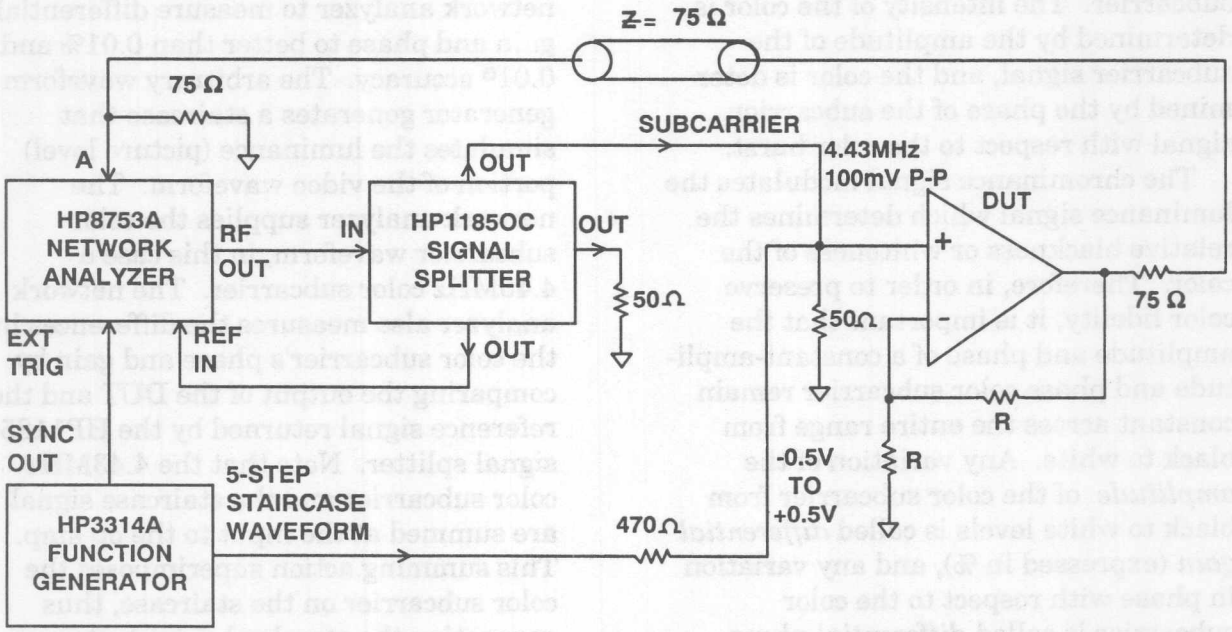
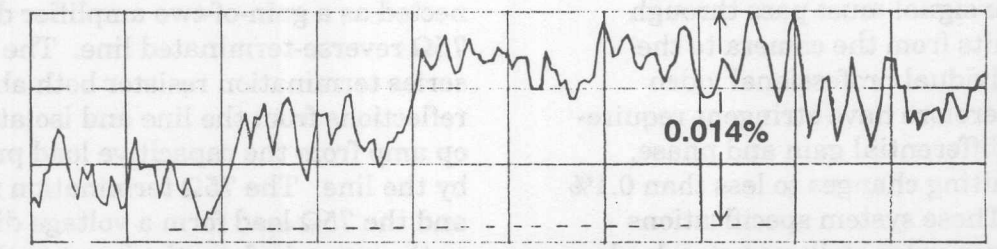


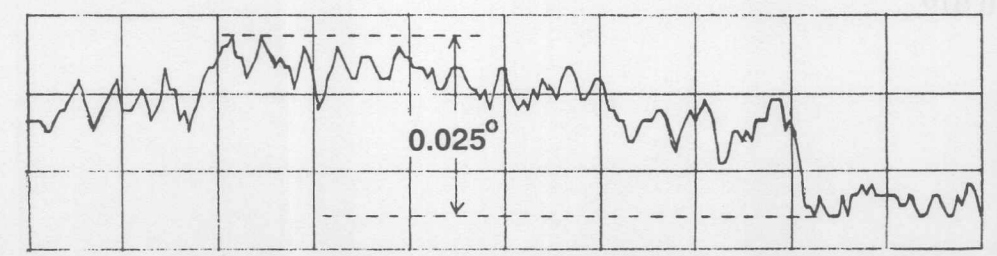
Figure 8.6

DIFFERENTIAL GAIN AND PHASE MEASURED WITH PRECISION TEST SET



DIFFERENTIAL GAIN

-1V R_L = 100 Ω, MODULATION: 200mV, 4.43 MHz +1V



DIFFERENTIAL PHASE

Figure 8.7

VIDEO CABLE DRIVING

WALT JUNG, DAVE WHITNEY

The recently introduced Analog Devices AD811 is the most up- to-date as well as the highest performer in a growing line of transimpedance amplifiers. Like such forerunners as the AD844, the AD846, the OP-160/OP-260, and the AD9617/AD9618, the AD811 is aimed primarily at high speed AC applications. While the part's mainstay uses are intended to be broadcast, studio and HDTV video signal processing, it should also find diverse other applications.

Amplifier categories such as those requiring wide band, large signal, low distortion operation are candidates. Some examples are signal generators and other lab instruments, radar IF and ultrasound amplifiers, medical instrumentation, gamma detectors, ADC & DAC input/ output buffers, and other demanding applications.

Built on AD's advanced high speed complementary bipolar (CB) process, the AD811 achieves new highs for performance vis-a- vis many industry predecessors. Highlights include a bandwidth of over 100 MHz and a SR of 2500 V/μs, combined with an output current capability of more than 100mA with very low distortion. In addition the AD811 settles quickly and cleanly; for a 2V step the time is 25ns to 0.1% , while for a 10V step it settles in just 65ns to 0.01%. The AD811 comes in two temperature grades with similar electrical specs. The AD811A is for -40 to +85°C operation, while the AD811S is for -55 to +125°C use. It is supplied a variety of packages, these include 8 pin plastic and cerdip, 16 and 20 pin SOIC, and 20 pin LCC formats. Key specifications for the AD811 are summarized in Figure 8.8.

8

AD811 HIGH PERFORMANCE VIDEO OP AMP KEY SPECIFICATIONS

- **120MHz Bandwidth (3db, G = +2)**
- **35MHz Bandwidth (0.1dB, G = +2)**
- **Video Specs: 0.01% Differential Gain, 0.01° Differential Phase**
- **Low Distortion: THD = -74dB @ 10MHz**
- **±100mA Output Current**
- **0.5mV Input Offset, 5μV/°C Drift**

Figure 8.8

Most importantly however, the device is specified for premium levels of performance in demanding video applications. The AD811's differential gain and phase is rated as 0.01% and 0.01° respectively (G=2 @ 3.58 MHz, R_L=150Ω). Further, it is also specified for a tight gain accuracy of 0.1dB at 35MHz... a performance parameter important for HDTV systems. In general the above features have optimum accessibility to the designer, since the AD811 is rated for operation from supplies of ±5V to ±15V. While there is some performance degradation with the lower supplies, the part is video characterized for various gains for these supply ranges. As a result, the user knows just what the tradeoffs will be (more on this below).

The basic circuit of the AD811 (not shown) is like many other similar transimpedance ICs. Nonetheless, the performance distinctions setting it apart come from attention to various design details within. With device trimming at the input stage, low offset voltage and bias current result. These are a Vos of 0.5mV and a bias current of 2μA; both low figures for this type of amplifier. In AC terms, an input stage slew enhancement circuit comes into play for large and fast non-inverting signals, allowing closer signal tracking and lower distortion. This removes a problem common in many other transimpedance amps when they operate as followers.

Transimpedance amplifiers as a rule aren't noted for high gain accuracy, for either DC or AC. Open loop gain in a transimpedance amplifier is maximum when the loaded transimpedance (R_t) is high, and the inverting node input resistance (R_{IN}) is low. In the AD811, the typical figures for these parameters are 1.5MΩ (unloaded) and 14Ω, respectively. The open loop gain is equal to R_t/R_{IN}, or 107,000. Even when loaded in 200Ω, the transimpedance only drops to 750,000Ω. The AD811's R_{IN} is 14Ω, and in general, the lower this parameter the better, as low R_{IN} values allow the amplifier to maintain more bandwidth as closed loop gain is raised.. a hallmark trait of the transimpedance topology.

A parallel array of high speed, large geometry complementary transistors is used in the output circuit of the AD811, with current limiting set at ±150mA. With the high gain linearity so provided by the effective output transistors, this allows loads of 100Ω to be driven to ±10V levels with low distortion. In addition, a special drive configuration optimizes gain flatness for various loads, and this stage's low open loop output resistance of 11Ω also contributes to load immunity. In addition to the NTSC video specs already cited, the 10MHz distortion of the AD811 is also low, at -74dBc, and the third order intercept is 43dBm. Harmonic distortion performance of the AD811 is shown in Figure 8.9.

For video designers, a more relevant aspect of the AD811 is that it is fully specified for typical "bread and butter" video uses, that is the circuit environment needed for a direct performance assessment. Figure 8.10 illustrates this point, showing a standard application of a gain-of-2 video buffer or line driver. This circuit replicates a standard NTSC video signal V_{IN}, with the input line terminated in 75Ω. The AD811 stage operates at a gain of 2, driving a pair of 75Ω output lines through 75Ω back terminations. V_{OUT1} and V_{OUT2} are thus individually isolated/buffered unity gain versions of V_{IN}. With the overall terminated gain of unity, this circuit serves well as a low distortion buffer, or a video distribution amp.

AD811 HARMONIC DISTORTION PERFORMANCE
G = +2, Rload = 100Ω, Vout = 2V p-p

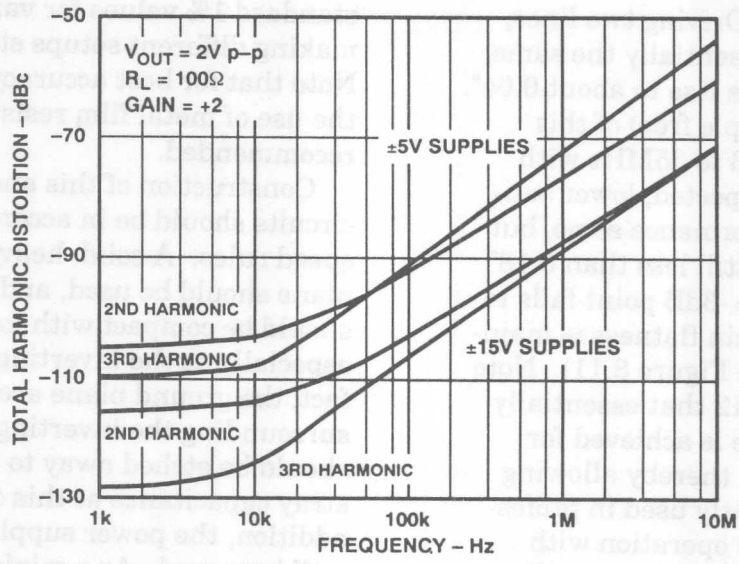


Figure 8.9

AD811 VIDEO LINE DRIVER

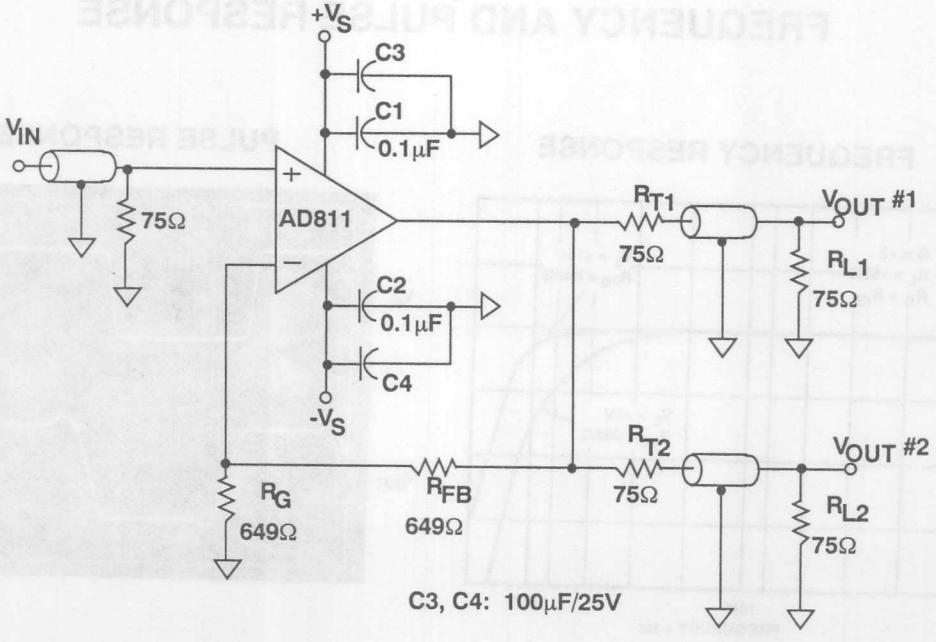


Figure 8.10

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Exactly as shown and operated from ±15V supplies, the circuit has a -3dB bandwidth of 120 MHz, and differential gain/phase of 0.01%/0.01° with one line driven (R_L = 150Ω). Driving two lines, the gain errors are essentially the same, while the phase errors rise to about 0.04°. The gain flatness (ripple free) of this circuit is within 0.1dB to 35MHz with ±15V supplies. As expected, lower supplies do degrade performance some, but differential phase is still less than 0.18° with ±5V power. The -3dB point falls to 80MHz, and 0.1dB gain flatness is maintained to 25MHz (see Figure 8.11). Note however in Figure 8.12 that essentially full differential phase is achieved for supplies above ±10V, thereby allowing ±12V supply (frequently used in professional video systems) operation with minimal degradation in video specifications.

Figure 8.13 summarizes performance for this basic circuit for a variety of other gain options (up to ±10), for both power supplies. The resistor values chosen are standard 1% values for various gains, making different setups straightforward. Note that for best accuracy and stability, the use of metal film resistor types are recommended.

Construction of this and other AD811 circuits should be in accordance with high speed rules. A solid, heavy copper ground plane should be used, and circuit layout should be compact with low capacitance, especially at the inverting input pin. In fact, the ground plane area immediately surrounding the inverting input pin should be etched away to insure minimum stray capacitance at this critical node. In addition, the power supplies should be well bypassed. As a minimum, local low inductance/low ESR RF bypass caps

AD811 VIDEO LINE DRIVER FREQUENCY AND PULSE RESPONSE

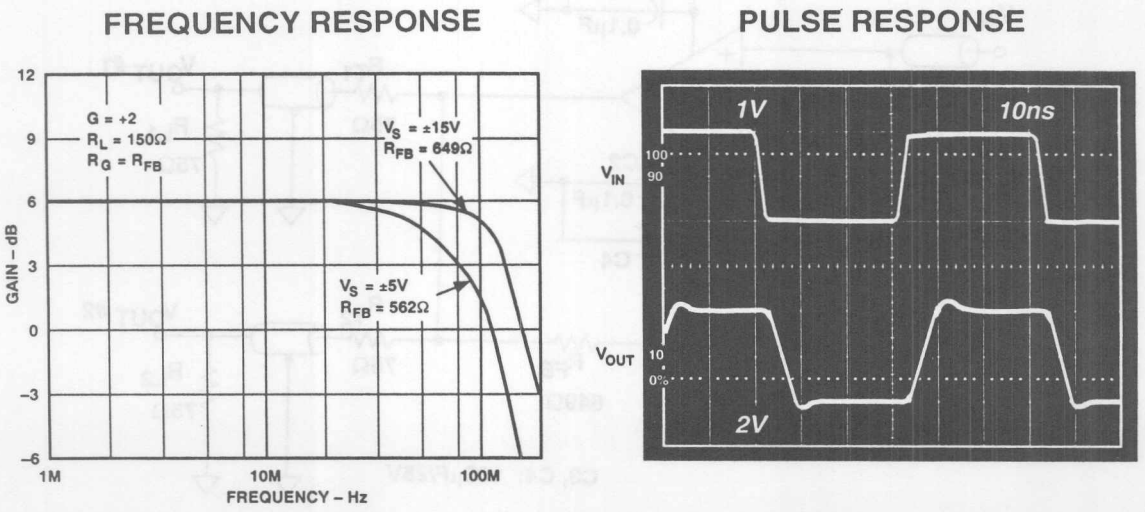


Figure 8.11

AD811 VIDEO LINE DRIVER DIFFERENTIAL GAIN AND PHASE PERFORMANCE

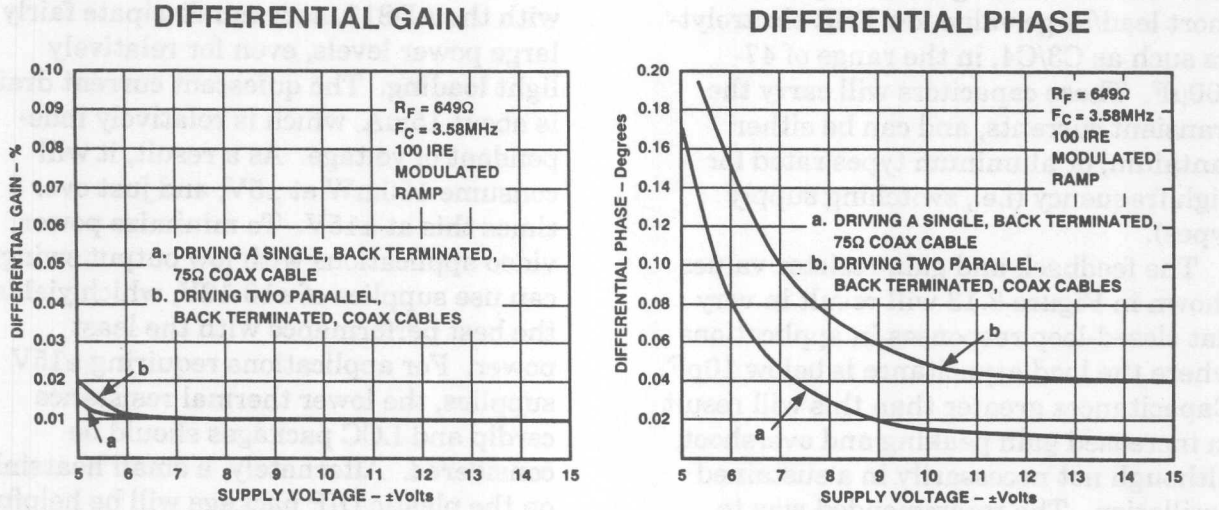


Figure 8.12

AD811 RECOMMENDED RESISTOR VALUES AND RESULTING BANDWIDTHS

V_S = ±15V Closed-Loop Gain	R_{fb} (Ω)	R_g (Ω)	-3dB BW (MHz)
+1	750		140
+2	649	649	120
+10	511	56.2	100
-1	590	590	115
-10	511	51.1	95
V_S = ±5V Closed-Loop Gain	R_{fb} (Ω)	R_g (Ω)	-3dB BW (MHz)
+1	619		80
+2	562	562	80
+10	442	48.7	65
-1	562	562	75
-10	442	44.2	65

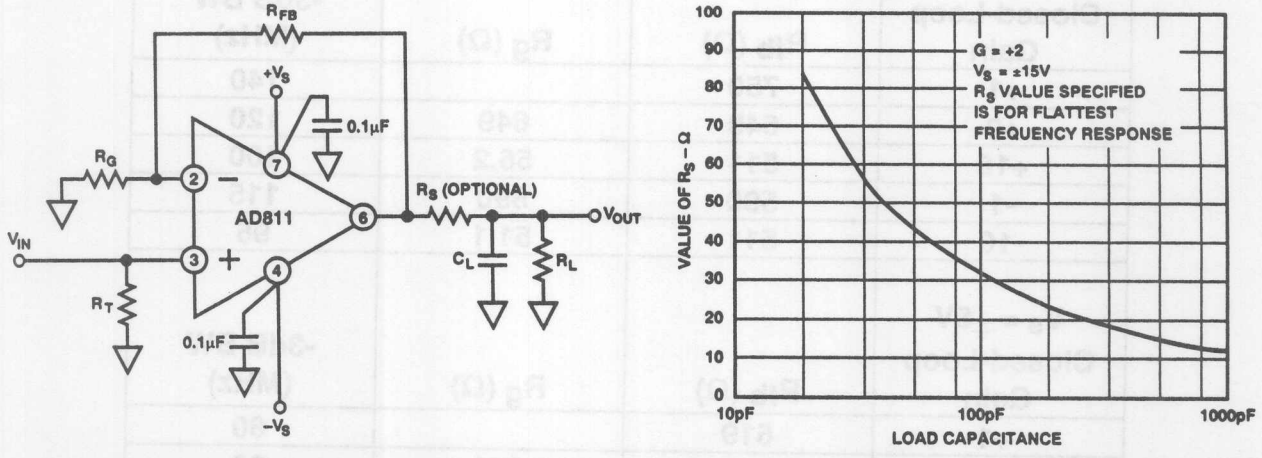
Figure 8.13

should used right at the device supply pins, shown as C1/C2. These are 0.1μF surface mount chips (or other low inductance type). When driving high peak current loads, these high frequency bypasses should be augmented by local, short lead/large value low ESR electrolytics such as C3/C4, in the range of 47-100μF. These capacitors will carry the transient currents, and can be either tantalum, or aluminum types rated for high frequency (i.e., switching supply types).

The feedback and gain resistor values shown in Figure 8.13 will result in very flat closed-loop responses in applications where the load capacitance is below 10pF. Capacitances greater than this will result in increased gain peaking and overshoot, although not necessarily in a sustained oscillation. The recommended way to stabilize the AD811 for load capacitances greater than 10pF is to add a small resistor in series with the output of the amplifier to isolate it from the capacitive load. The recommended resistor values for various values of capacitive loads are shown in Figure 8.14

Power management can be important with the AD811, as it can dissipate fairly large power levels, even for relatively light loading. The quiescent current drain is about 15mA, which is relatively independent of voltage. As a result, it will consume 150mW at ±5V, and just over 3 times this at ±15V. To minimize power, video applications with low output swings can use supplies of ±10-12V, which yields the best performance with the least power. For applications requiring ±15V supplies, the lower thermal resistance cerdip and LCC packages should be considered. Alternately, a small heatsink on the plastic DIP package will be helpful, such as the Aavid #5801.

DRIVING CAPACITIVE LOADS GREATER THAN 10pF WITH THE AD811



NOTE: R_L = 10kΩ

Figure 8.14

A COMPOSITE VIDEO SYNC TIP DC RESTORER

WALT JUNG, DAVE WHITNEY

A common video signal processing requirement is DC restoration, or clamping. When used with a composite NTSC video signal, sync tip clamping is commonly used. This fixes the most negative excursion of the signal to a fixed DC level, which is usually ground. With a constant input signal level, note that this operation also fixes the remainder of the signal with respect to ground. The circuit of Figure 8.15 is an example of a sync tip clamper, using 2 ICs and a pair of discrete transistors. With a standard NTSC composite video signal at the input, the circuit DC restores the signal to a ground reference, and makes the DC restored and buffered version available at the output, source terminated by 75Ω.

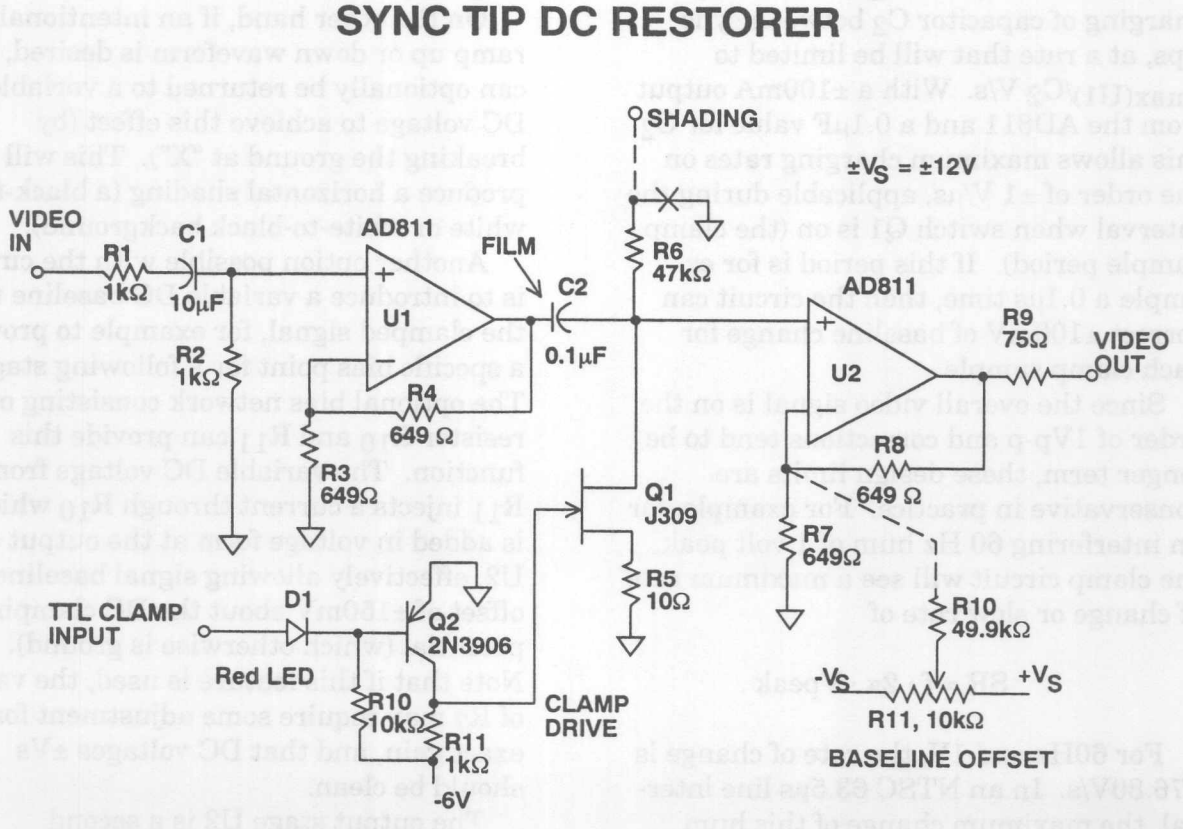


Figure 8.15

In operation, the U1 stage functions as an input line isolator and buffer. The signal at the input is divided by a factor of 2 by R_1 and R_2, and is AC coupled into U1. U1 is an AD811 configured as a wideband times 2 amplifier, by virtue of the R_4-R_3 ratio. With the values shown for R_4-R_3 and the use of ±10V (or more) DC supplies, the 0.1dB bandwidth of stages U1 (and U2) will be more than 30MHz.

The output of U1 drives Q1, a shunt JFET switch through a film coupling cap, C_2. The N channel JFET is a low capacitance, high transconductance unit, chosen for 50Ω or less of on-resistance. The low capacitance allows it to be easily driven from U1, minimizing potential distortion to the signal. The low on-resistance of Q1 and high output current of the AD811 driver stage allows very fast charging of capacitor C_2 between sync tips, at a rate that will be limited to $I_{max(U1)}/C_2$ V/s. With a ±100mA output from the AD811 and a 0.1μF value for C_2, this allows maximum charging rates on the order of ±1 V/μs, applicable during the interval when switch Q1 is on (the clamp sample period). If this period is for example a 0.1μs time, then the circuit can correct ±100mV of baseline change for each clamp sample.

Since the overall video signal is on the order of 1Vp-p and corrections tend to be longer term, these design limits are conservative in practice. For example, for an interfering 60 Hz hum of 1 volt peak, the clamp circuit will see a maximum rate of change or slew rate of

$$SR = f \cdot 2\pi \cdot Vpeak .$$

For 60Hz and 1V, the rate of change is 376.80V/s. In an NTSC 63.5μs line interval, the maximum change of this hum signal is 376.80·63.5e-6 = 0.024V, which is correctable.

The clamp sample period drive signal is derived elsewhere, and is presented to this circuit as a TTL signal at D1-Q2. This signal, , is an active low TTL logic signal, and is timed to occur during the video waveform negative sync tips. The low state signal drives both Q2 and Q1 on, effectively connecting C_2 to ground through Q1-R_5, and so provides the DC reference path to ground described above.

During the remaining time period of a video line time, the switch Q1 is off due to the -6V bias from R_{11}. The bias current of U2 is the main DC load on the C_2-R_6 voltage node during this time, which will tend to ramp ±, slowly charging C_2 with the bias current of U2. Since this current could be as high as 5μA, the baseline ramp error in 50μs time could be (5e-6/0.10e-6)*50e-6 volts, or 2.5mV. However, this is not likely to be a problem, as the typical AD811 bias current is lower, and the video signal is appreciably larger in amplitude.

On the other hand, if an intentional ramp up or down waveform is desired, R_6 can optionally be returned to a variable DC voltage to achieve this effect (by breaking the ground at "X"). This will produce a horizontal shading (a black-to-white or white-to-black background).

Another option possible with the circuit is to introduce a variable DC baseline to the clamped signal, for example to provide a specific bias point for a following stage. The optional bias network consisting of resistor R_{10} and R_{11} can provide this function. The variable DC voltage from R_{11} injects a current through R_{10} which is added in voltage form at the output of U2, effectively allowing signal baseline offset of ±150mV about the DC clamping potential (which otherwise is ground). Note that if this feature is used, the value of R_7 may require some adjustment for exact gain, and that DC voltages ±Vs should be clean.

The output stage U2 is a second wideband AD811, configured as a 75Ω line driver in this case. U2 presents the DC restored video signal to the output, with a level equal to the original input signal.

A VIDEO SYNC STRIPPER CIRCUIT

WALT JUNG, DAVE WHITNEY

Another common video signal processing requirement is the function of sync stripping. In a sync stripper, horizontal and vertical timing information is removed from the composite NTSC video signal and converted to logic levels for further processing. The circuit of Figure 8.16 is a self-contained sync stripper, using 1 IC and a pair of discrete transistors. It is driven from an NTSC composite video signal and delivers TTL compatible positive going sync at the output.

In this circuit the U1 stage performs three functions. First, components L_1-C_2 act as a low pass filter, removing the 3.58MHz chrominance components. U1, an AD811, also is an isolator with gain as well as a buffer to drive the following stage, which is a low input impedance sync tip clamp. The input signal is divided by a nominal factor of 2 by R_1 and R_2-R_3, and AC coupled to the input of U1. U1 is configured as a wideband times 6 amplifier, by the R_5-R_4 ratio. This yields an overall luminance signal gain of three times, from the input to C_3. With the gain values shown and ±5V (or more) DC supplies for U1, the stage can handle normal video signals without clipping at the output.

U1's output drives Q1, a PNP shunt clamp in an unusual configuration. In steady-state DC terms, Q1 is held in saturation by the bias current from R_7, where the emitter is close to ground. Since the AC signal driving Q1 through C_3 is a composite video signal with the sync tips the most negative limit, on a

SYNC STRIPPER GENERATES COMPOSITE SYNC

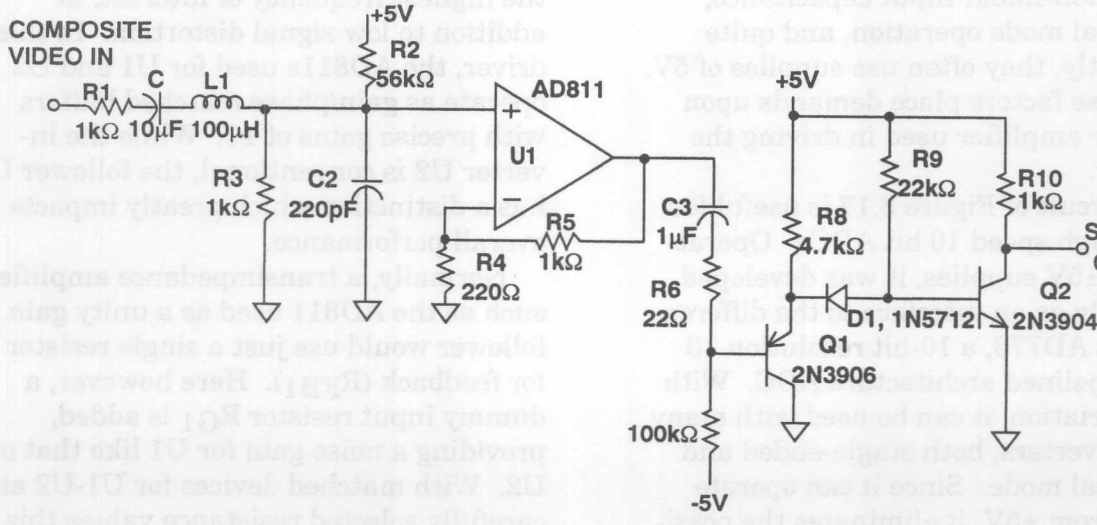


Figure 8.16

dynamic basis Q1 acts as a DC restorer. The negative going video waveform sync tips drive Q1 into hard saturation, and the more positive parts of the waveform bring it out of saturation, where it acts as a linear emitter follower. This action produces a DC restored composite video signal at the emitter of Q1, with the sync tips referred to ground.

The output of Q1 is coupled to the base of NPN switch Q2, through Schottky diode D1. The combination of this diode's forward drop and the V_{BE} of Q2 produce a switching threshold at the base of Q2 which, with consideration of the signal levels, causes Q2 to switch on/off cleanly at about the sync tip 50% amplitude point.

The output from Q2 consists of clean, noise-free sync timing information, positive going during sync tips. This signal is TTL compatible, by virtue of the +5V supply to Q2 as shown. Practical hints in getting the most from this circuit involve some attention to good decoupling of the U1 stage. The high instantaneous currents during the sync tips can generate power supply and/or ground noise. Local bypassing of U1 with large capacitors to the logic supply ground will help to control this, as will a compact layout and the use of a ground plane.

A HIGH PERFORMANCE VIDEO ADC DIFFERENTIAL INPUT BUFFER

WALT JUNG, DAVE WHITNEY

Closely related to video applications are analog-digital- converter (ADC) input buffers. This class of circuit is in some regards even more demanding in performance. The distortion levels are desirably in the -60 to -70dB range for signals around 1V full scale, and up to 10MHz or more in frequency. In addition, high speed ADCs are often difficult to drive in terms of non-linear input capacitance, differential mode operation, and quite importantly, they often use supplies of 5V. All of these factors place demands upon the buffer amplifier used in driving the converter.

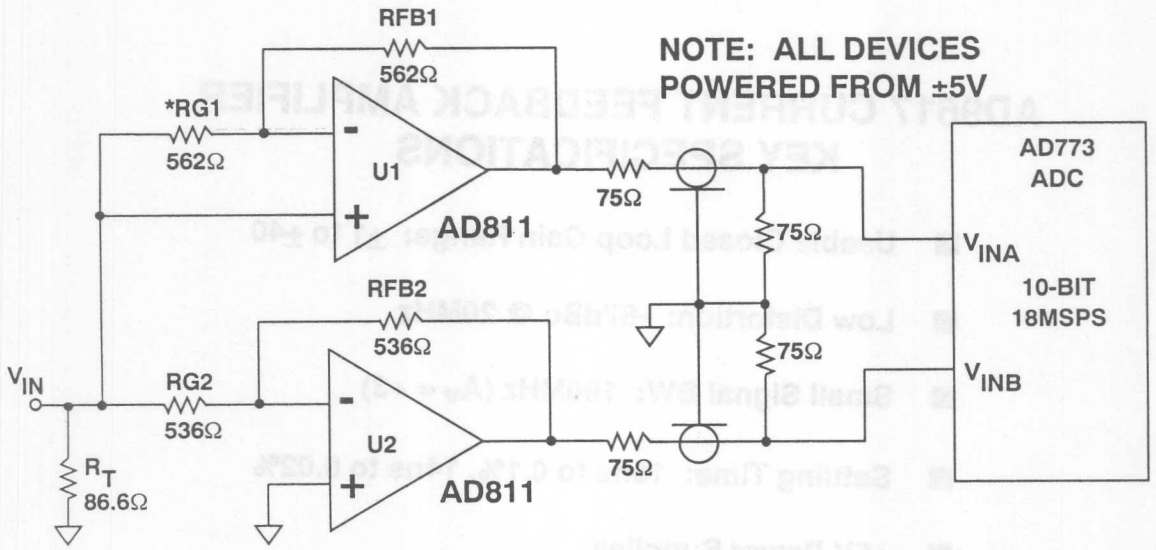
The circuit of Figure 8.17 is useful for driving high speed 10 bit ADCs. Operating from ±5V supplies, it was developed specifically as an interface to the differential input AD773, a 10-bit resolution 18 MSPS pipelined architecture ADC. With minor variation, it can be used with many other converters, both single-ended and differential mode. Since it can operate directly from ±5V, it eliminates the possibility of destructive ADC overdrive with higher supply voltage buffers.

The AD773 ADC operates best when driven differentially between inputs V_{INA} and V_{INB}, with full scale signals of ±500mV. The dual AD811 driver translates a ±500mV single ended signal across R_{Tin} to dual ±250mV signals at V_{INA} and V_{INB}.

In many differentially driven applications, the two output signals should maintain gain and phase flatness for high performance. This is desirable to above the highest frequency of interest, in addition to low signal distortion. In this driver, the AD811s used for U1 and U2 operate as gain/phase matched buffers with precise gains of ±1. While the inverter U2 is conventional, the follower U1 has a distinction which greatly impacts overall performance.

Normally, a transimpedance amplifier such as the AD811 used as a unity gain follower would use just a single resistor for feedback (R_{FB1}). Here however, a dummy input resistor R_{G1} is added, providing a noise gain for U1 like that of U2. With matched devices for U1-U2 and carefully selected resistance values this allows similar gain/phase characteristics, important for the accurate conversion of video and other high resolution signals.

OPTIMIZED AD811 DIFFERENTIAL ADC BUFFER



***RG1 MAKES NOISE GAIN OF U1=NOISE GAIN OF U2**

Figure 8.17

This gain/phase matching is quite effective, with results of 0.05dB and 0.5° between the two output signals at 20MHz, loaded as shown. These figures are 5-10 times better than they would be with the use of a conventional follower (i.e., without R_{G1}). Bandwidth of this driver is 80MHz at the -3dB point, and the 0.1dB bandwidth is 25MHz. Second harmonic distortion results at 8MHz with the AD773 using the buffer showed an improvement of about 15dB over more simple drive schemes.

While this example has illustrated driving an AD773 directly, it is worth noting that the line driving capability of the AD811 will allow this driver to be located remote from an ADC, if necessary.

8

APPLYING ULTRA-HIGH SPEED OP AMPS

WALT KESTER, CHRIS HYDE

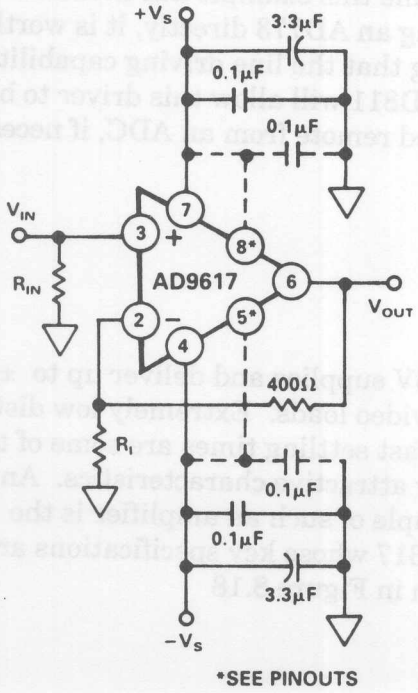
New high speed complementary bipolar processes with matching PNP and NPN transistors having F_ts of approximately 3GHz coupled with proprietary circuit designs have resulted in the development of an entire new class of ultra high speed op amps having bandwidths in excess of 150MHz. These op amps typically operate on ±5V supplies and deliver up to ±3V into video loads. Extremely low distortion and fast settling times are some of the other attractive characteristics. An example of such an amplifier is the AD9617 whose key specifications are given in Figure 8.18

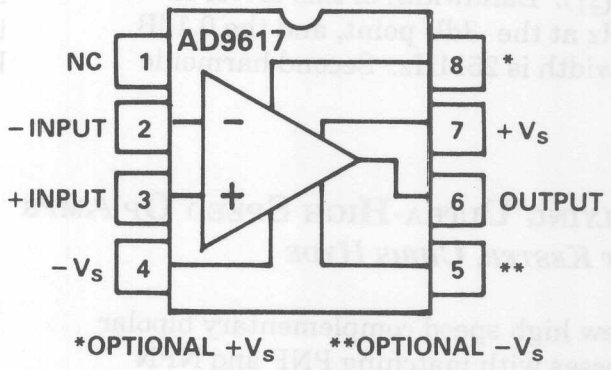
AD9617 CURRENT FEEDBACK AMPLIFIER KEY SPECIFICATIONS

- **Usable Closed Loop Gain Range: ±1 to ±40**
- **Low Distortion: -67dBc @ 20MHz**
- **Small Signal BW: 190MHz (A_V = +3)**
- **Settling Time: 10ns to 0.1%, 14ns to 0.02%**
- **±5V Power Supplies**

Figure 8.18

PROPER LAYOUT AND DECOUPLING IS CRITICAL TO AD9617 OP AMP PERFORMANCE





NOTE: FOR BEST SETTLING TIME AND DISTORTION PERFORMANCE, USE OPTIONAL SUPPLY CONNECTIONS. PERFORMANCE INDICATED IN SPECIFICATIONS IS BASED ON SUPPLY CONNECTIONS TO THESE PINS.

Figure 8.19

AD9617 FREQUENCY RESPONSE AND SETTLING TIME PERFORMANCE

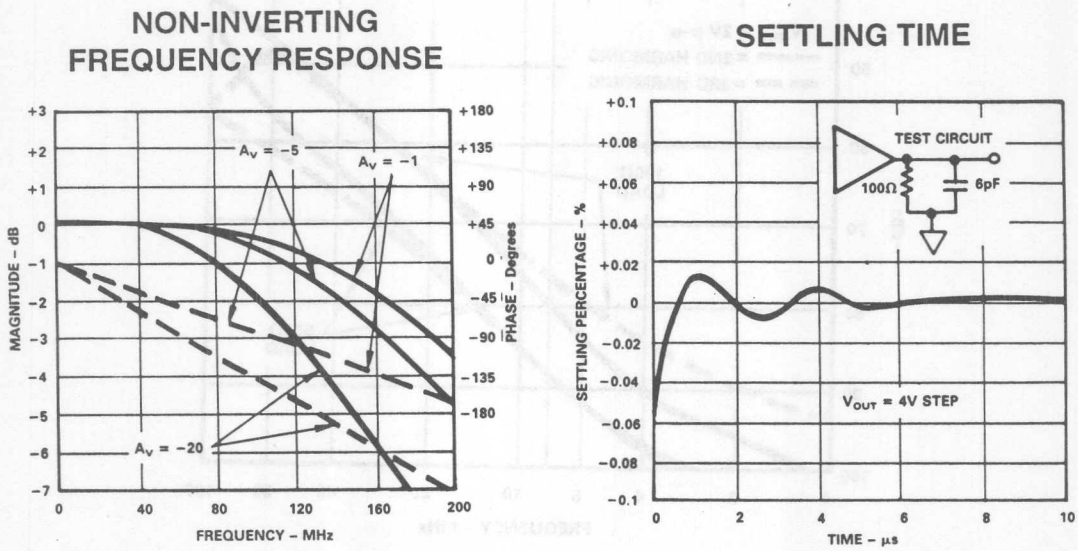


Figure 8.20

In order to achieve performance levels of this type, extreme attention must be given to every detail of PCB layout. Each power supply trace should be decoupled close to the package with a low inductance 0.1µF low inductance ceramic capacitor and at least a 3.3µF tantalum capacitor as shown in Figure 8.19. Gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave, or carbon film resistors. Stripline techniques should be used for lead lengths in excess of one inch. Sockets should be avoided because of their stray capacitance and inductance. If sockets are necessary, individual pin sockets such as AMP p/n 6-330808-3 should be used. Molded socket assemblies are unacceptable! On a proper layout with good decoupling techniques described above, the AD9617 frequency response and settling time characteristics shown in Figure 8.20 will be achieved. Harmonic distortion performance is shown in Figure 8.21 for both 100Ω and 500Ω loads. Note that even when heavily loaded in 100Ω, the harmonic distortion at 100MHz is better than -40dB.

Stray capacitance on the inverting input greater than 5pF will cause gain peaking and increases in settling time. Output load capacitance greater than 20pF will also cause settling time to increase unless the proper value of series isolation resistance is added. The effects on settling time due to input and unisolated output capacitance are shown graphically in Figure 8.22. The proper value of series isolation resistor for various values of load capacitance is shown in Figure 8.23.

AD9617 HARMONIC DISTORTION PERFORMANCE

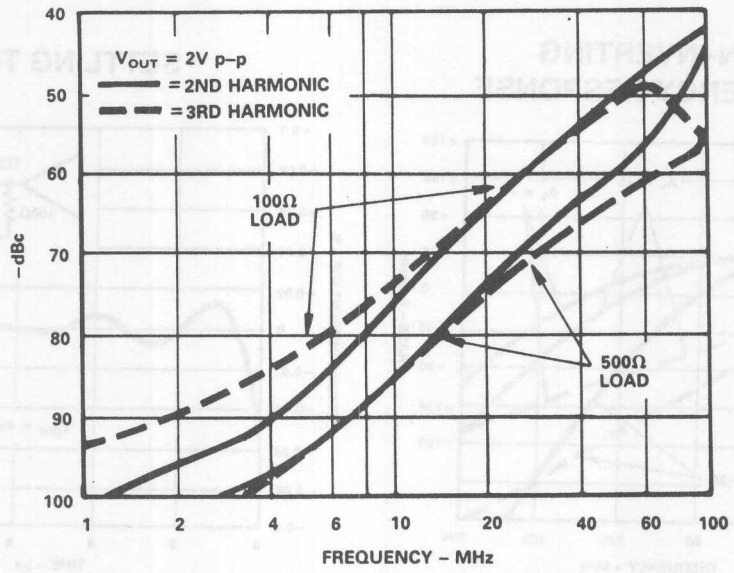


Figure 8.21

EFFECTS OF INPUT AND OUTPUT LOAD CAPACITANCE ON AD9617 SETTLING TIME

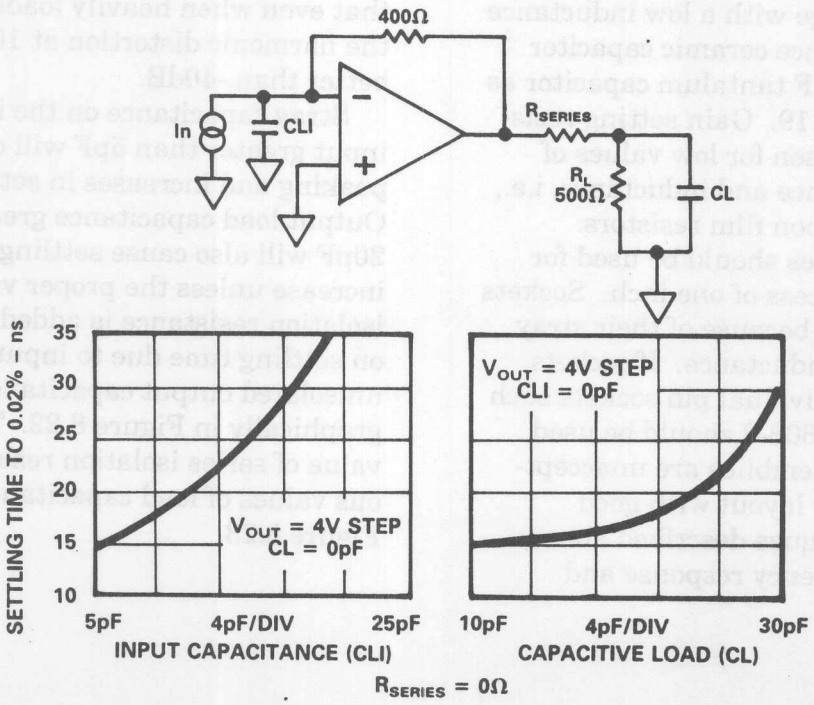


Figure 8.22

SERIES RESISTOR ISOLATES AD9617 OUTPUT FROM CAPACITIVE LOADS GREATER THAN 20pF

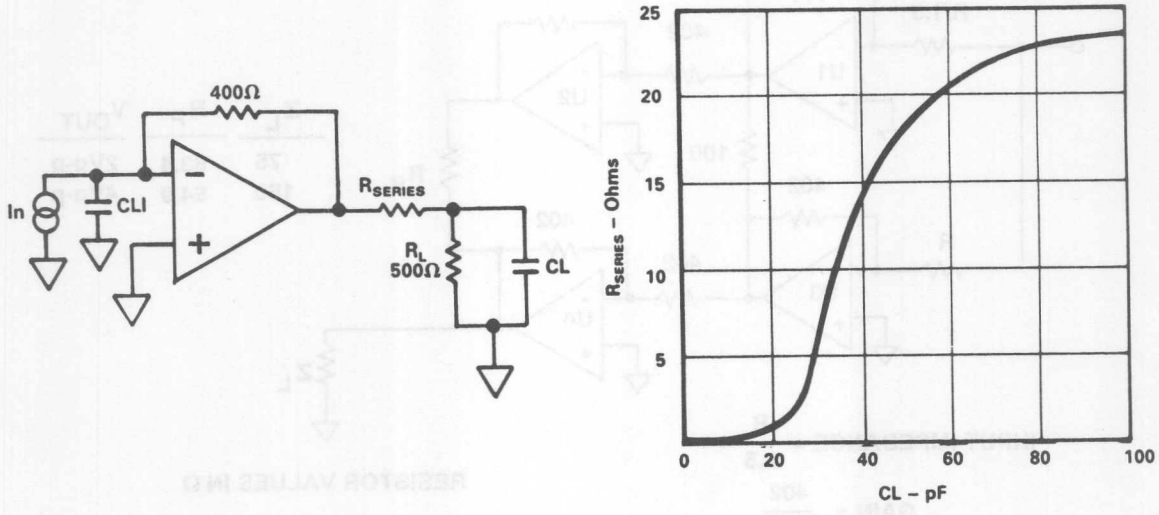
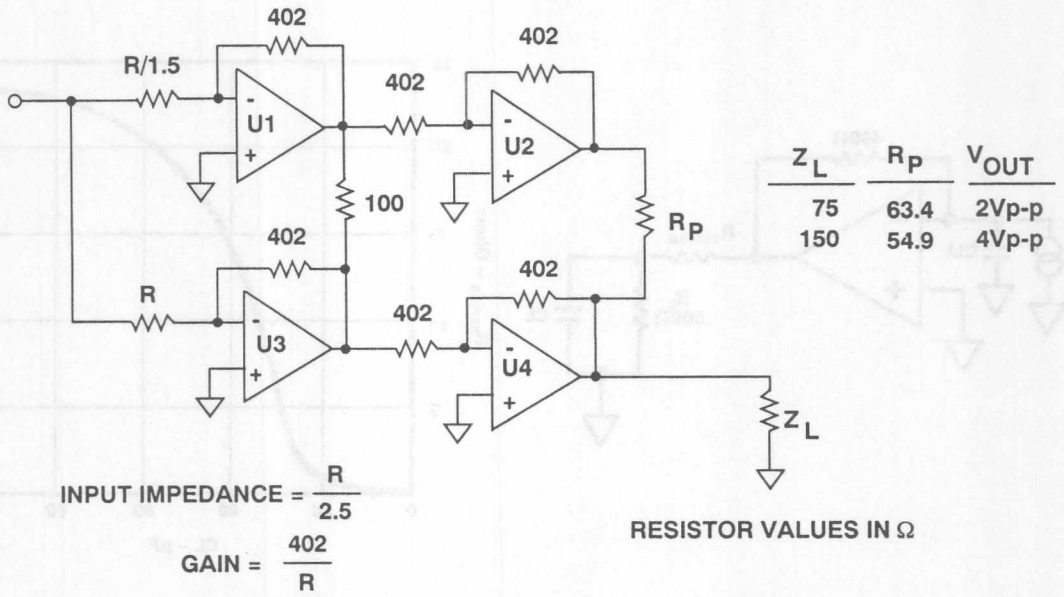


Figure 8.23

A LOW DISTORTION DRIVE CIRCUIT FOR PRECISION WIDE DYNAMIC RANGE ADCs

When gain is required ahead of precision wide dynamic range ADCs such as the AD9014, the circuit shown in Figure 8.24 is recommended in order to give ultra-low distortion levels. This configuration works well for analog input frequencies through 10MHz without introducing spurs that degrade the ADC's dynamic range. At 2.3MHz and 2V p-p output, all spurs generated in the drive circuit are less than -100dBc. The signal path is through U3 and U4, which are set up in a series inverting configuration to cancel even-order harmonics that are generated as the loop gain diminishes with frequency. U1 and U2 reduce the drive current of U3 and U4, respectively. Since U1 and U2 are set up in gains twice that of U3 and U4, the net effect is that the output stages of U3 and U4 are unloaded. This minimizes the odd-order harmonics generated in the output stages of U3 and U4. The gain of the overall block is +402Ω/R, and the input impedance is R/2.5. The output of the amplifier circuit is set up to drive either 2V p-p into 75Ω or 4V p-p into 150Ω by properly selecting R_p.

LOW DISTORTION DRIVE CIRCUIT (>100dBc) FOR AD9014 USING AD9617 OP AMPS



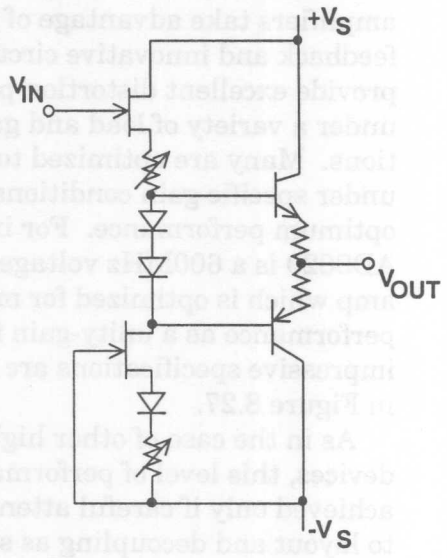
Z_L	R_P	V_{OUT}
75	63.4	2Vp-p
150	54.9	4Vp-p

Figure 8.24

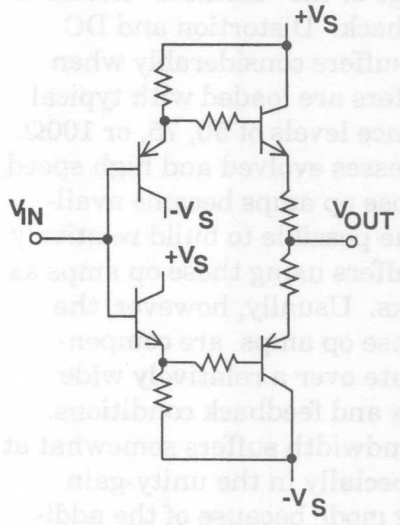
ULTRA HIGH SPEED BUFFERS

Buffer stages are basic to analog circuits, and are used to preserve signal accuracy and/or drive difficult loads. The previous section has discussed both video and ultra-high speed op amps which may be used as high performance signal buffers. In the early 1970's, before high speed IC op amps were available, the term *high speed buffer* usually referred to discrete *open loop* source and/or emitter follower circuits such as the two shown in Figure 8.25. The FET input circuit shown on the left was first implemented in hybrid form by National Semiconductor, Inc., and resulted in the industry-standard LH-0033 buffer. For circuits requiring higher speed without a FET input, the bipolar circuit on the right in Figure 8.25 was implemented by Analog Devices in a hybrid, the HOS-100. Although bandwidths in excess of 100MHz were achieved at fairly respectable levels of harmonic distortion, these hybrids were costly, high-power, and suffered from non-linearities (dc and ac) when loaded with impedances much less than 500Ω. An early IC implementation of these functions was the Precision Monolithic's, Inc. (now the PMI division of Analog Devices) BUF-03 shown in Figure 8.25. This open-loop IC buffer achieved a bandwidth of about 50MHz.

EARLY OPEN-LOOP, 100MHz BANDWIDTH HYBRID BUFFERS



LH-0033



HOS-100

Figure 8.25

8

EARLY IC OPEN-LOOP, 50MHz BUFFER, THE BUF-03

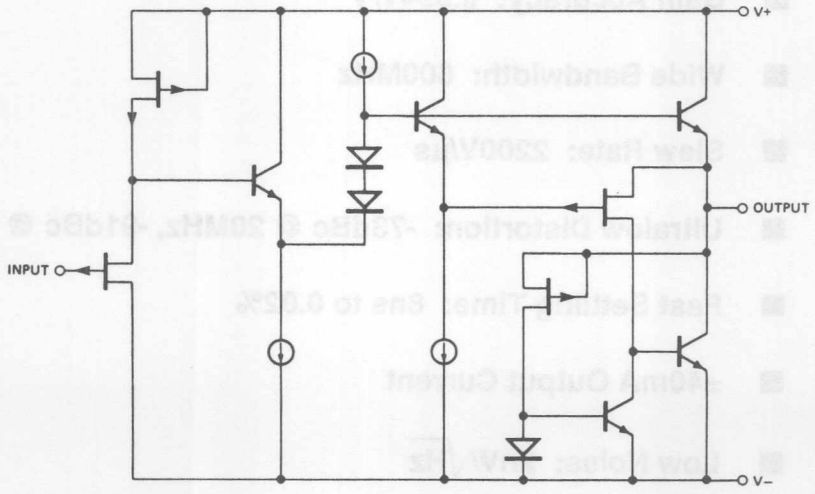


Figure 8.26

One of the problems with open loop buffers is that although high bandwidths may be achieved, these devices cannot take advantage of the "curative" effects of negative feedback. Distortion and DC performance suffers considerably when open loop buffers are loaded with typical video impedance levels of 50, 75, or 100Ω.

As IC processes evolved and high speed general-purpose op amps became available, it became possible to build relatively high speed buffers using these op amps as building blocks. Usually, however, the general-purpose op amps are compensated to operate over a relatively wide range of gains and feedback conditions. Therefore, bandwidth suffers somewhat at low gains, especially in the unity-gain non-inverting mode because of the additional external compensation usually required.

High speed complementary bipolar (CB) processes with matching PNP and NPN transistors have led to an entire new generation of op amps based on both traditional voltage feedback (VFB) and current feedback CFB) topologies. These amplifiers take advantage of negative feedback and innovative circuit design to provide excellent distortion performance under a variety of load and gain conditions. Many are optimized to operate under specific gain conditions to achieve optimum performance. For instance, AD9620 is a 600MHz voltage feedback op amp which is optimized for maximum performance as a unity-gain follower. The impressive specifications are summarized in Figure 8.27.

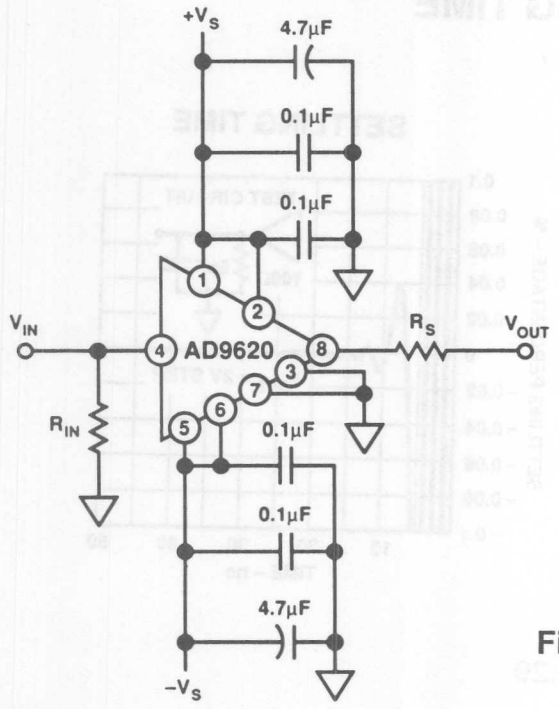
As in the case of other high speed devices, this level of performance can be achieved only if careful attention is given to layout and decoupling as shown in Figure 8.28. In the case of the AD9620, settling time and ac performance will be optimized with surface mount 0.1μF

AD9620 ULTRALOW DISTORTION 600MHz BUFFER KEY SPECIFICATIONS

- **Gain Accuracy: 0.994V/V**
- **Wide Bandwidth: 600MHz**
- **Slew Rate: 2200V/μs**
- **Ultralow Distortion: -73dBc @ 20MHz, -91dBc @ 2.3MHz**
- **Fast Settling Time: 8ns to 0.02%**
- **±40mA Output Current**
- **Low Noise: 2nV/$\sqrt{Hz}$**

Figure 8.27

PROPER LAYOUT AND DECOUPLING IS CRITICAL TO AD9620 BUFFER PERFORMANCE



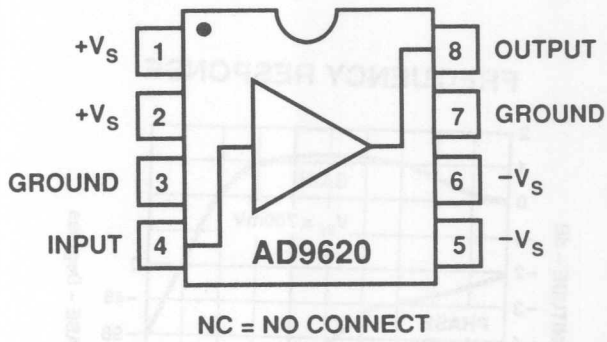


Figure 8.28

decoupling capacitors located within 50mils of their corresponding device pins, with the opposite side of the capacitor soldered directly to the ground plane. If surface mount capacitors cannot be used, radial lead ceramic capacitors with lead lengths less than 30mils are recommended. Low frequency power supply decoupling is also necessary and can be accomplished with 4.7µF tantalum capacitors mounted within 0.5 inch of the voltage supply pins. The interaction of the series inductance of the tantalum capacitor with the 0.1µF decoupling capacitor and the supply leads may cause high frequency oscillations at the output. These can be eliminated with a ferrite bead mounted between the tantalum and ceramic capacitors.

Connections to the AD9620 should be as short as possible. If either the source circuit or the driven circuit is further than 1 inch from the buffer, the PCB line impedances should be matched to the buffer input and output resistors. Basic microstrip techniques should be observed. The input and output termination resistors should both be connected as close to the AD9620 as possible.

The AD9620 should be soldered directly to the PCB with minimum vertical clearance. Molded sockets should not be used due to high pin reactances which will cause gain peaking and possibly induce oscillation. If sockets must be used for test or prototyping purposes, individual pin sockets such as the AMP-6-330808 series are recommended.

If the proper high speed techniques described above are observer, bandwidth and settling time performance shown in Figure 8.29 will be achieved.

AD9620 BUFFER FREQUENCY RESPONSE AND SETTLING TIME

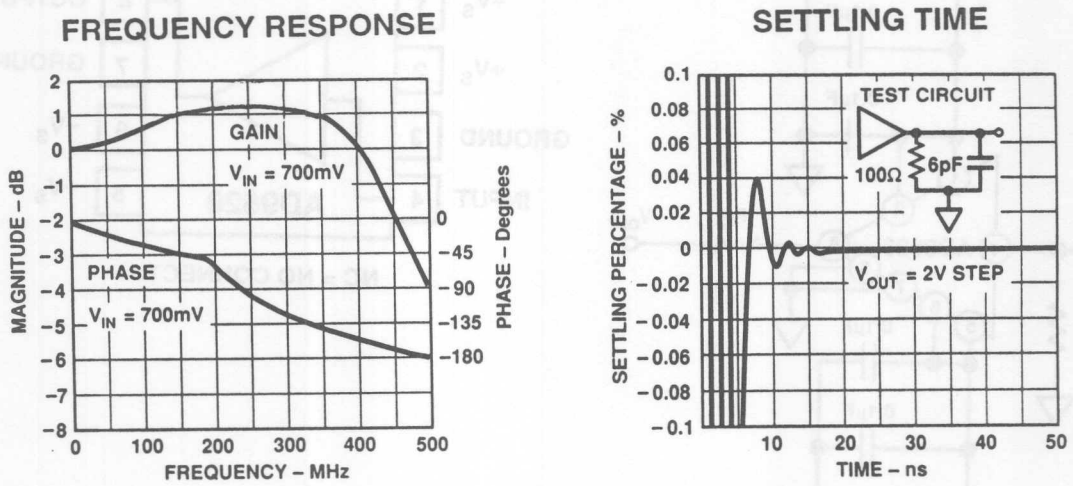


Figure 8.29

AD9620 BUFFER DC ENDPOINT LINEARITY ERROR FOR 100Ω AND 200Ω LOADS INDICATES OPEN-LOOP GAIN STABILITY OVER SIGNAL RANGE

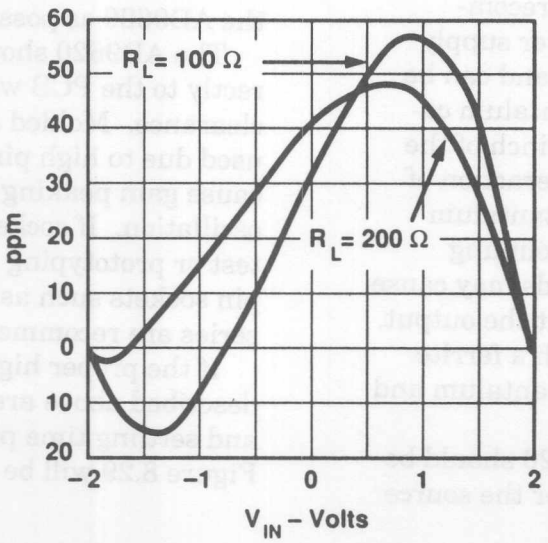


Figure 8.30

AD9620 BUFFER HARMONIC DISTORTION PERFORMANCE

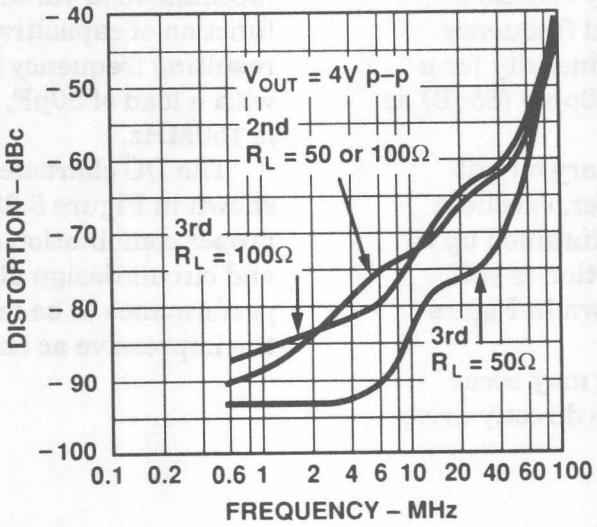


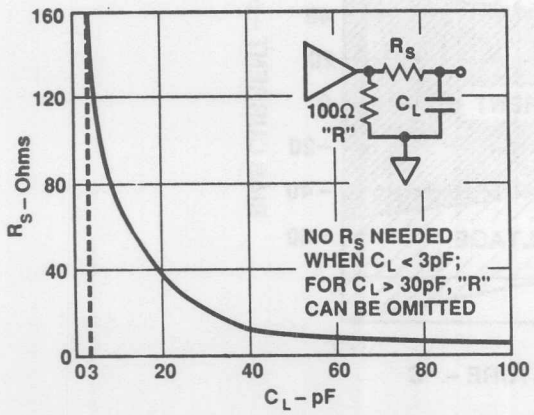
Figure 8.31

ISOLATION RESISTOR STABILIZES AD9620 WHEN DRIVING CAPACITIVE LOADS GREATER THAN 3pF

8

12 bit resolution @50mHz.

ISOLATION RESISTOR SELECTION



FREQUENCY RESPONSE

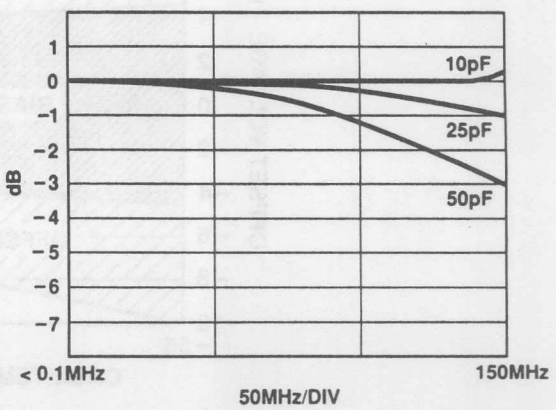


Figure 8.32

Although the open loop dc gain of the AD9620 is only about 2000, the proprietary voltage feedback circuit design of the AD9620 (Patents Pending) insures that this value is relatively constant under a variety of load and frequency conditions. DC endpoint linearity for a 100Ω load is better than 60ppm (85dB) as shown in Figure 8.30.

Because of the proprietary circuit design of the AD9620 buffer, excellent harmonic distortion is maintained up to 100MHz, where the distortion is still better than -40dBc as shown in Figure 8.31

Excessive gain peaking may occur when using the AD9620 to directly drive loads with more than 3pF of capacitance. To prevent this, a small value of resistance should be placed in series with the buffer output. Figure 8.32 shows the recommended value of resistance as a function of capacitive load as well as the resulting frequency response. Note that with a load of 50pF, the overall bandwidth is 150MHz.

The DC characteristics of the AD9620 shown in Figure 8.33 illustrate that the proper combination of process technology and circuit design allows respectable dc performance to be maintained along with the impressive ac characteristics.

AD9620 BUFFER OFFSET VOLTAGE AND BIAS CURRENT PERFORMANCE

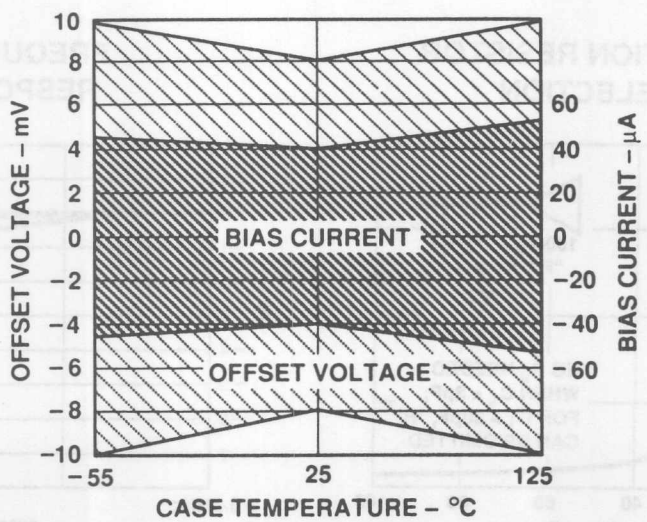


Figure 8.33

HIGH SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

WALT KESTER, CHRIS HYDE

A problem which has plagued the high speed circuit designers for years is that of transmitting video signals across noisy interfaces. This problem has been largely solved at low frequencies with high CMRR instrumentation amplifiers. At audio frequencies, products such as the SSM-2142 balanced line driver and SSM-2141/ SSM2143 line receiver offer outstanding CMRRs and the ability to transmit low-level signals in the presence of large amounts of noise.

The problem at video frequencies is twofold. First, video signals are generally single-ended and therefore don't adapt easily to balanced transmission line techniques. In addition, shielded twin-conductor coaxial cable with good bandwidth is usually somewhat bully and expensive. Second, designing high bandwidth, low distortion differential video amplifiers with high CMRRs at high frequencies is an extremely difficult task.

Even with the above problems, there are differential techniques available now which offer distinct advantages over single-ended methods. Some of these techniques make use of discrete components, while others utilize the latest in state-of-the-art video differential amplifiers.

Three solutions to the problem of differential transmission and reception are shown in Figure 8.34. The first represents the ideal case, where a balanced differential line driver drives a balanced twin-conductor coaxial cable which in turn drives a differential line receiver. This circuit, however, is difficult to implement fully at video frequencies for the reasons previously discussed.

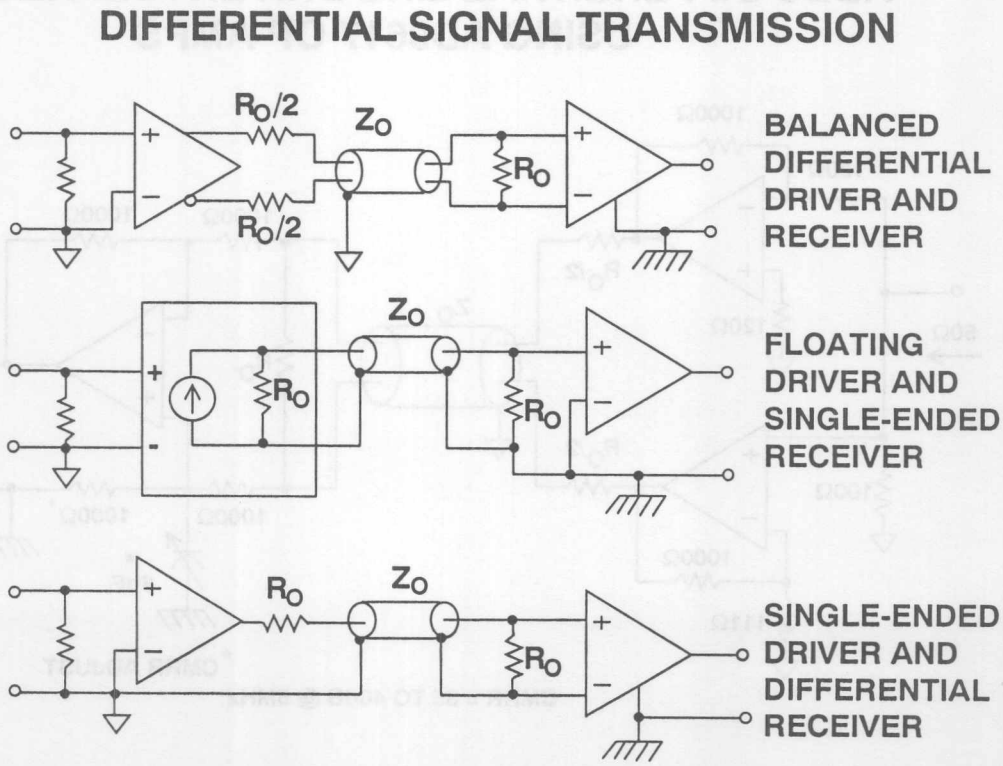


Figure 8.34

The second approach shown in Figure 8.34 uses a floating line driver (represented by the floating current source) to drive a single-conductor coaxial cable which is terminated at the receiving end in its characteristic impedance. Both the shield and the center conductor of the cable are driven by the floating line driver, and the cable is terminated at the receiving end. In this manner, noise between the two ground systems is isolated from the receiver output by the CMRR of the floating line driver.

The third approach makes use of a single-ended driver which drives a source-terminated coaxial cable. The shield of the coaxial cable is grounded at the transmitting end. At the receiving end, the coaxial cable is terminated in its characteristic impedance, but the shield is left floating. The common mode ground noise is rejected by the CMRR of the differential line receiver.

Figure 8.35 shows an implementation of the balanced driver and receiver approach using AD9617 op amps. Although bandwidths in excess of 100MHz can be achieved with this circuit, the CMRR at 5MHz is limited to between 35 and 40dB, even with the CMRR trims.

The second approach shown in Figure 8.34 using the floating line driver may be implemented using two Howland current sources (Reference 3, pp. 209-214, and Reference 4.). The single-ended Howland current source is shown in Figure 8.36 along with the equations which govern the resistor ratios. Two such circuits are connected as shown in Figure 8.37, one acting as a current source, and the other as a sink. This circuit provides about 800Ω of isolation between the two grounds, and yields better than 60dB harmonic distortion performance at 20MHz.

VIDEO DIFFERENTIAL LINE DRIVER AND RECEIVER USING AD9617 OP AMPS

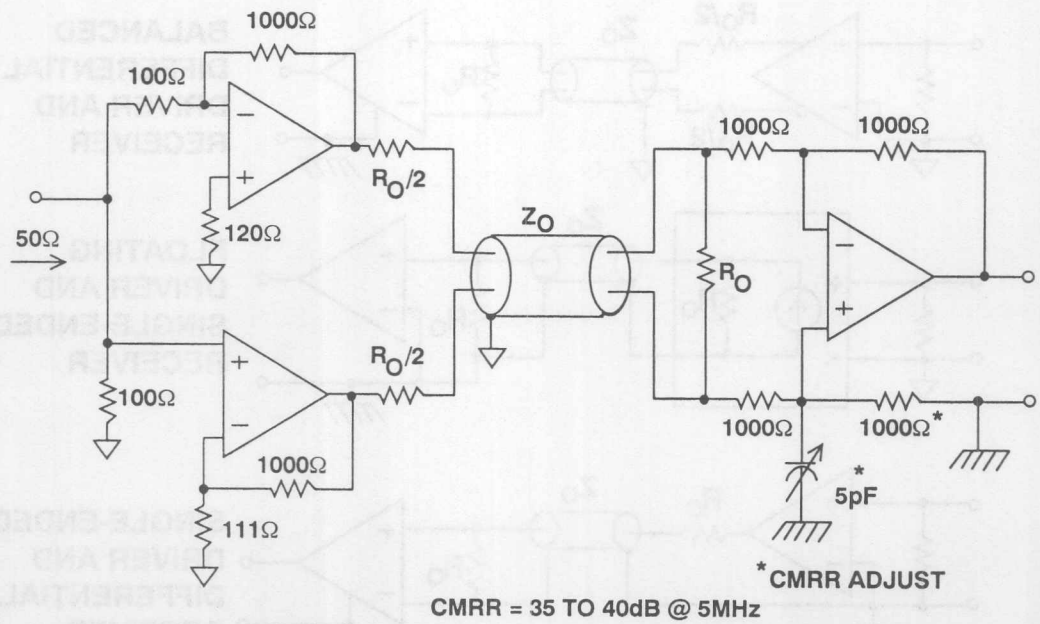
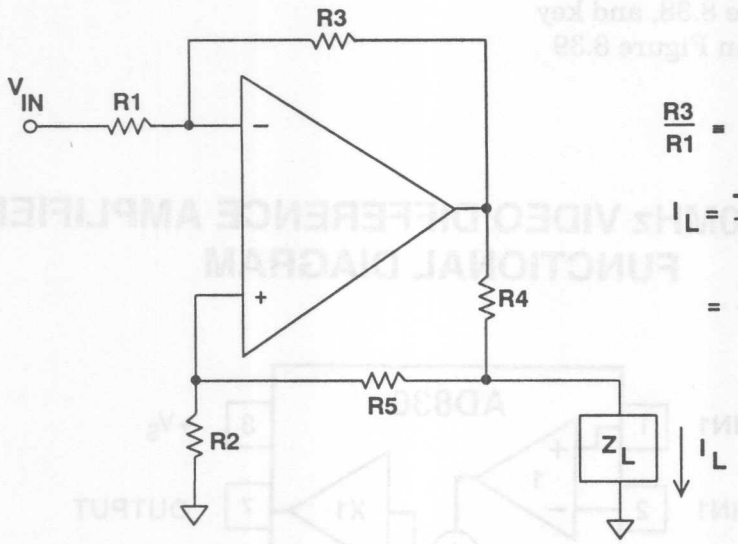


Figure 8.35

HOWLAND CURRENT SOURCE



$$\frac{R3}{R1} = \frac{R4 + R5}{R2}$$

$$I_L = \frac{-V_{IN}\,R3}{R1 \cdot R2}$$

$$= \frac{-V_{IN}\,(R4 + R5)}{R2 \cdot R4}$$

Figure 8.36

FLOATING LINE DRIVER

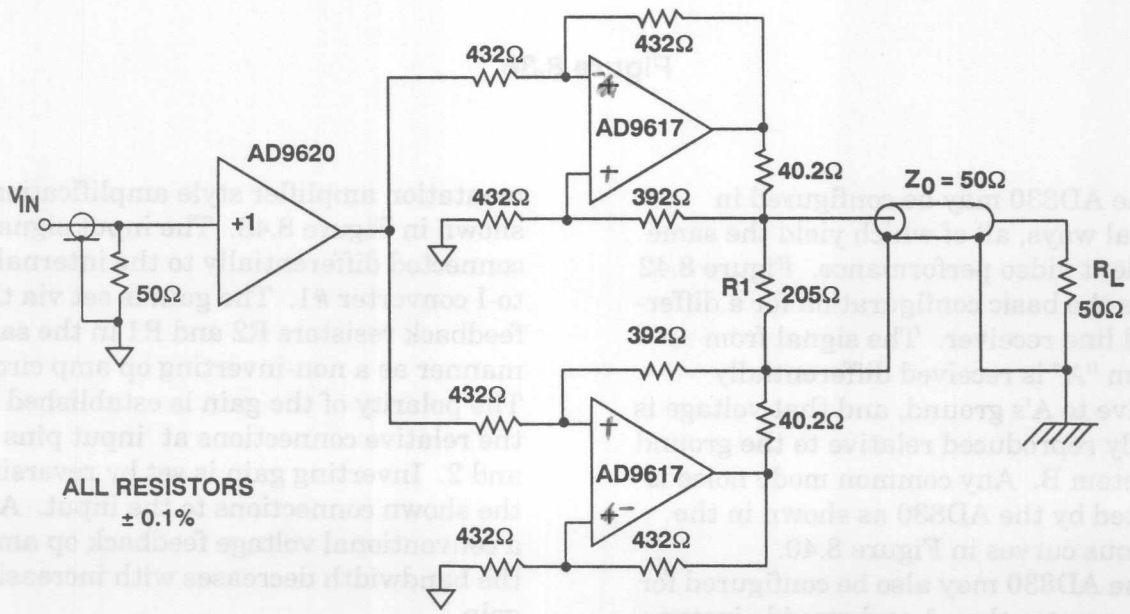


Figure 8.37

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Implementation of the third approach shown in Figure 8.34 is based on a state-of-the-art video difference amplifier, the AD830. A functional block diagram of the device is shown in Figure 8.38, and key specifications are given in Figure 8.39

CMRR and bandwidth performance for the device are shown in Figure 8.40, and harmonic distortion and differential gain and phase in Figure 8.41.

AD830 50MHz VIDEO DIFFERENCE AMPLIFIER FUNCTIONAL DIAGRAM

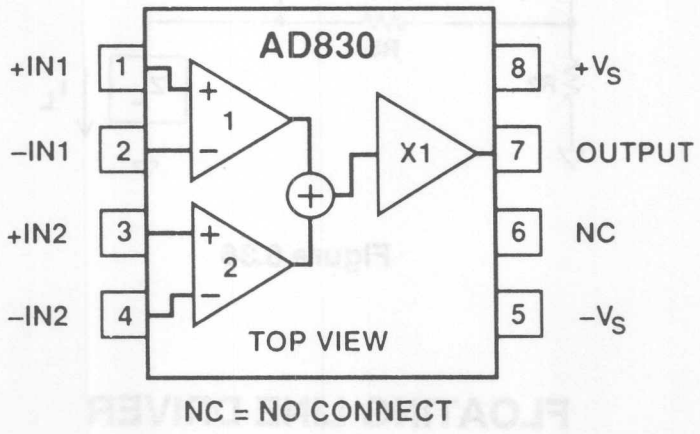


Figure 8.38

The AD830 may be configured in several ways, all of which yield the same excellent video performance. Figure 8.42 shows the basic configuration for a differential line receiver. The signal from system "A" is received differentially relative to A's ground, and that voltage is exactly reproduced relative to the ground in system B. Any common mode noise is rejected by the AD830 as shown in the previous curves in Figure 8.40.

The AD830 may also be configured for gains greater than 1 and provide instrumentation amplifier style amplification as shown in Figure 8.43. The input signal is connected differentially to the internal V-to-I converter #1. The gain is set via the feedback resistors R2 and R1 in the same manner as a non-inverting op amp circuit. The polarity of the gain is established by the relative connections at input pins 1 and 2. Inverting gain is set by reversing the shown connections to the input. As in a conventional voltage feedback op amp, the bandwidth decreases with increasing gain.

AD830 VIDEO DIFFERENCE AMPLIFIER KEY SPECIFICATIONS

- Common Mode Voltage Range: ±11.5V
- Differential Voltage Range: ±2V
- CMRR: 60dB @ 4.43MHz, 50dB @ 10MHz
- Bandwidth: 50Mhz
- Distortion: -60dBc @ 4.43Mhz
- Differential Gain: 0.1%, Differential Phase: 0.1°

Figure 8.39

AD830 CMRR AND FREQUENCY RESPONSE FOR ±5V AND ±15V SUPPLIES

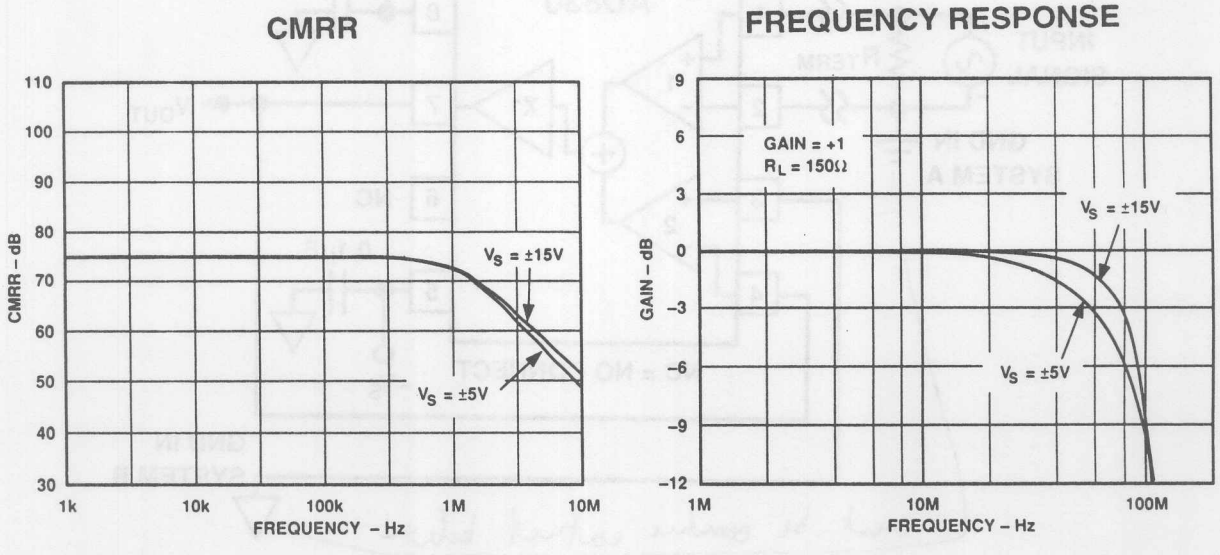


Figure 8.40

AD830 DIFFERENTIAL GAIN, PHASE, AND HARMONIC DISTORTION PERFORMANCE

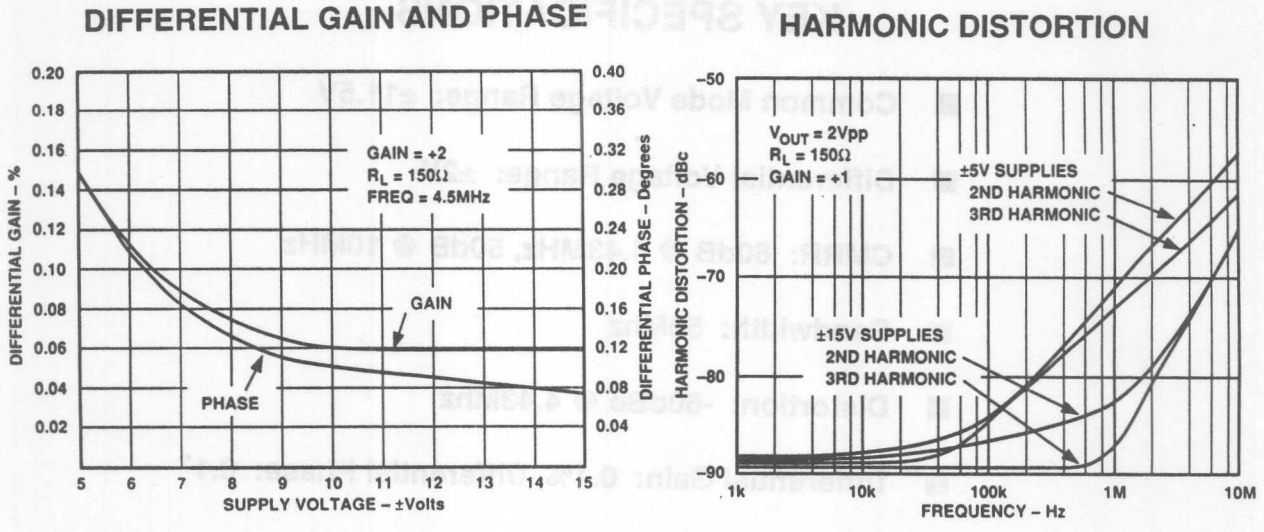


Figure 8.41

DIFFERENTIAL LINE RECEIVER USING THE AD830

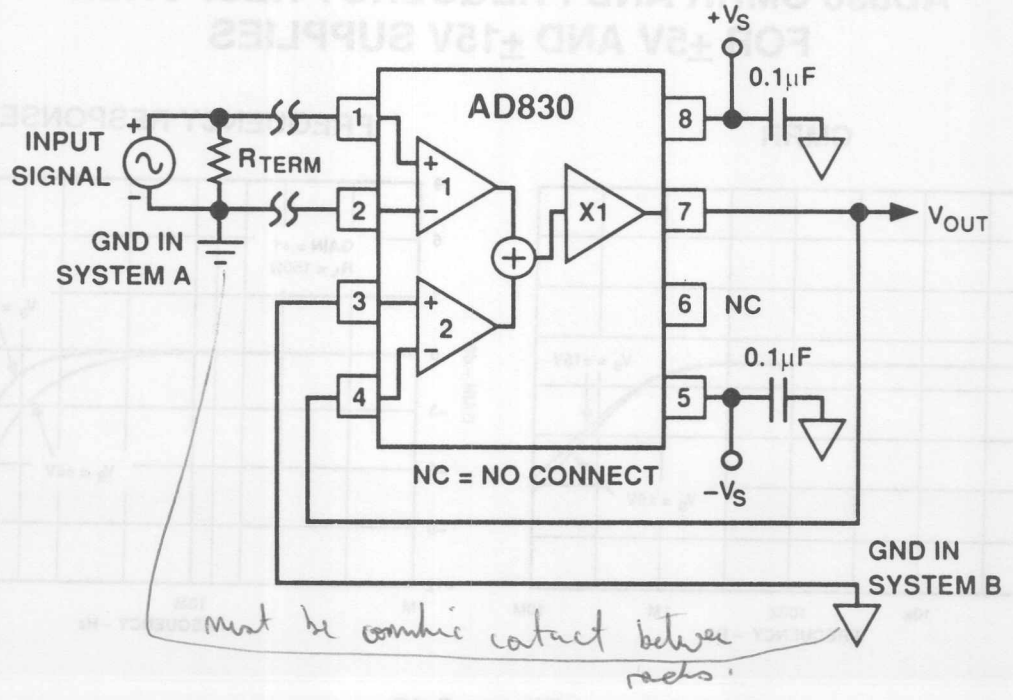
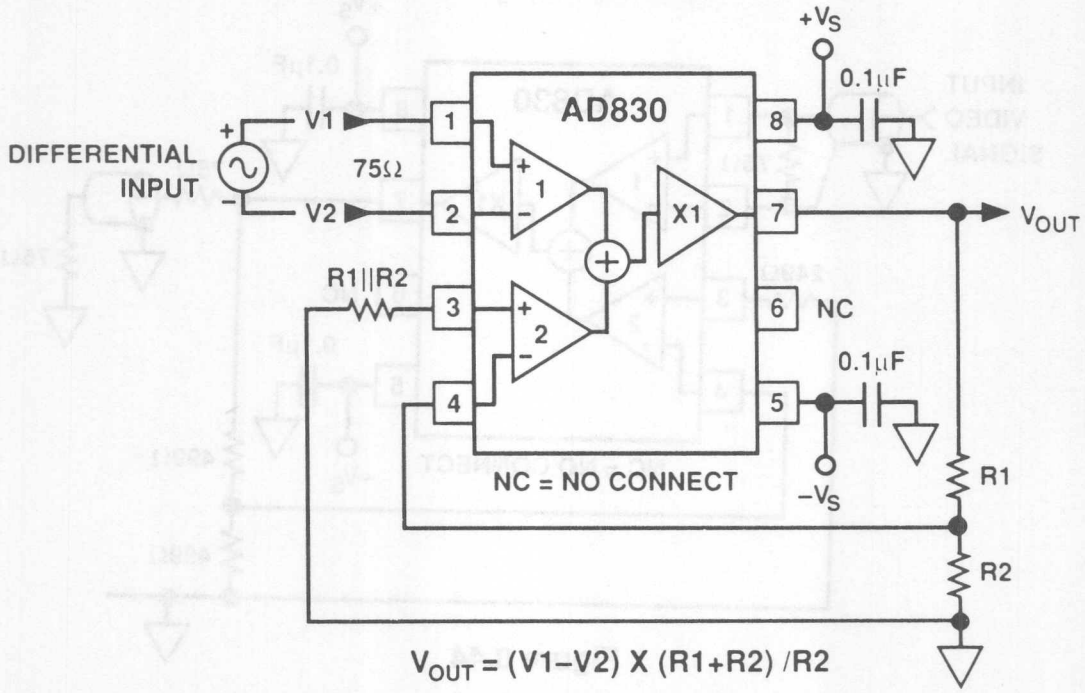


Figure 8.42

GAIN-OF-N INSTRUMENTATION AMPLIFIER USING THE AD830



$V_{OUT} = (V1–V2) \times (R1+R2) / R2$

GAIN = (R1+R2) /R2

Figure 8.43

The AD830 is ideally suited for the video cable receiver circuit shown in Figure 8.44. Here the cable shield is terminated at the driving end. The input signal to the AD830 is taken differentially from the conductor to shield and then amplified relative to the PCB ground. The 499Ω resistors set the gain at 2, with the 249Ω resistor included in series with the input to ground to cancel input bias current induced offsets. The 75Ω resistor connected in series with the output serves as the standard back termination impedance. Therefore, the net gain to the load resistor is unity.

VIDEO CABLE RECEIVER/DRIVER USING THE AD830

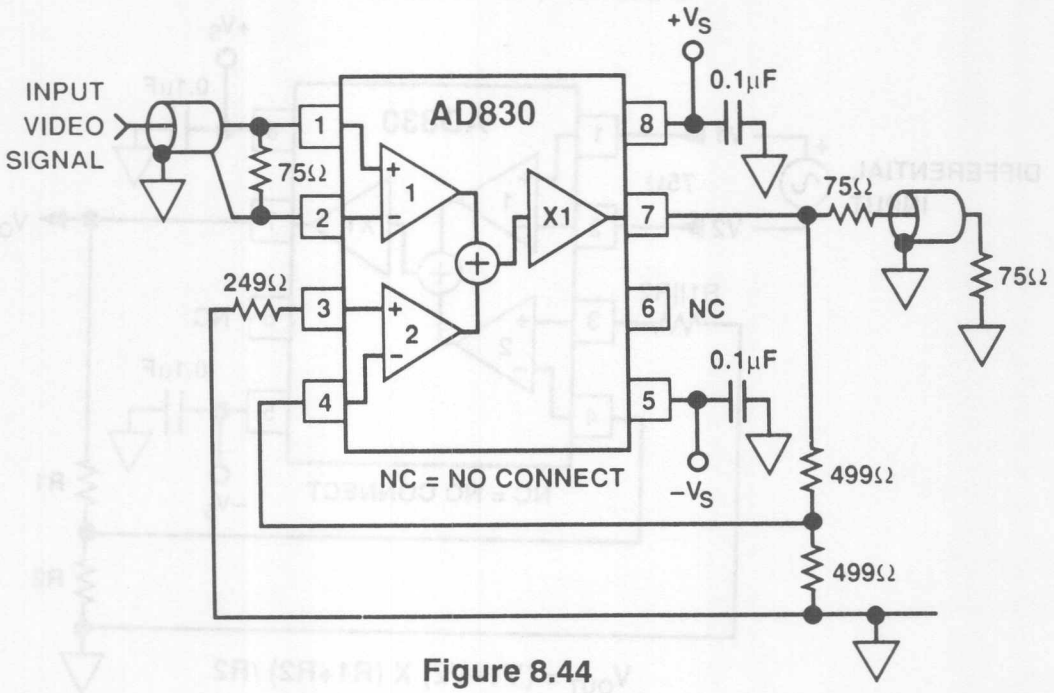
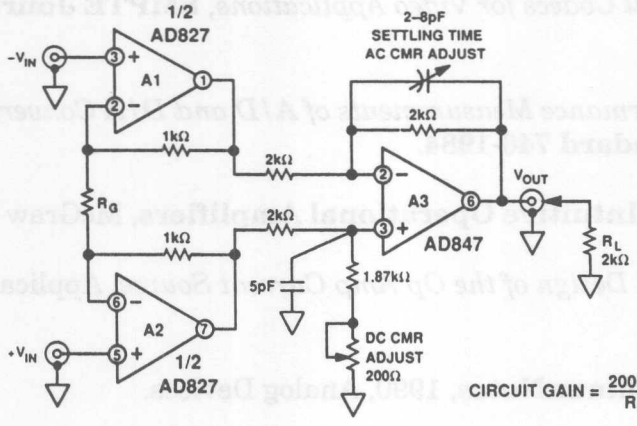


Figure 8.44

A HIGH SPEED THREE OP AMP INSTRUMENTATION AMPLIFIER

The circuit shown in Figure 8.45 lends itself well to CCD imaging and other video speed applications. It uses two high speed CB process op amps: Amplifier A3, the output amplifier, is an AD847. The input amplifier (A1 and A2) is an AD827, which is a dual version of the AD847. This circuit has the optional flexibility of both dc and ac trims for common-mode rejection, plus the ability to adjust for minimum settling time. Performance data is also given on Figure 8.45.

A HIGH SPEED, THREE OP AMP INSTRUMENTATION AMPLIFIER



INPUT FREQUENCY	CMRR
100Hz	88.3dB
1kHz	87.4dB
10kHz	86.2dB
100kHz	67.4dB
1MHz	47.1dB
10MHz	26.4dB

BANDWIDTH, SETTLING TIME AND TOTAL HARMONIC DISTORTION VS. GAIN

GAIN	R_G	C_{ADJ} (pF)	SMALL SIGNAL BANDWIDTH	SETTLING TIME TO 0.1%	THD + NOISE BELOW INPUT LEVEL @ 10kHz
1	OPEN	2–8	16.1MHz	200ns	82dB
2	2kΩ	2–8	14.7MHz	200ns	82dB
10	226Ω	2–8	4.5MHz	370ns	81dB
100	200Ω	2–8	660kHz	2.5µs	71dB

Figure 8.45

8

REFERENCES

1. W. A. Kester, *PCM Signal Codecs for Video Applications*, **SMPTE Journal**, No. 88, November 1979, pp. 770-778.

2. *IEEE Standard for Performance Measurements of A/D and D/A Converters for PCM Television Circuits*, **IEEE Standard 746-1984**.

3. Thomas M. Frederiksen, **Intuitive Operational Amplifiers**, McGraw Hill, 1988.

4. Tim Henry, *Analysis and Design of the Op Amp Current Source*, Application Note AN-587, Motorola, Inc., 1973.

5. **High Speed Design Seminar Notes**, 1990, Analog Devices.

SECTION IX
NON-LINEAR CIRCUIT APPLICATIONS

- Introduction to Dynamic Range Compression

- Voltage Controlled Amplifiers (VCAs):
  Structures, Using Analog Multipliers to Build VCAs, The X-Amp, AD600, AD602 Applications

- Logarithmic Amplifiers:
  Classifications, Scaling, Translinear Log Amps, Progressive-Compression Log Amps, The AD640 Log Amp, Log Amps Based on Bipolar Differential Stages

- Using the AD834 in DC to 500MHz Applications: RMS-to-DC Conversion, Voltage-Controlled Amplifiers, and Video Switches

- Video VCAs and Keyers Using the AD834 and AD811

SECTION IX

NON-LINEAR CIRCUIT APPLICATIONS

Barrie Gilbert, Bob Clarke

9.1 INTRODUCTION TO DYNAMIC RANGE COMPRESSION

In real-world signal-processing systems the signal of interest often exhibits a wide range of amplitudes. Familiar examples are: radio and radar receivers, where the dynamic range of an electromagnetic signal may be as high as 120 dB; analytical instruments such as gas chromatographs, where the output current of a photodetector may vary from picoamps to milliamps; sonar and ultrasound systems, where the attenuation of an acoustic signal varies rapidly with the path length; and so on. In terms of the signal voltage,

$$\text{Dynamic range (dB)} = 20\ lgt \frac{\text{Largest signal voltage}}{\text{Smallest signal voltage}}.$$

where *lgt* here, and throughout this section, means $\log_{10}$, or "logarithm to base 10".

Note that in a *linear-impedance* system, power is proportional to the voltage (or current) squared. Therefore, a 10,000:1 *voltage* ratio – that is, an 80 dB dynamic range – corresponds to a 100,000,000:1 *power* ratio. Accordingly:

$$\text{Dynamic range (dB)} = 10\ lgt \frac{\text{Largest signal power}}{\text{Smallest signal power}}.$$

We have chosen to use voltage ratios throughout this section because the majority of signal-processing circuits respond to purely voltage-mode signals, and occasionally operate on purely current-mode signals. Of course, at any branch in a real circuit there are both voltage- and current-mode components of the signal, hence finite power. On the other hand, the miniscule power "consumed" at the gate input of an MOS amplifier is not a very good indicator of the available dynamic range . This is because the voltage noise at this node of the circuit might be quite high, from microvolts to millivolts depending on the noise bandwidth and allowing for the possibility of 1/f noise, while the largest signal voltage might only be a volt or two. Power ratios are more useful in fixed-impedance systems, such as RF amplifiers operating between a resistively-matched source and load, usually 50 Ω.

At this point, we should differentiate between the dynamic range of the *signal* and that of the processing *system*:

$$\text{Signal dynamic range (dB)} = 20\ lgt \frac{\text{Largest actual signal voltage}}{\text{Smallest actual signal voltage}}$$

$$\text{System dynamic range (dB)} = 20\ lgt \frac{\text{Largest permissible signal voltage}}{\text{Smallest detectable signal voltage}}$$

We are solely concerned in this Section with the *system* dynamic range, in particular, with methods for maximizing this range, preferably matching or somewhat exceeding that of the signal. We will present the theoretical foundations as well as fully-tested practical circuits for dealing with many commonly-encountered situations in which signals of unusually wide dynamic range must be compressed to a more manageable level.

In dealing with such signals the need invariably arises for amplifiers which, on the one hand, can provide high gain with low noise levels when the signal is weak, in order to drive high-level processing circuits (such as A/D converters) while, on the other hand, being able to cope with large signals with minimum degradation. This Section also provides guidelines in the selection of suitable amplifiers for use in wide dynamic range systems.

DYNAMIC RANGE DEFINITIONS

$$\text{Dynamic range (dB)} = 20\ lgt \frac{\text{Largest signal voltage}}{\text{Smallest signal voltage}}$$

$$\text{Dynamic range (dB)} = 10\ lgt \frac{\text{Largest signal power}}{\text{Smallest signal power}}$$

$$\text{Signal dynamic range (dB)} = 20\ lgt \frac{\text{Largest actual signal voltage}}{\text{Smallest actual signal voltage}}$$

$$\text{System dynamic range (dB)} = 20\ lgt \frac{\text{Largest permissible signal voltage}}{\text{Smallest detectable signal voltage}}$$

Figure 9.1.1

9.1.1 NOISE LIMITATIONS

The dynamic range of all signal-processing systems is limited by random noise, which sets a fundamental bound on the smallest signal that can be detected or otherwise utilized with adequate signal-to-noise ratio (SNR). This noise may be generated by numerous mechanisms, including those associated with the source itself (e.g., antenna, photomultiplier, piezoelectric transducer, etc.) as well as by the active and passive devices in the amplifier.

Noise cannot be discussed without reference to bandwidth, which will be unavoidably limited by the type of amplifier(s) used. Deliberate filtering is often included in a signal-processing channel to reduce noise, as well as to improve the separation of wanted from unwanted signals. This may take the form of band-pass, low-pass or high-pass functions, or combinations of these, depending on the situation. Nonlinear filtering may also be used, for example, in order to minimize the disturbance of the signal path in the presence of impulsive noise. In some case, adaptive filtering is effective: a "lock-in amplifier" seeks a periodic (and often extremely weak) component in a noisy signal and automatically tunes a narrow-band filter to track its frequency (Reference 9.1.1). A key element of such a system is a synchronous detector.

The noise powers of uncorrelated sources add, so noise voltages (or currents) must be added using a root-sum-of-squares (RSS) calculation. This leads to some rather startling consequences. Suppose a system has a major voltage noise source of magnitude E_a and several minor noise sources which RSS sum to a magnitude of E_b. Then, for the major source to contribute almost 90 % of the total system noise, E_a needs to be only twice E_b. When $E_a/E_b = 5$, fully 98 % of the noise is due to E_a.

It follows that the overall noise performance of a practical system can benefit greatly by (1) minimizing the input-referred noise of the first stage and (2) using the highest possible gain in this stage. However, the second of these objectives is frequently unrealizable in systems that must handle signals of large dynamic range, because the high gain would then preclude distortion-free operation at maximum signal levels.

Noise is frequently specified in terms of "noise spectral density", or NSD. This term reflects the fact that the total noise power is directly proportional to the system's noise bandwidth, B_N (in Hertz). The NSD is therefore usually of interest in specifying a channel's *input-noise* limitations. Note that the noise bandwidth is not, in general, equal to the –3dB bandwidth. B_N can be viewed as the bandwidth of an equivalent system with a "brick-wall" cessation of response at that frequency. A system with a single-pole low-pass corner at $f_o = 1/2\pi T$ has a B_N equal to $\pi f_o/2$, or $1.57 f_o$, while for two such real-pole low-pass sections in cascade B_N is $\pi f_o/4$. (See Figure 9.1.2).

FILTER NOISE BANDWIDTHS

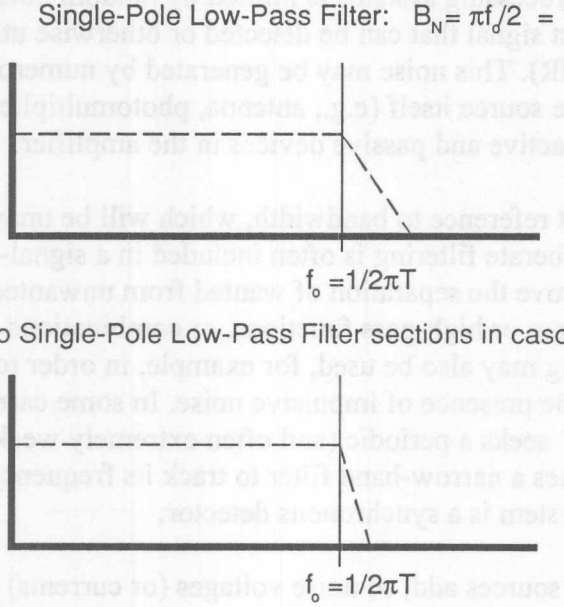


Figure 9.1.2

The total NSD will have both voltage- and current-components. We will use the symbol S_E to refer to the *voltage* noise spectral density and the symbol S_I to refer to the *current* noise spectral density. Since the noise power is proportional to the square of either the voltage or current, S_E and S_I have the dimensions of Volts per Root-Hertz and Amps per Root-Hertz, respectively. Noise signals are usually small, and therefore nonlinear effects are often negligible; in such circumstances, it is permissible to use superposition methods to evaluate each contributing source independently, followed by an RSS calculation to calculate the total noise. A notable exception is the logarithmic amplifier, where even very small noise voltages at the input can cause later stages in the amplifier to be in heavy limiting. Special approaches to both noise analysis and noise specification are required in such cases.

9.1.1.1 NOISE GENERATORS

We will only briefly review some of the most basic aspects of noise generation. The topic is well-covered in many fine standard texts; see, for example, Reference 9.1.2. The thermal (Johnson) noise voltage of an ideal resistor has an open-circuit magnitude of

$$S_E = (4kTR)^{0.5} \qquad \text{Eq. 9.1.1}$$

where T is the absolute temperature in Kelvins, k is Boltzmann's constant (1.38×10^{-23} Joules/Kelvin) and R is the resistance in Ohms. This evaluates to 0.129 nV/$\sqrt{}$Hz per root-ohm at

a temperature of 300 K (about 27 °C). We will refer to this constant as the *standard temperature ohm-normalized noise-spectral density*, and assign it the symbol S_Ω.

A 100 Ω resistor generates 10SΩ or 1.29 nV/√Hz at T = 300 K.

It is sometimes more useful to consider the resistor to be noise-free and then represent the noise as an equivalent current-source in shunt with it; of course, this has the same value as the short-circuit current-noise, $S_I = (4kT/R)^{0.5}$.

Some real resistors exhibit excess noise, which is a function of the current flowing in the resistor. This occurs whenever there are grain boundaries in the resistive material. Monolithic diffused and thin-film resistors do not have significant excess noise. The contact-related artifacts which were troublesome in thin-film resistors many years ago are nowadays eliminated through the use of one or more intermediate conductive layers.

The incremental channel resistance of a junction-FET or strongly-inverted MOS transistor behaves as a simple ohmic resistance, as far as noise is concerned, but has a value of 3/2*gm*. The transconductance, *gm*, is proportional to the width-to-length (W/L) ratio of the channel and the channel current (I_{DS}). Low-noise MOS stages demand the use of large interdigitated devices (large W) operating at high values of I_{DS}. Field-effect transistors, and in particular, MOS types, suffer from significant amounts of flicker noise. This noise increases with decreasing frequency, f, roughly with a $1/f^{\alpha}$ form, where α is often taken to be unity; thus, it is called "1/f noise". The topic is complex and even controversial (see, for example, Reference 9.1.3). However, as a guideline, 1/f noise can only be reduced by increasing the channel *area*, WL.

The base-emitter voltage, V_{BE}, of an ideal bipolar junction transistor (BJT) operating at a constant collector current I_C is not noise-free. There is unavoidable "granularity" in this current, expressed as the shot noise, which has a current noise spectral density of

$$S_I = (2qI_C)^{0.5} \qquad \text{Eq. 9.1.2}$$

This noise current operates on the transistor's (noiseless) incremental emitter resistance

$$re = kT/qI_C \qquad \text{Eq. 9.1.3}$$

to generate a voltage-noise spectral density of

$$S_E = (2qI_C)^{0.5}\, kT/qI_C$$

$$= kT\,(2/q)^{0.5}(1/I_C)^{0.5} \qquad \text{Eq. 9.1.4}$$

9

The shot-noise-induced voltage which effective appears in series with base-emitter path is thus inversely proportional to the square-root of the collector current and *totally independent of the transistor geometry or process technology.*

The V_{BE} noise for a BJT is 0.476 nV/√Hz per root-milliamp of I_C at T = 300 K.

It is interesting to note in passing that this noise is √2 times *smaller* than the noise in a real resistance of the same value as *re*.

NOISE GENERATORS

$$S_E = (4kTR)^{0.5} \qquad \text{Eq. 9.1.1}$$

A 100 Ω resistor generates $10S_\Omega$ or 1.29 nV/√Hz at T = 300 K.

$$S_I = (2qI_C)^{0.5} \qquad \text{Eq. 9.1.2}$$

$$re = kT/qI_C \qquad \text{Eq. 9.1.3}$$

$$S_E = (2qI_C)^{0.5}\, kT/qI_C \qquad \text{Eq. 9.1.4}$$

$$= kT\,(2/q)^{0.5}(1/I_C)^{0.5}$$

The V_{BE} noise for a BJT is 0.476 nV/√Hz per root-milliamp of I_C at T = 300 K.

$$R_N = \frac{S_E^2}{4kT} \qquad \text{Eq. 9.1.5}$$

Figure 9.1.3

9.1.1.2 NOISE OF TYPICAL INPUTS STAGES

When dealing with signal sources which have relatively low resistance, the input stage should be chosen to exhibit a low value of S_E. After all the noise generators have been RSS-added, the resulting S_E can be expressed as an equivalent noise resistance

$$R_N = \frac{S_E^2}{4kT} \qquad \text{Eq. 9.1.5}$$

An input-noise resistance of one quarter that of the source would contribute only 10% of the total noise. For bipolar input stages, the dominant noise-voltage generator is typically the base resistance, $r_{bb'}$. The channel resistances of field-effect transistors used in input stages exhibit the same noise behavior as simple resistors.

9.1.1.3 PRACTICAL AMPLIFIER NOISE SPECIFICATIONS

We can define the absolute lower limit of the system's dynamic range as simply being equal to its noise referred to the input, when driven from some specified source impedance, and in a specified bandwidth. This is commonly referred to as the "noise floor". A signal of the same magnitude presented to the input would result in a SNR of 0 dB, by definition. While this clearly represents the fundamental lower limit on the system dynamic range, it may be more meaningful to specify this limit in terms of some acceptable SNR, say, 20 dB. In analog channels handling digital data, this limit may be specified in terms of the maximum allowable bit-error-rate (BER).

In low-frequency applications, it is customary to specify the noise at the input of an amplifier in terms of separate voltage and noise components. The voltage noise spectral density is that noise which appears to be present at the input when this input is short-circuited. The best of contemporary op-amps exhibit values of the order of 1 to 5nV/√Hz. The bipolar-input AD797, optimized for this specification, has an NSD of 0.9 nV/√Hz. The generic workhorse "741", on the other hand, has a typical NSD of 15nV/√Hz due to the use of a four-transistor input stage operating at only ~10μA. As previously noted, there is a fundamental limit to what can be achieved at any given bias level. It is quite unrealistic to expect a micropower amplifier to have a low voltage-NSD. An ideal bipolar differential pair operating at a 1 μA cannot have a NSD lower than 30 nV/√Hz at room temperature.

In high-frequency circuits, it is common to specify the *noise-figure* of amplifiers. Noise Figure (NF) is often computed using the formula

$$NF = 10\ lgt\ \frac{e_n^2 + I_n^2 R_s^2 + 4kTR_sB_N}{4kTR_sB_N} \qquad \text{Eq. 9.1.6}$$

In the formula, e_n is the voltage noise, I_n is the current noise, B_N is the bandwidth in Hz, T is the absolute temperature in Kelvins, k is Boltzmann's constant (1.38×10^{-23} Joules/Kelvin) and R_S is the source resistance in Ohms.

9.1.2 DYNAMIC-RANGE LIMITATIONS

While noise limits the lower end of a system's dynamic range, performance at the upper end of the signal range is always degraded by the increasing importance of nonlinear aspects of circuit behavior. Thus, one way to specify the upper limit to the system's dynamic range is by determining the magnitude of the signal at which the *total harmonic distortion* reaches some maximum acceptable level, say 1 %. Alternatively, it may be specified as that signal level which causes the system's incremental gain to fall by 1 dB; this is called the *1 dB compression point* as shown in Figure 9.1.4.

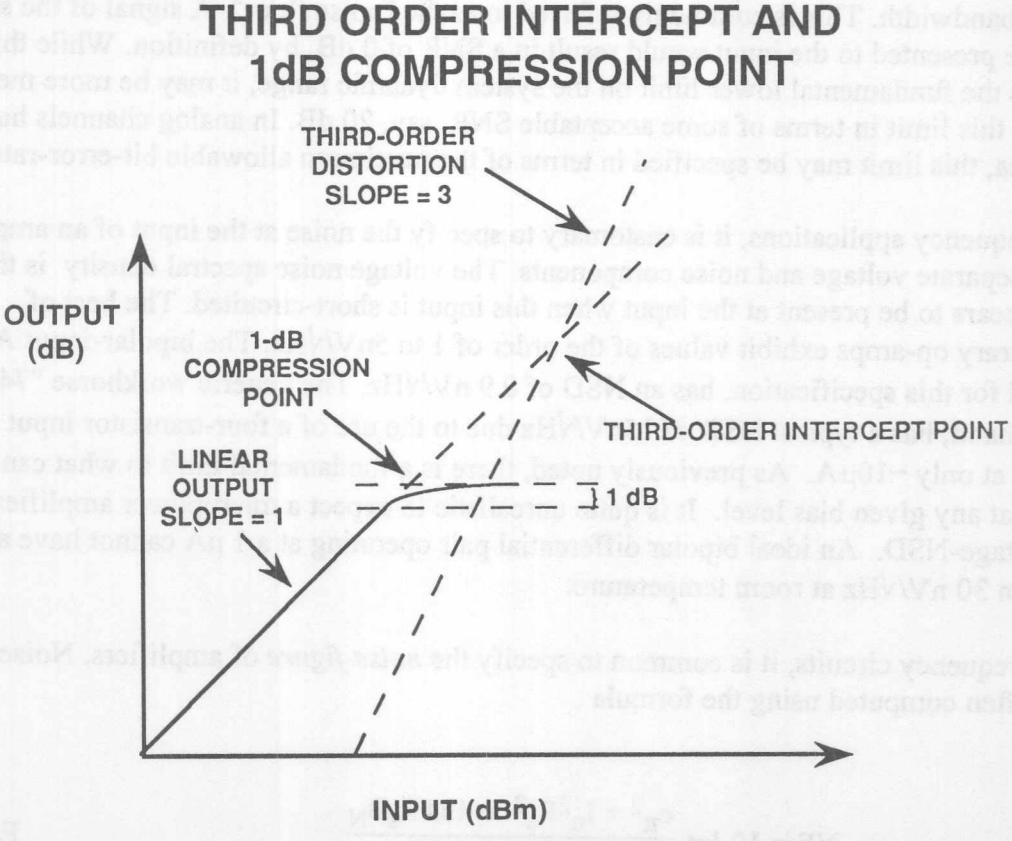


Figure 9.1.4

The term "spurious-free dynamic range", sometimes used in this context, is a little misleading because of course the distortion of any real amplifier is always finite, and a continuous function of signal level. In systems involving frequency-translation using mixers, distortion generates spurious signal components in the intermediate (IF) output spectrum, which are usually troublesome. The term *third-order intercept* is often used to specify the signal-handling capacity of the mixer; this can be defined as the extrapolated single-tone input level which would generate equal fundamental and third-harmonic outputs.

In some cases (such as the gas chromatograph) it may be more appropriate to characterize the entire dynamic range in "DC" terms, limited at the low end by such things as finite offset and input bias current of the input stage, and at the upper end by the onset of unacceptable nonlinearity or even clipping. In other words, the dynamic range in these cases is that range over which the measurement *accuracy* is held to within defined limits (for example, ±1 % of

reading). In such cases, flicker noise (both voltage and current), which dominates the performance of many such low-bandwidth systems, may impose a serious limitation on the available dynamic range.

From these considerations, it will be apparent that the precise method for defining the "dynamic range" of a given system clearly depends on the nature of the signal and the type of processing invoked. No single standard can be applied to adequately define the dynamic range of all systems. In fact, the central challenge of the design of a signal-processing system is ultimately that of optimizing each section so as to recover the maximum possible information (in digital systems, to achieve the lowest possible bit-error rate).

9.1.3 SIGNAL COMPRESSION

In some cases, a wide dynamic range is an essential aspect of the signal, something to be preserved at all costs. This is true, for example, in the high-quality reproduction of music. However, it is often necessary to compress the signal down to a smaller range without any significant loss of information. Compression is often used in magnetic recording, where the upper end of the dynamic range is limited by tape saturation and the lower end by the granularity of the medium. In professional noise-reduction systems, compression is "undone" by precisely-matched nonlinear expansion during reproduction. Similar techniques are often used in conveying speech over noisy channels, where the performance is more likely to be measured in terms of word-intelligibility than audio fidelity. The reciprocal processes of compressing and expanding are implemented using "compandors"; many schemes have been devised to achieve this function.

In radio systems, the received energy exhibits a large dynamic range due to the variability of the propagation path, requiring dynamic-range compression in the receiver. In this case, the wanted information is in the modulation envelope (whatever the modulation mode), not in the absolute magnitude of the carrier. For example, a 1 MHz carrier modulated at 1 kHz to a 30 % modulation depth would convey the same information whether the received carrier level is at 0 dBm or –120 dBm. Some type of automatic gain control (AGC) in the receiver is invariably utilized to restore the carrier amplitude to some normalized reference level in the presence of large input fluctuations. AGC circuits are dynamic-range compressors which respond to some metric of the signal – often its mean amplitude – acquired over an interval corresponding to many periods of the carrier. Consequently, they require time to adjust to variations in received signal level. The time required to respond to a sudden increase in signal level can be reduced by using peak detection methods, but with some loss of robustness, since impulsive noise can now activate the AGC detection circuits. Nonlinear filtering and the concept of "delayed AGC" can be useful in optimizing an AGC system. Many tradeoffs are found in practice; Figure 9.1.5. shows a basic system.

A TYPICAL AGC SYSTEM

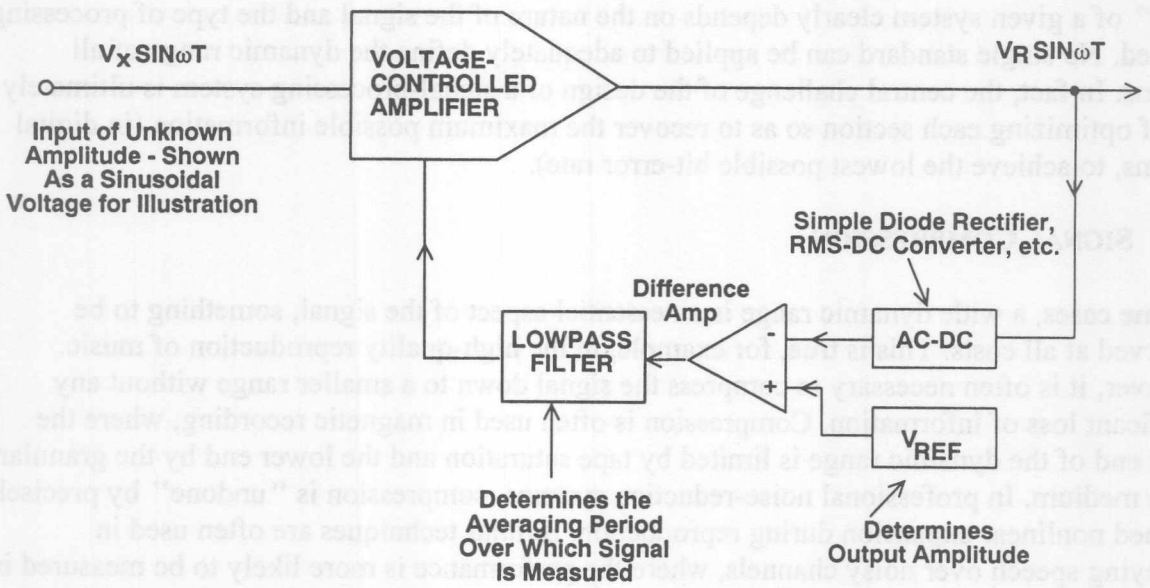


Figure 9.1.5

In other cases, the system is required to respond almost instantaneously to the signal. For example, the waveshape of the pulse output of a microwave radar detector must be preserved over many decades of amplitude, which requires that each value of voltage on the input waveform maps uniquely to a value of the output, with essentially the same response for signals of some arbitrarily low frequency (often DC) up to the maximum bandwidth of the channel. The most common mapping functions are the logarithm (or its near-neighbor, the inverse hyperbolic sine) and square-root.

In this section a variety of practical circuit solutions will be presented for compressing signals of large dynamic range. Because of their extensive scope, we will not discuss signal-path filtering techniques, except where they arise incidentally.

9.1.4 LINEAR VS NONLINEAR COMPRESSION

We can divide dynamic range compression systems into "linear" and "nonlinear". In the first category, the gain of the amplifier(s) in the processing chain is independent of the magnitude of the signal but is arranged to vary such a way as to render the output (that is, its peak, mean or RMS value) essentially constant. The harmonic distortion is relatively low.

These systems use what are often called variable-gain amplifiers. While correct, this lacks precision, because *nonlinear* amplifiers (such as log-amps) also exhibit variable gain, but in direct response to the signal magnitude. The term voltage-controlled amplifier (VCA) is preferred in this context; it clearly describes the way in which the gain-control is implemented while allowing latitude in regard to the actual circuit means used to achieve the function. In fact, the gain may be controlled by a *current* within the circuit, but usually by conversion from a voltage at the control interface.

Analog multipliers and dividers are sometimes used as VCAs, but far more optimal circuit topologies are available.

AGC systems use one or more VCAs in conjunction with a level detector and low-pass filter (LPF), usually driven by the output. Occasionally, an analog divider will be used, in which case the input level is extracted and used as the denominator; unlike conventional (feedback) AGC systems, this approach makes use of *feedforward* control.

Any voltage-controlled amplifier may be converted to digital control by the inclusion of a DAC. There are relatively few amplifier products available which provide direct digital control, for reasons explained in the following section.

A special type of VCA is used in "swept-gain" applications. This is an amplifier whose gain is controlled without measurement of the actual signal level; instead, it utilizes the predictable magnitude of the signal as a function of time (or occasionally some other parameter). For example, in medical ultrasound systems the attenuation varies with the depth of the tissue layer being imaged. Similar circumstances arise in sonar and short-range radar.

By contrast, nonlinear dynamic-range compression is used in circumstances where low harmonic distortion is not a requirement. Log-amps provide the best example of this type of compression. All types of log-amps produce a low-dynamic-range output without the need to first acquire some measure of the signal amplitude for use in controlling gain. As we shall see later, these can be basically divided into baseband and demodulating types. Baseband log-amps produce an output with minimal time delay and do not employ rectification (that is, signal detection). Demodulating log-amps provide the detection function, and produce a baseband output from a higher-frequency input; filtering is employed on the detected output only to remove the unwanted high-frequency components. In special cases, VCAs of the type used for AGC or swept-gain applications can be used for nonlinear compression; some examples will be presented. In all such cases, an A/D converter of moderate resolution (say, 8 bits) can be made to handle a signal of large dynamic range (say, 16 bits, or 96 dB) while preserving equal incremental resolution over the whole range.

REFERENCES

9.1.1 See , for example, **Lock-In Amplifiers: Principles and Applications** by M. L. Meade, Peter Peregnius, Ltd., 1983

9.1.2 **Low Noise Electronic Design** by C. D. Motchenbacher and F. C. Fitchen, John Wiley Inc., 1973.

9.1.3 **The MOS Transistor** by Y.P. Tsividis, McGraw-Hill, Inc., 1987.

9.2 VOLTAGE CONTROLLED AMPLIFIERS (VCAS)

There are many ways to build voltage-controlled amplifiers. The literature goes back to the earliest days of electronics, amounting to thousands of papers and hundreds of patents. This section will review some of the most important contemporary techniques and show several practical applications.

Such digitally-controlled circuits as software-programmable-gain amplifiers or multiplying D/A converters (MDACs) provide discrete-gain steps. The Analog Devices LOGDAC™ AD7111 is a development of the MDAC approach to gain control. This special-purpose CMOS D/A converter emulates an attenuator with a range of 0 to –88.5 dB and resolution of 0.375 dB (a 4.4 % gain change per step) using an 8-bit control input.

Often, much finer gain-control is necessary, which requires the use of a larger control word. This is not of itself a basic problem: if one wished to achieve the above range of 88.5 dB with the resolution increased to 0.086 dB (a 1 % gain change per step), it would require a 10-bit word. However, important practical issues arise. In applications where the dynamic range is wide (88.5 dB corresponds to a voltage ratio of about 27,000:1), it follows that at the low end of the gain-control range the channel must process very small signals.

The complete separation of the digital control inputs from these weak signals is difficult, at both the silicon level and the board level. For example, this problem becomes severe when it is necessary to update the gain quickly – over a period of a few microseconds or less – in which case the feedthrough of rapidly-changing binary data edges ("glitching") becomes intolerable.

Furthermore, the use of MOS switches, such as those found in MDACs and their derivatives, is not conducive to low-noise, wideband design: the Johnson noise of the FET channel resistance can be reduced only by the use of large-geometry devices, and these in turn exhibit significant parasitic capacitances, leading to problems in controlling both the phase and the amplitude of the system response under all conditions, but particularly at high attenuation levels.

Consequently, in applications where (a) the signal to be compressed covers a wide dynamic range, (b) the required accuracy of the AC gain and phase response is high, and (c) the gain must be swept rapidly, digital control techniques are not attractive and in the most critical applications cannot be used at all. In these cases, a voltage-controlled amplifier (VCA) is indispensable.

It must also be remembered that there remain numerous applications where direct analog control is still the preferred approach from other considerations. For instance, it is inconvenient to distribute the control data on a wide digital bus to a large number of parallel signal-processing channels, as in an ultrasound system. It is also simpler to implement AGC systems using VCAs.

9.2.1 A COMMON VCA STRUCTURE

A popular approach to the design of a VCA is to use the reliable exponential relationship between collector current and base-emitter voltage in a bipolar junction transistor, through which means it is possible to achieve a gain-control range of several decades. A very widely-used

circuit is shown in Figure 9.2.1. The signal voltage V_Y is first converted to a complementary pair of currents, which are here denoted as $(1+Y)I_Y$ and $(1-Y)I_Y$, by a voltage-to-current (V/I) converter formed by Q1, Q2 and R_Y. The "modulation index" Y has a maximum range of ±1; in practice, it will have a peak value of about 0.75, to minimize distortion due to the nonlinear V_{BE} of the transistors. To a good approximation, $Y = V_Y/I_YR_Y$ (true when $I_YR_Y \geq 100$ kT/q).

A COMMON VARIABLE -GAIN CELL: THE "CONTROLLED CASCODE"

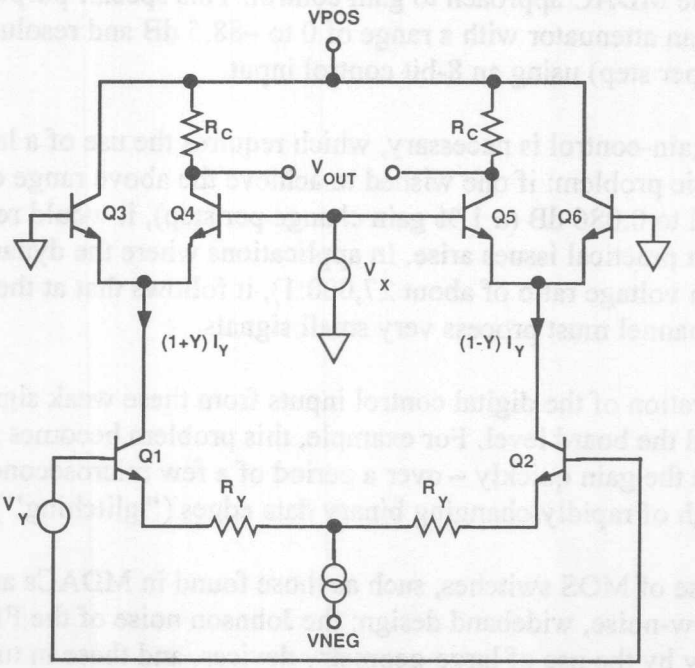


Figure 9.2.1

The signal-plus-bias currents are then applied to a "current-fork", comprising Q3 through Q6, that steers some fraction, $0 \leq X \leq 1$, of the signal currents to the output load resistors, and dumps the remainder to the positive supply. These transistors also act as a cascode stage, which extends the frequency range of the amplifier; because of this feature, we will refer to this cell as a "controlled cascode".

The parameter X is determined by the gain-control voltage V_X. It is readily shown that

$$X = \frac{exp(V_X/V_T)}{1 + exp(V_X/V_T)} \qquad \text{Eq. 9.2.1}$$

where V_T is the thermal voltage kT/q, which has a value of 25.85 mV at T = 300 K (about 27°C). At this temperature, X is 0.99 when V_X = 120 mV and 0.01 when V_X = –118 mV. If the

system gain is normalized to 0 dB when X = 1, the loss is 6 dB for $V_X = 0$; Figure 9.2.2 shows the decibel value of gain as a function of V_X at three temperatures.

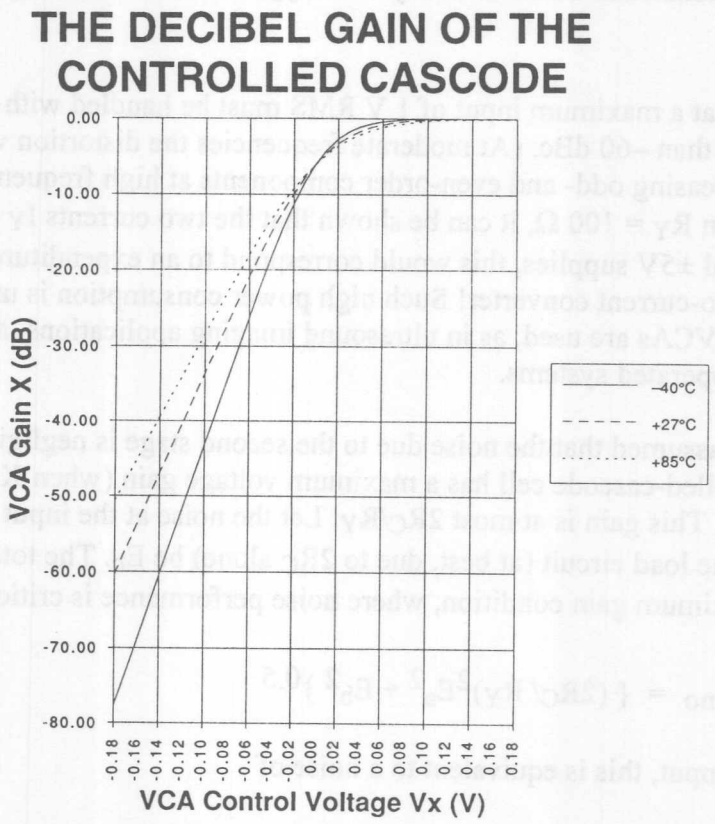


Figure 9.2.2

Several potential problems are immediately apparent from this graph. First, the circuit's control function is not "linear in decibels"; it approaches this condition only for very high attenuation. Second, the attenuation is a strong function of temperature; this, and the nonlinear control function, may not matter too much in closed-loop AGC systems, but both would be troublesome in "swept-gain" VCA applications, or in feed-forward AGC systems. The temperature-sensitivity can be addressed using special resistors to form an attenuator between the actual gain-control voltage and the base nodes.

Apart from these obvious weaknesses, this cell has additional problems. Notice that the lower end of the input dynamic range is fundamentally limited by the Johnson noise of R_Y. If this resistor is reduced to the point where acceptable noise performance is achieved, the upper end of the dynamic range will also be reduced, due to the onset of distortion, unless very large values of bias current I_Y are used.

For example, suppose we wish to achieve a short-circuited input noise spectral density of 1.5 nV/√Hz at 300 K (which corresponds to 15 μV in a 100 MHz bandwidth) then R_Y can be no more than 135 Ω. This assumes that Q1 and Q2 have no ohmic resistances; in practice, the $r_{bb'}$

of both transistors must be subtracted from R_Y to maintain the desired total resistance. Even well-optimized monolithic transistors may have $r_{bb'}$ values of 15 Ω, typically requiring R_Y to be 100 Ω.

Now postulate that a maximum input of 1 V RMS must be handled with a total harmonic distortion of less than –60 dBc. (At moderate frequencies the distortion will be third-order, but there will be increasing odd- and even-order components at high frequencies.) To meet this last requirement when R_Y = 100 Ω, it can be shown that the two currents I_Y must each be at least 23 mA; using typical ±5V supplies, this would correspond to an expenditure of almost half a watt in just the voltage-to-current converter! Such high power consumption is unwelcome where a very large number of VCAs are used, as in ultrasound imaging applications, and would be intolerable in most battery-operated systems.

So far, we have assumed that the noise due to the second stage is negligible, but that can only be true if the controlled-cascode cell has a maximum voltage gain (when X = 1) that is much greater than one. This gain is at most $2R_C/R_Y$. Let the noise at the input (due to $2r_{bb'} + R_Y$) be E_a, and that in the load circuit (at best, due to $2R_C$ alone) be E_b. The total noise at the output, E_{no}, for the maximum gain condition, where noise performance is critical, is

$$E_{no} = \{ (2R_C/ R_Y)^2 E_a^2 + E_b^2 \}^{0.5} \qquad \text{Eq. 9.2.2}$$

Referred to the input, this is equivalent to a noise of

$$E_{ni} = \frac{\{ (2R_C/ R_Y)^2 E_a^2 + E_b^2 \}^{0.5}}{2R_C/ R_Y} \qquad \text{Eq. 9.2.3}$$

Noting that $E_a = S_\Omega(2r_{bb'} + R_Y)^{0.5}$ and $E_b = S_\Omega(2R_C)^{0.5}$, where S_Ω is the ohm-normalized noise-spectral density (see Section 9.1.1.1) and setting $r_{bb'}$=0 for simplicity and also to show the fundamental limitations more clearly, we can write

$$E_{ni} = S_\Omega R_Y^{0.5} (1 + R_Y/2R_C)^{0.5} \qquad \text{Eq. 9.2.4}$$

The first part of this expression is simply the Johnson noise of R_Y. E_{ni} is increased in direct proportion to the second factor, requiring that $2R_C$ be much greater than R_Y. When $R_C = 2 R_Y$, the noise is increased by about 12 % or 1 dB. In our example, therefore, we might use R_C = 400Ω. But this raises a practical problem: if a value of I_Y = 23 mA were used to maintain acceptable distortion levels, the maximum voltage drop across the load resistors R_C would be nearly 15 V at full gain and full signal, requiring an inordinately high supply voltage. Further noise and distortion is generated by the base resistances and capacitances of the cascode transistors. At low gains, HF signal feedthrough occurs via the T-network formed by the $C_{je}/r_{bb'}/C_{jc}$ of these transistors, causing aberrations in the AC response.

In numerous ways this type of VCA fails to meet the exacting requirements of modern systems. Nevertheless, the approach remains appealing where some concessions to noise, distortion and gain-accuracy can be made. It is a simple cell for use in embedded applications, and provides the highest possible bandwidth for a given technology. Variable-gain amplifiers built along these lines are available for use up to about 1 GHz.

9.2.2 USING ANALOG MULTIPLIER/DIVIDERS TO BUILD VCAS

Analog multipliers and dividers can also be used in gain-control applications. These circuits are invariably based on the translinear principle, which exploits the precise proportionality of transconductance to collector current in a bipolar transistor.

Voltage-controlled amplifiers (VCAs) built from analog multipliers take one of two forms. In the first, the multiplier acts as a voltage-controlled attenuator ahead of a fixed-gain amplifier. This type of VCA is used in applications where not only a moderate maximum gain is needed but also a fairly high maximum loss. In the second, the variable attenuation is placed in the feedback path around an op amp, which in fact implements an analog divider. Analog dividers are more suitable for applications requiring high gains.

Products available from Analog Devices include the low-cost AD633, the high-accuracy AD734, and the high speed AD834 (useful to 500 MHz). These are four-quadrant multipliers. For gain-control applications, a two-quadrant circuit is more useful, such as the dual-channel AD539, which provides a signal bandwidth of about 60 MHz.

VCAs and multipliers based on the nonlinear properties of transistors inevitably exhibit various types of spurious nonlinearity, caused by non-ideal aspects of transistor behavior and the necessity for "open-loop" design. Nevertheless, with care in design and the use of distortion-nulling laser-trimming techniques in manufacturing, exceptionally low levels can be achieved. For example, the AD734 Multiplier/Divider exhibits nonlinearities of only 0.02 % from either the X- or Y-input, and provides a gain-bandwidth product of 200 MHz in its two-quadrant divider mode, implemented by direct control of the denominator voltage (rather than by putting a multiplier in a feedback path) over a 1000:1 range (10 mV to 10V).

Many practical circuits can be built using multipliers. We begin with a discussion of the AD539 and its use in conjunction with such transimpedance amplifiers as the AD844, because the AD539's basic structure is similar to that of the cell described in the last section, but the means have been included to provide accurate *linear* gain control, rather than the roughly-exponential, temperature-dependent gain control function of the basic cell. Figure 9.2.3 shows the essential pieces of the AD539. Note that there are two nominally identical channels whose gains are simultaneously controlled by a common voltage, V_X. These may be used separately, or in simple parallel to improve bandwidth and noise performance, or in a differential mode with appropriate support circuits.

SIMPLIFIED SCHEMATIC OF THE AD539 ANALOG MULTIPLIER

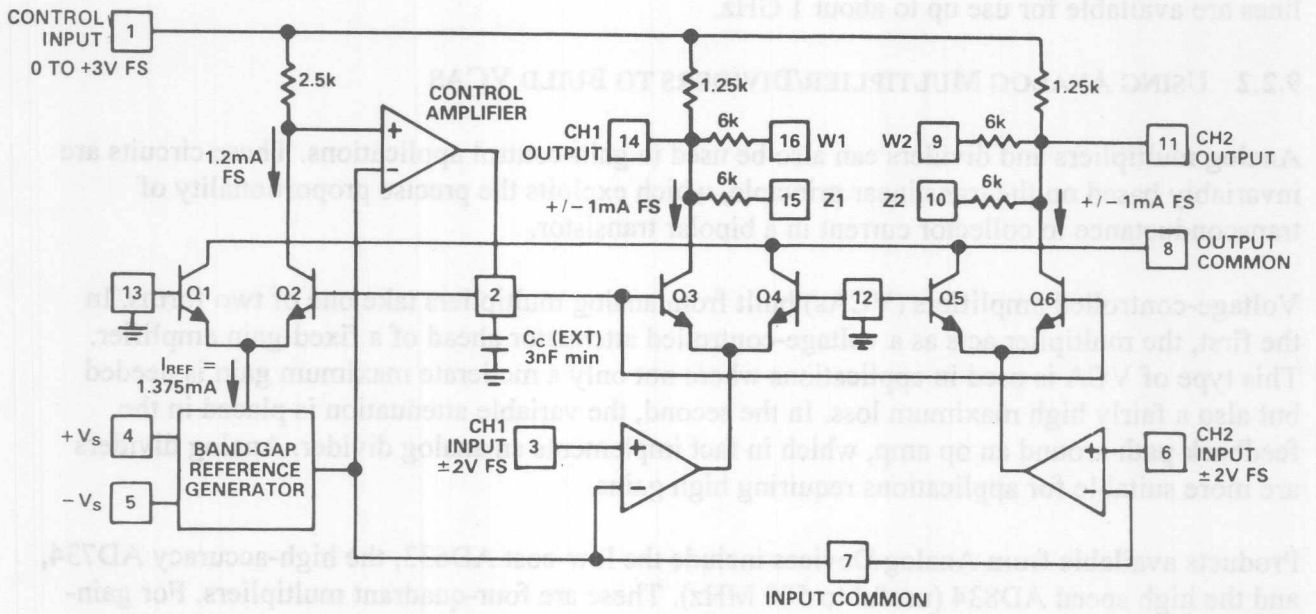


Figure 9.2.3

Two applications are shown. In Figure 9.2.4, the two sections of the AD539 are connected in simple parallel to double the output current. An AD844 transimpedance amplifier provides current-to-voltage conversion. The transfer function of this circuit is

$$V_W = \frac{-V_X V_Y}{2V} \qquad \text{Eq. 9.2.4}$$

where V_X is the gain-control voltage, a positive input from 0 V to 3.2 V , and V_Y is the signal input voltage, nominally ±2V full scale but capable of operating up to ±4.2 V. Connecting all four of the feedback resistors provided on the AD539 in parallel results in a feedback resistance of 1.5 kΩ, at which value the bandwidth of the AD844 is about 22 MHz, independent of V_X. The gain at V_X = 3.16V is +4 dB. Figure 9.2.5 shows the small signal response for a 50 dB gain-control range (V_X = +10 mV to +3.16 V). At small values of V_X, capacitive feedthrough on the PC board becomes troublesome, and careful layout techniques are needed.

In Figure 9.2.6, The AD827 dual high-speed op amp is used to provide output current-to-voltage conversion and the two sections of the AD539 are connected in series to provide a VCA with a square-law response. The transfer function of this circuit (measured at the reverse-terminated load) is

$$\frac{V_{OUT}}{V_{IN}} = \frac{-V_X^2}{8V^2} \qquad \text{Eq. 9.2.5}$$

Alternately, the two sections may be operated in parallel with linear gain control. The frequency response of this circuit is about 8 MHz using the AD827 op amp. The AD811 high-speed op amp may be substituted in these circuits for increased performance.

For wider bandwidths, the AD834 multiplier (Figure 9.2.7) may be used with a variety of op amps to build VCAs with small-signal bandwidths as high as 480 MHz. In each case, the op amp converts the differential-current outputs of the AD834 into a voltage.

A 20MHz VCA USING THE AD539 AND THE AD844

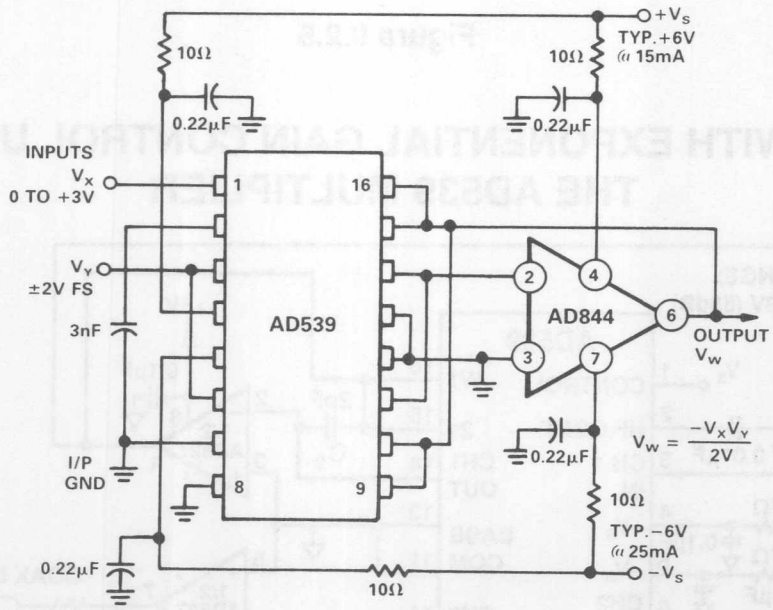


Figure 9.2.4

FREQUENCY RESPONSE OF THE 20MHz VCA

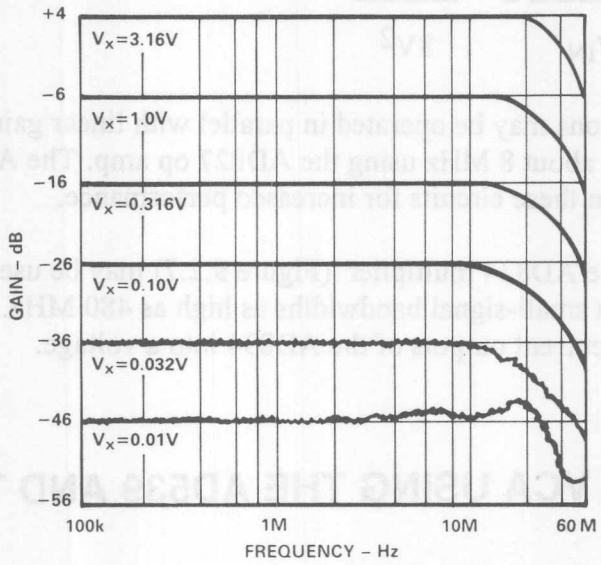
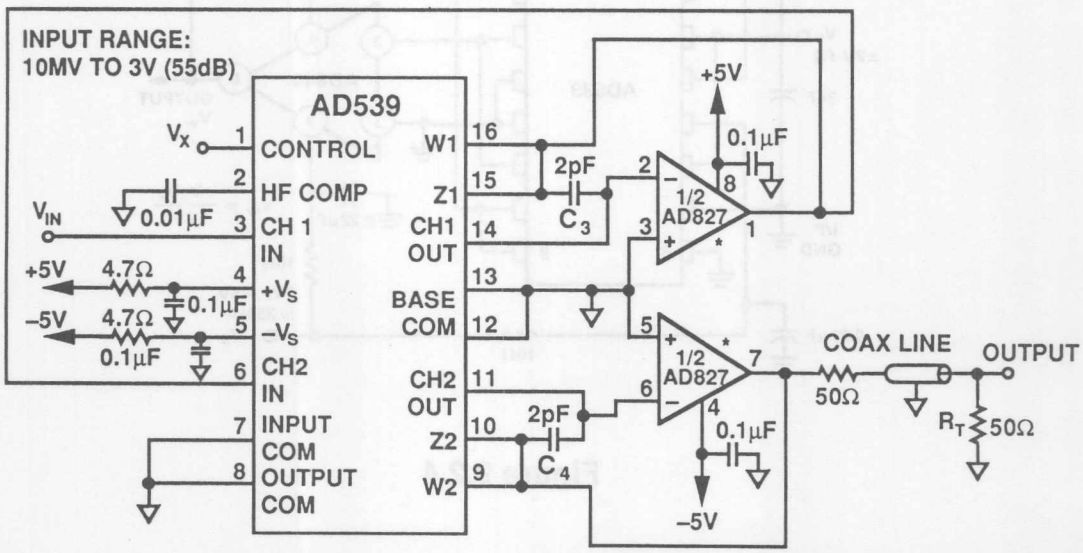


Figure 9.2.5

VCA WITH EXPONENTIAL GAIN CONTROL USING THE AD539 MULTIPLIER



*PINOUT SHOWN IS FOR MINI-DIP PACKAGE

V_{out} AT TERMINATION RESISTOR, $R_T = V_X^2 V_{in}/8V^2$

V_{out} AT PIN 7 OF AD827 = $V_X^2 V_{in}/4V^2$

Figure 9.2.6

SIMPLIFIED BLOCK DIAGRAM OF THE AD834 MULTIPLIER

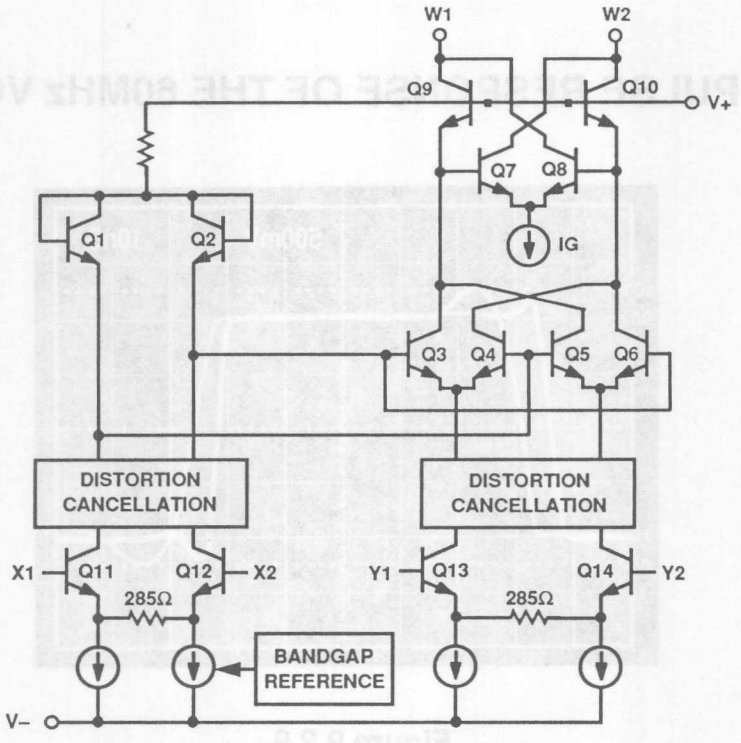


Figure 9.2.7

A 60MHz VCA USING THE AD834 AND THE AD5539

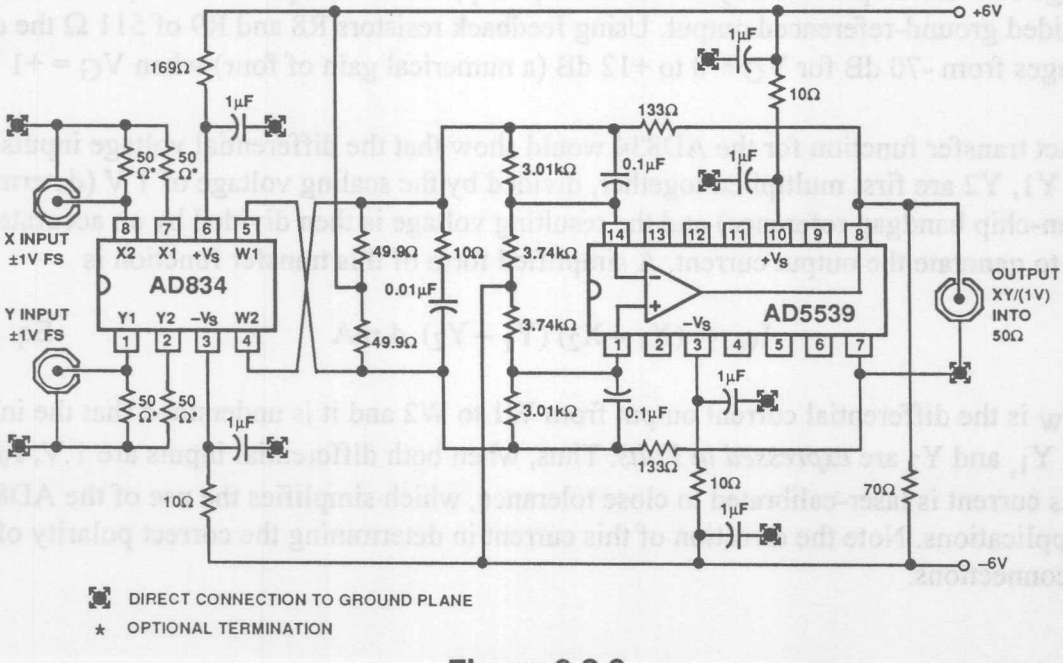


Figure 9.2.8

9

PULSE RESPONSE OF THE 60MHz VCA

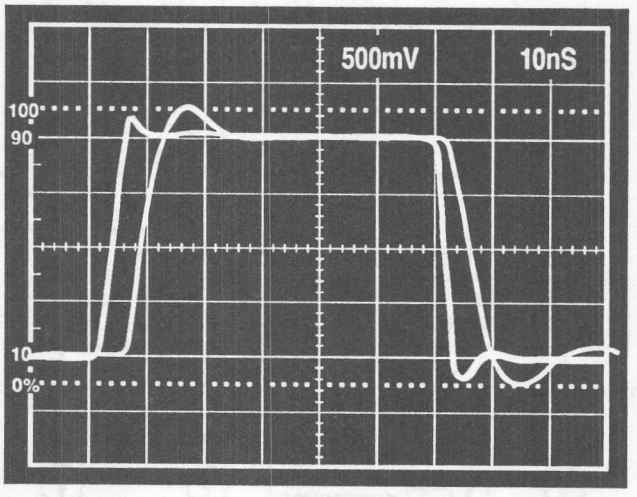


Figure 9.2.9

A 90MHz VCA is shown in Figure 9.2.10. The AD834's outputs are in the form of differential currents from a pair of open collectors, ensuring that the full bandwidth of the multiplier (which exceeds 500 MHz) is available. In this case, more moderate bandwidth is obtained using current-to-voltage conversion provided by the AD811 op amp, to realize a practical amplifier with a single-sided ground-referenced output. Using feedback resistors R8 and R9 of 511 Ω the overall gain ranges from -70 dB for $V_G \sim 0$ to +12 dB (a numerical gain of four) when $V_G = +1$ V.

The exact transfer function for the AD834 would show that the differential voltage inputs at X1, X2 and Y1, Y2 are first multiplied together, divided by the scaling voltage of 1 V (determined by the on-chip bandgap reference) and the resulting voltage is then divided by an accurate 250 Ω resistor to generate the output current. A simplified form of this transfer function is

$$I_W = (X_1 - X_2)(Y_1 - Y_2)\ 4\ \text{mA} \qquad \text{Eq. 9.2.6}$$

where I_W is the differential current output from W1 to W2 and it is understood that the inputs X_1, X_2, Y_1, and Y_2 are *expressed in Volts*. Thus, when both differential inputs are 1 V, I_W is 4 mA; this current is laser-calibrated to close tolerance, which simplifies the use of the AD834 in many applications. Note the direction of this current in determining the correct polarity of the output connections.

A 90MHz VCA USING THE AD834 AND THE AD811

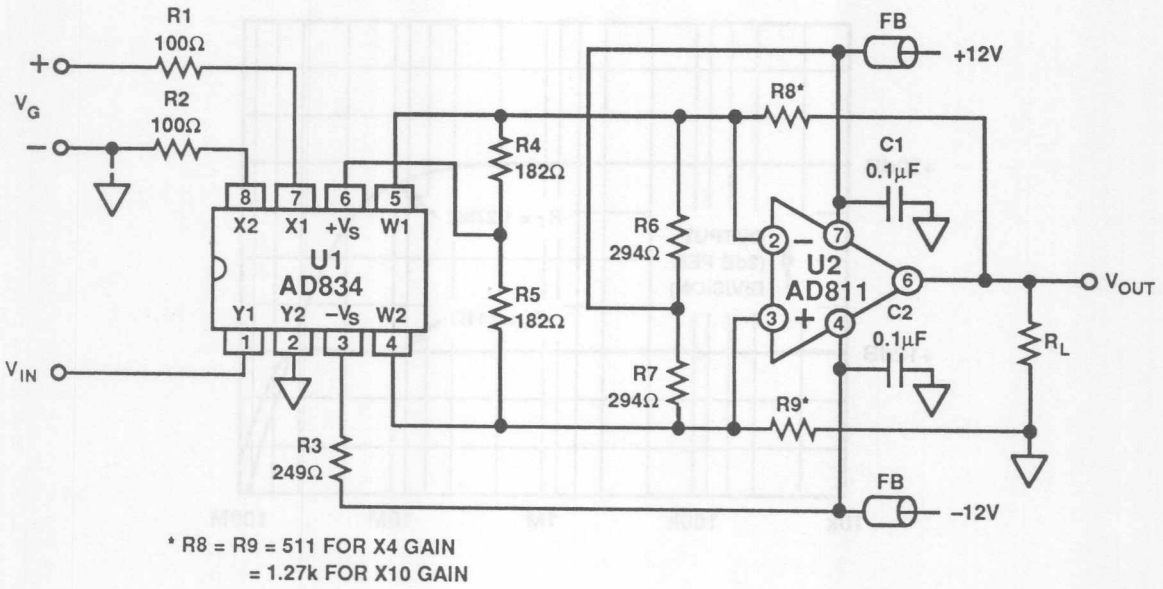


Figure 9.2.10

It is easy to show that the output of the AD811 is

$$V_{OUT} = 2 \times I_W \times R_F \qquad \text{Eq. 9.2.7}$$

where R_F is the feedback resistor. For $R_F = 500\ \Omega$ the overall transfer function of the VCA becomes

$$V_{OUT} = 4\,(X_1 - X_2)\,(Y_1 - Y_2) \qquad \text{Eq. 9.2.8}$$

which reduces to $V_{OUT} = 4\ V_G\ V_{IN}$ using the labeling conventions shown in Figure 9.2.10. As noted, the phase of the output reverses when V_G is negative. A slightly higher value of R_F compensates for the finite gain of the AD811.

The -3 dB bandwidth is 90 MHz (Figure 9.2.11) and independent of gain. The response can be maintained flat to within ±0.1 dB from DC to 40 MHz at full gain with the addition of a 0.3 pF capacitor across the feedback resistor R8. The circuit produces a full-scale output of ±4 V for a ±1 V input, and can drive a reverse-terminated load of 50 Ω or 75 Ω to ±2 V. Figure 9.2.12 shows the typical pulse response.

FREQUENCY RESPONSE OF THE 90MHz VCA

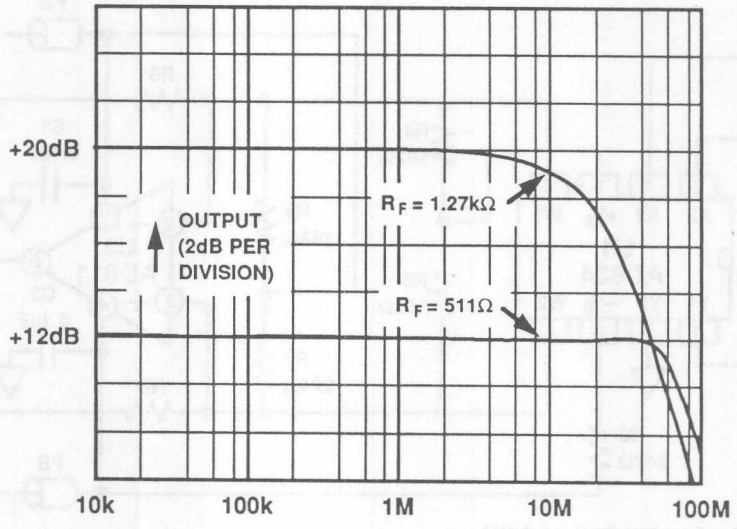


Figure 9.2.11

PULSE RESPONSE OF THE 90MHz VCA

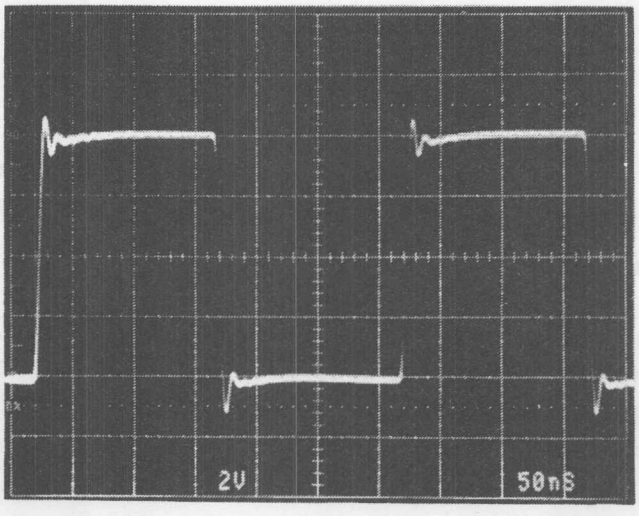


Figure 9.2.12

The gain can be increased to 20 dB (10) by increasing the values of R8 and R9 to 1.27 kΩ; this also reduces the -3 dB bandwidth to about 25 MHz and produces a maximum output voltage of ±9 V using ±12 V supplies. It is not necessary to alter the values of R6 and R7 for the high-gain version of the amplifier, although an optimized design would increase these slightly to restore the common-mode voltage at the input of the AD811 to +5 V.

Figure 9.2.13 shows a DC to 480 MHz VCA using a PNP transistor as a common base stage or cascode. The transistor's base is tied to +5 V, ensuring that the emitter potential stays at 5.7 V and provides a steady voltage drop across the emitter resistors. In this circuit, the AD9617 op amp's inputs are 350 mV below ground and within their common mode range.

A 480MHz VCA USING THE AD834 AND THE AD9617

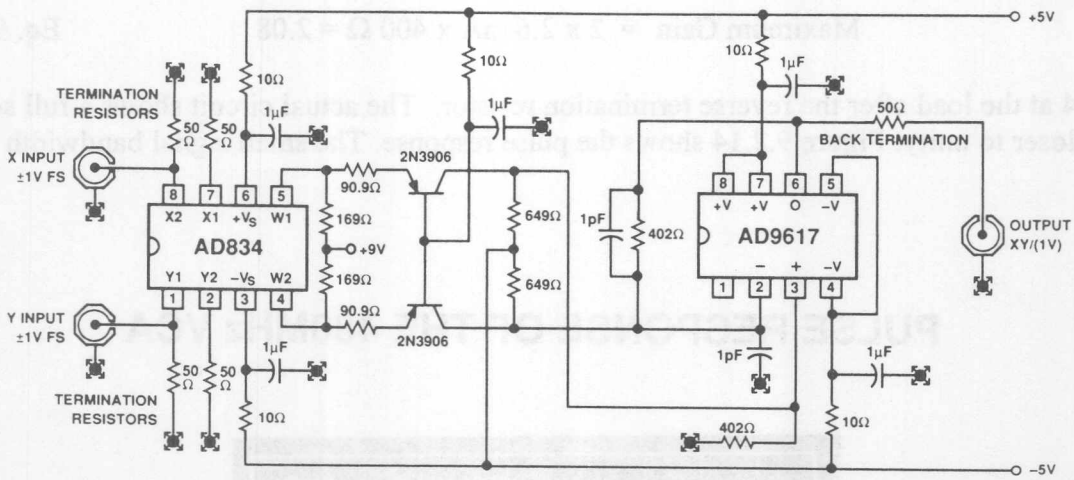


Figure 9.2.13

The bandwidth of a transistor configured as a cascode is approximately the unity gain frequency (f_t) of the transistor, provided that the user does not create any spurious poles. Choosing emitter resistors which are too large for the transistor's parasitic emitter-base capacitance or collector resistors too large for the transistor's parasitic collector-base capacitance will create unwanted poles that lower the frequency response of the circuit.

Another potential pitfall when using the active PNP level shifter is oscillations at the cascode's emitter. The input impedance of a bipolar junction transistor's emitter is inductive at frequencies approaching f_t, while the AD834's output is capacitive. These conditions can lead to oscillations.

To prevent such oscillations, the PNP's emitters in Figure 9.2.13 have been isolated from the AD834's output by the 90.9Ω resistors. These dampen any tendency to oscillate and provide signal attenuation. The 2N3906s and their accompanying network has proven to provide wideband level shifting without resonance or oscillation. Care must be taken when specifying alternative transistors.

The signal currents at the 2N3906s' collectors are now fed to an AD9617 op amp in a differential current-to-voltage converter configuration. This configuration is similar to the op-amp driven current-to-voltage converter that typically follows a current-output multiplying digital-to-analog converter.

The AD9617's inputs are connected to the collectors of the 2N3906s. The op amp creates a virtual short between the input nodes, forcing all the signal current to flow in the feedback paths. The differential transresistance of the converter is 400 Ω. The full scale gain of the circuit (X=Y=1V) at the AD9617's output is calculated as:

$$\text{Maximum Gain} = 2 \times 2.6\ \text{mA} \times 400\ \Omega = 2.08 \qquad \text{Eq. 9.2.9}$$

or 1.04 at the load after the reverse termination resistor. The actual circuit shows a full scale gain closer to unity. Figure 9.2.14 shows the pulse response. The small signal bandwidth is 480 MHz.

PULSE RESPONSE OF THE 480MHz VCA

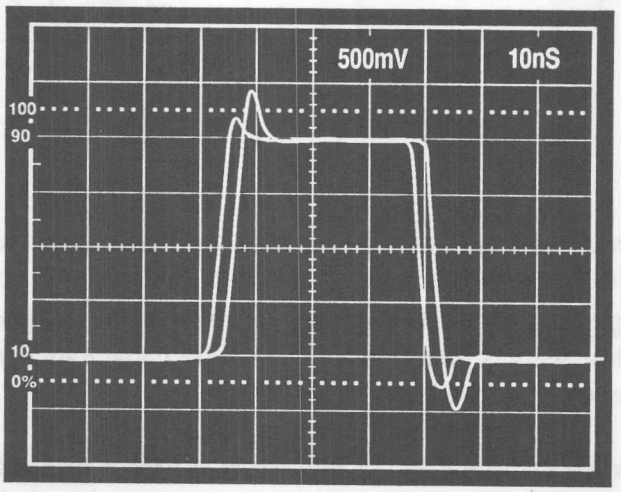


Figure 9.2.14

9.2.2.1 VIDEO KEYER

The AD834 also lends itself to a special form of a VCA called a video keyer. Keying is the term used in reference to blending two or more video sources under the control of a further signal or signals to create such special effects as dissolves and overlays. The circuit described here is a two-input keyer, with video inputs V_A and V_B, and a control input V_G.

The output at the load is given by

$$V_{OUT} = G\,V_A + (1-G)\,V_B \qquad \text{Eq. 9.2.10}$$

where G is a dimensionless variable (actually, just the gain of the "A" signal path) that ranges from 0 when $V_G = 0$, to 1 when $V_G = +1$ V. Thus, V_{OUT} varies continuously between V_A and V_B as G varies from 0 to 1.

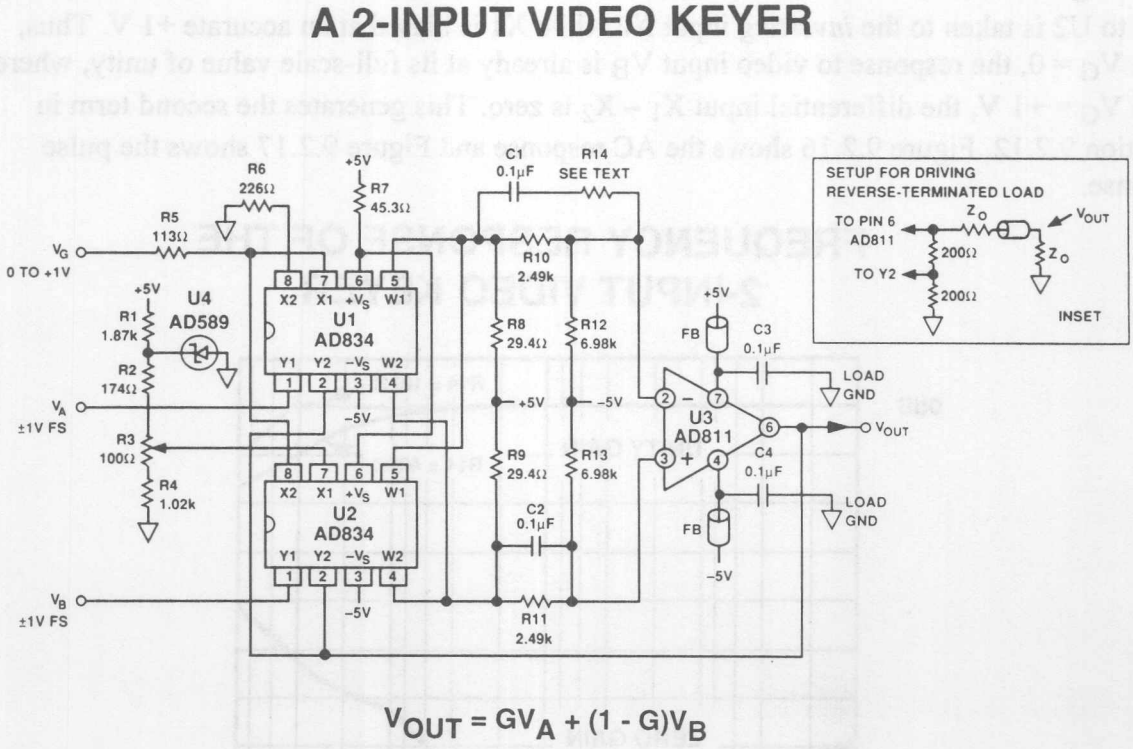


Figure 9.2.15

Figure 9.2.15 shows the circuit. Note first that V_{OUT} is returned to the inverting inputs Y2 of the multipliers and that their outputs are added. The sum is forced to zero by the assumed high open-loop gain of the op amp. Multiplier U1 produces an output $G(V_A - V_{OUT})$, while U2 produces an output $(1\text{-}G)(V_B\text{-}V_{OUT})$, where G is $V_G/(1\text{ V})$ and ranges from 0 to 1. Therefore, the complete system is described by the limiting condition

$$G(V_A - V_{OUT}) + (1-G)(V_B - V_{OUT}) \rightarrow 0 \qquad \text{Eq. 9.2.11}$$

which requires that

$$V_{OUT} = GV_A + (1-G)V_B \qquad \text{Eq. 9.2.12}$$

exactly as required for a two-input keyer. The summation of the differential current-mode outputs of the two AD834s is achieved by connecting together their respective W1 and W2 nodes. The resulting signal — essentially the loop error represented by the left-hand-side of Equation 9.2.11 — is forced to zero by the high gain of an AD811 op amp.

The operation is straightforward. Consider first the signal path through U1, which handles video input V_A. Its gain is zero when $V_G = 0$ and the scaling we have chosen ensures that it is unity when $V_G = +1$ V; this takes care of the first term in Equation 9.2.12. On the other hand, the V_G input to U2 is taken to the *inverting* input X2 while X1 is biased at an accurate +1 V. Thus, when $V_G = 0$, the response to video input V_B is already at its full-scale value of unity, whereas when $V_G = +1$ V, the differential input $X_1 - X_2$ is zero. This generates the second term in Equation 9.2.12. Figure 9.2.16 shows the AC response and Figure 9.2.17 shows the pulse response.

FREQUENCY RESPONSE OF THE 2-INPUT VIDEO KEYER

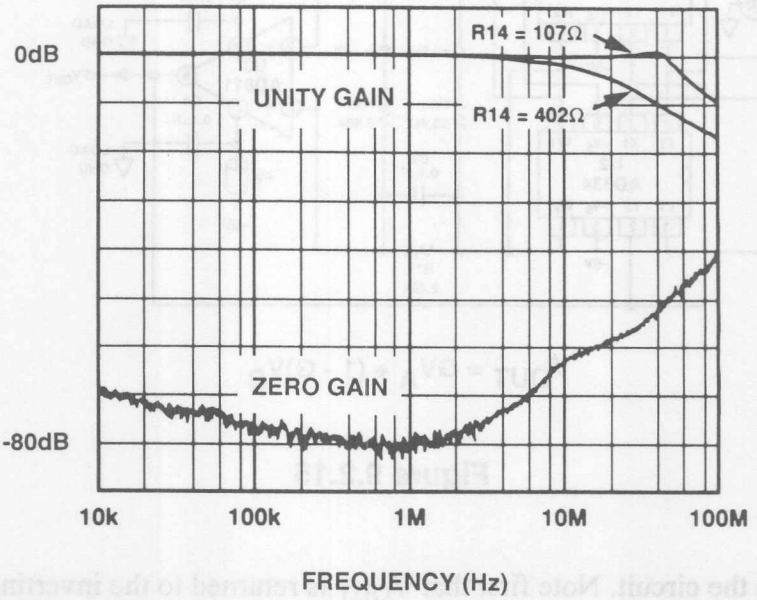
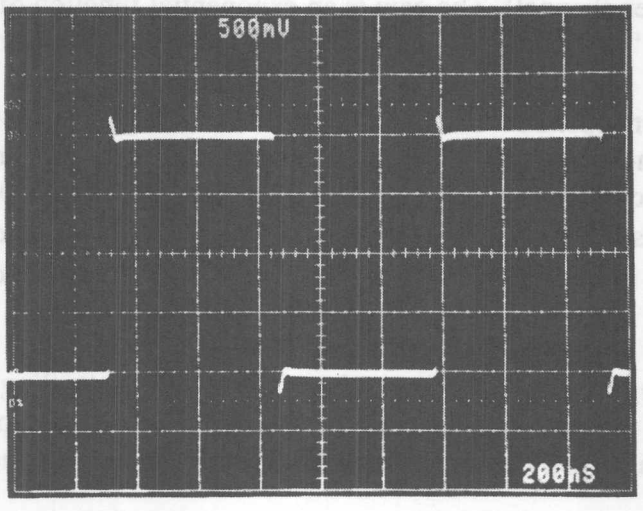


Figure 9.2.16

PULSE RESPONSE OF THE 2-INPUT VIDEO KEYER



R14 = 107Ω

Figure 9.2.17

To generate the 1 V DC needed for the "1–G" term, an AD589 reference supplies 1.225V±25mV to a voltage divider consisting of resistors R2 through R4. Potentiometer R3 should be adjusted to provide +1 V at the X1 input.

The bias currents required at the output of the multipliers are provided by R8 and R9. A DC-level-shifting network comprising R10/R12 and R11/R13 ensures that the input nodes of the AD811 are positioned within an acceptable common-mode range for this IC. At high frequencies, C1 and C2 bypass R10 and R11, respectively.

9.2.3 THE X-AMP

Two new dual-channel voltage-controlled amplifiers, the AD600 and AD602, have recently been introduced by Analog Devices. They differ from the multipliers just discussed in that the signal passes only through circuits that are linear: specifically a resistive ladder attenuator and a fixed-gain amplifier that uses negative feedback to enhance linearity. The term "X-AMP", coined to apply to this proprietary architecture, is a reference to the *exponential* gain function which they provide.

The X-AMP was developed for medical ultrasound applications. It provides the unusual combination of low noise (1.4 nV/√Hz), good signal-handling capabilities (1 V RMS at the input, 2 V RMS at the output), a constant 3 dB bandwidth of DC to 35 MHz, constant phase and group-delay characteristics, low distortion (–60 dBc to 10 MHz) and low power consumption (125 mW maximum per channel). The gain is an exponential function of the control voltage, V_G, which means it is "linear in dB", calibrated to 32 dB/Volt (31.25 mV/dB).

The two channels are independent and may be cascaded for a gain range of up to 80 dB in one package. Separate high-impedance, differential gain-control interfaces are provided. In the AD600 the gain for each section is 0 dB for V_G = –625 mV, 20 dB for 0 V, and 40 dB for +625 mV. When V_G exceeds these values, the minimum gain becomes –1.07 dB and the maximum is 41.07 dB. The AD602 is similar, except that each VCA provides a gain of –11.07 dB to 31.07 dB.

These precise over-range values will later be important in understanding the gain-sequencing scheme used in one of the circuits presented. The sections can also be operated in parallel, to achieve a noise spectral density of 1 nV/√Hz with no compromise in other aspect of performance.

As we will show, by adding an RMS converter to two series-connected VCA sections (a single AD600), a circuit can be built which provides both accurate automatic gain control (AGC) and an accurately-calibrated output voltage proportional to the decibel value of the RMS input over an 80 dB range.

9.2.3.1 X-AMP BASICS

The key idea behind these amplifiers is the use of a low-noise *fixed-gain* amplifier, which employs negative feedback to achieve low distortion and high gain-accuracy, preceded by a broadband *passive* R-2R attenuator network.

The new technique allows the attenuator to be *continuously* interpolated, thus providing the smooth decibel-scaled gain function. The fixed-gain amplifier (Figure 9.2.18) uses classical negative feedback to achieve accurate gain. Since it never has to cope with large input signals it can be optimized for low noise and low distortion. The overall bandwidth is constant. The resulting amplifier comes very close to the ideal VCA.

When a correctly-terminated regular ladder network is used for this attenuator, a "linear-dB" control law is *automatically guaranteed*, because the signals between adjacent tap-points bear a constant ratio, diminishing in an exponential fashion from input to termination. Using the familiar R-2R network the voltage ratio from left to right is exactly two, or about 6.02 dB. Using an R-R network, the attenuation would be 8.36 dB. Obviously, any desired ratio can be used; in practice, the use of integer resistor multiples ensures excellent attenuation accuracy without the need for trimming.

THE STARTING POINT IN THE SYNTHESIS OF THE X-AMP

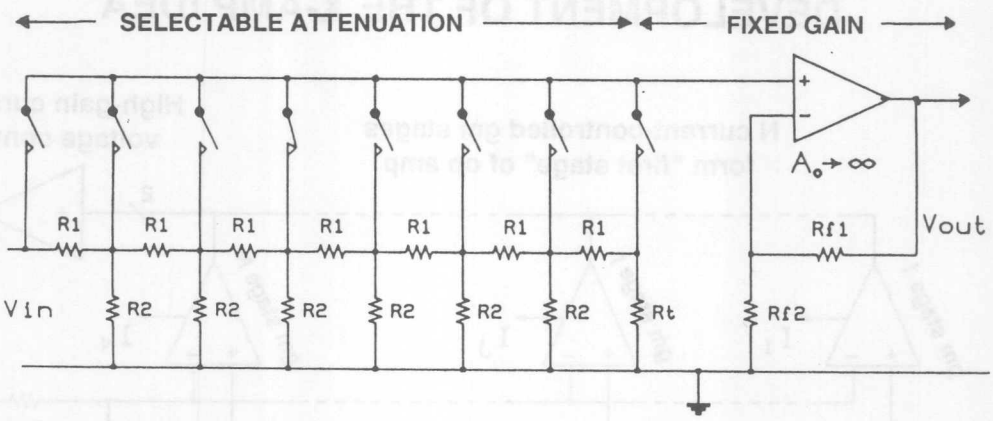


Figure 9.2.18

A seven-section R-2R attenuator provides a total attenuation of 42.14 dB (corresponding to an overall voltage ratio of 128). For the moment, assume that the taps on this attenuator are selected by a simple rotary switch, to provide eight discrete values of gain, separated by constant decibel steps of 6.02 dB. When a large input is to be handled, the full attenuation is used: a 1V input is reduced to 7.8 mV, easily handled by the main amplifier stage.

On the other hand, for small signals, the amplifier's input can be *directly* connected to the source, with essentially no extra thermal noise. In this condition, the noise generation mechanisms can be reduced to those fundamentally attributable to shot noise in the input stage of the amplifier and the combined Johnson noise of the source and feedback resistors. This is a distinct and unique advantage of the technique.

In an IC realization, the rotary switch might be replaced by eight digitally-selected MOS transistors. However, these would introduce significant amounts of extra noise due to their channel resistance, unless they were made very large, in which case parasitic capacitances would cause very undesirable feedthrough effects at high frequencies. They would still only provide discrete gain steps; any attempt to increase the resolution by using more attenuator sections with closer tap points, adding correspondingly more switches, would only exacerbate the feedthrough problem.

The key step in the development of the X-AMP concept is to replace the switches with controllable *gm* stages, as shown in Figure 9.2.19. These are bipolar differential pairs having a set of tail currents that are in the form of overlapping Gaussian sections. In this way, the effective input of the amplifier can be moved *continuously* from the source to the last tap on the attenuator. By correctly proportioning the interpolation currents, excellent gain linearity can be achieved: for the AD600 and AD602 it is about ±0.1 dB. Further development of the X-AMP showing the bipolar differential pairs is shown in Figure 9.2.20.

DEVELOPMENT OF THE X-AMP IDEA

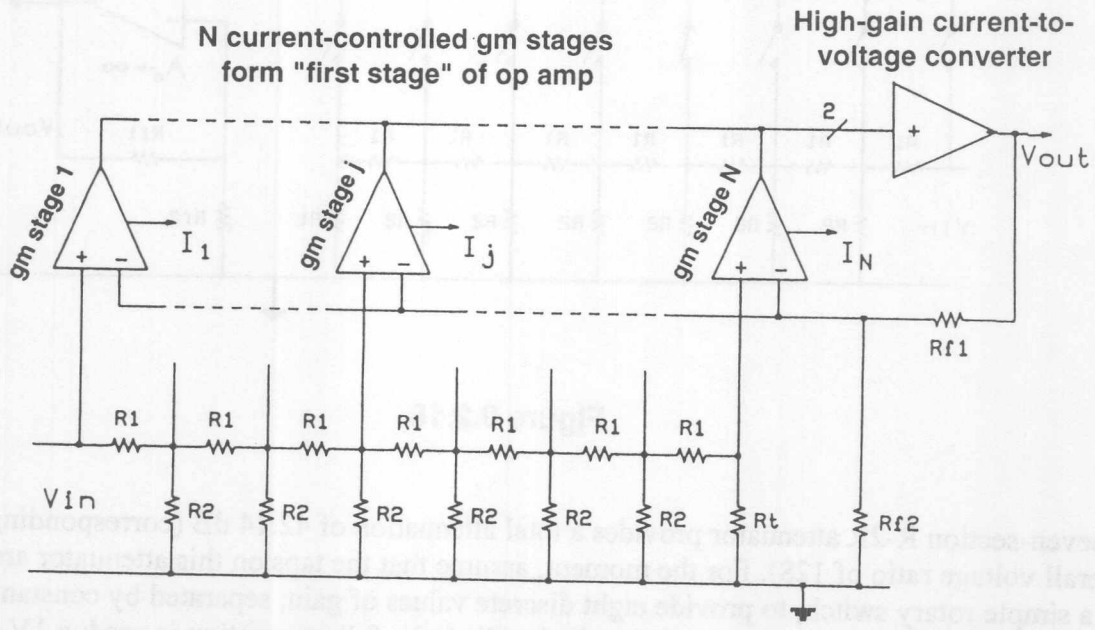


Figure 9.2.19

FURTHER DEVELOPMENT OF THE X-AMP IDEA

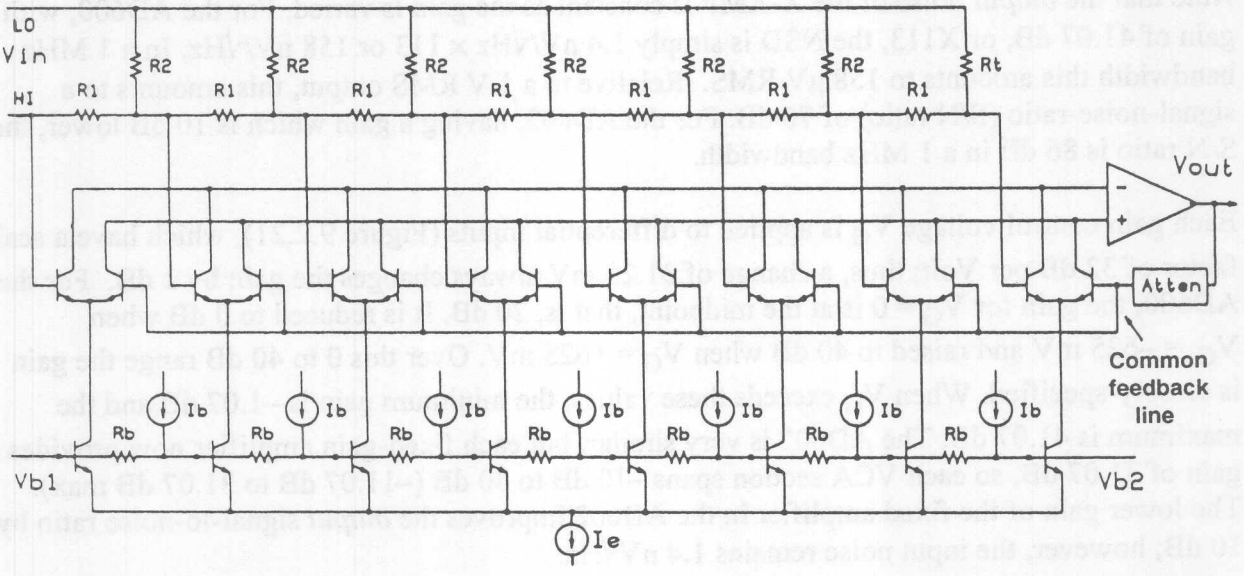


Figure 9.2.20

The fundamental noise floor for a differential bipolar transconductance (*gm*) stage, limited by shot-noise, is

$$S_I = \frac{0.926\text{nV} / \sqrt{\text{Hz}}}{\sqrt{I_T}} \qquad \text{Eq. 9.2.13}$$

at 300 K (27°C) where I_T is the differential amplifier "tail" current expressed in milliamps. In the AD600 and AD602, I_T is 2.4 mA, producing a theoretical noise-spectral-density (NSD) of 0.6 nV/√Hz. In addition, there will be Johnson noise in the resistances associated with the source, input stage and attenuators; at 300 K this evaluates to

$$S_\Omega = 0.129\sqrt{R_T} \quad \text{nV}/\sqrt{\text{Hz}}, \qquad \text{Eq. 9.2.14}$$

where R_T is the total ohmic resistance associated with the input system, that is, the sum of the source or tap resistance, the feedback resistor R_{F1} and the two base resistances of the input

transistors, $r_{bb'}$. For the AD600 and AD602, R_T is about 80 Ω, producing a NSD of 1.15nV/√Hz. The RMS sum of the shot noise S_I and Johnson noise S_Ω is 1.3 nV/√Hz. Some second-stage noise contributions and base-current noise raise this to 1.4 nV/√Hz.

Note that the *output* noise of the X-AMP is constant as the gain is varied. For the AD600, with a gain of 41.07 dB, or X113, the NSD is simply 1.4 nV/√Hz × 113 or 158 nV/√Hz. In a 1 MHz bandwidth this amounts to 158 μV RMS. Relative to a 1 V RMS output, this amounts to a signal-noise-ratio (S/N ratio) of 76 dB. For the AD602, having a gain which is 10 dB lower, the S/N ratio is 86 dB in a 1 MHz bandwidth.

Each gain control voltage V_G is applied to differential inputs (Figure 9.2.21), which have a scale factor of 32 dB per Volt; thus, a change of 31.25 mV always changes the gain by 1 dB. For the AD600, the gain for $V_G = 0$ is at the midpoint, that is, 20 dB. It is reduced to 0 dB when $V_G = -625$ mV and raised to 40 dB when $V_G = +625$ mV. Over this 0 to 40 dB range the gain is closely-specified. When V_G exceeds these values, the minimum gain is –1.07 dB and the maximum is 41.07 dB. The AD602 is very similar, but each fixed-gain amplifier now provides a gain of 31.07 dB, so each VCA section spans –10 dB to 30 dB (–11.07 dB to 31.07 dB max). The lower gain of the fixed amplifier in the AD602 improves the *output* signal-to-noise ratio by 10 dB; however, the input noise remains 1.4 nV√Hz.

BLOCK DIAGRAM OF THE AD600 AND AD602

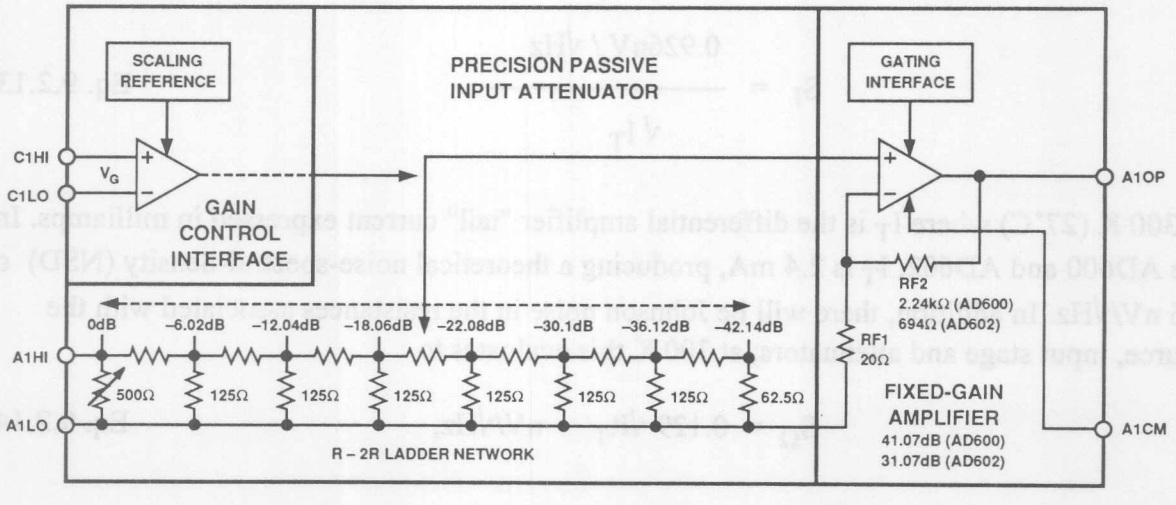


Figure 9.2.21

Since the AD600 and AD602 each provide two independent VCAs, A1 and A2, gain ranges of over 80 dB can be achieved. In the simplest case, their individual gain-control inputs are connected in parallel, and the gain varies by 64 dB per Volt. However, in order to optimize the signal-to-noise performance over the entire gain range, a sequential arrangement of the A1 and A2 gain control voltages can be used, in which the gain of A1 is first varied over its 40 dB range, while A2 operates at minimum gain (thus, with the lowest coupling of the output noise of A1); thereafter, only the gain of A2 is varied to provide the second 40 dB segment of the overall gain range. This "sequential-gain" function can be achieved by including an offset voltage (corresponding to about 40 dB) between the A1 and A2 gain-control inputs. We shall later show another modification to the gain-control function, using a small control offsets (3 dB in the case of two cascaded VCAs, 2 dB in the case of three sections) to achieve exceptionally accurate gain and excellent logarithmic linearity. Figure 9.2.22 lists the highlights of the X-AMP.

HIGHLIGHTS OF THE X-AMP

- Precise Decibel-Scaled Gain Control
- Accurate Absolute Gain Calibration
- Low Noise (1.4nV/ √Hz)
- Constant Bandwidth (dc to 35MHz)
- Stable Group Delay (±2ns over gain range)
- Low Distortion -- Uses Negative Feedback
- Low Power (125mW per channel maximum)

Figure 9.2.22

9.2.4 APPLYING THE X-AMP

The X-AMP is simple to apply. However, as for all wideband, high-gain amplifiers, careful PC board layout and adequate supply decoupling are important. This is particularly true when the amplifier sections are used in cascade. To simplify the following explanation, references to pin labels will be for amplifier A1, the connections for which are shown in Figure 9.2.23.

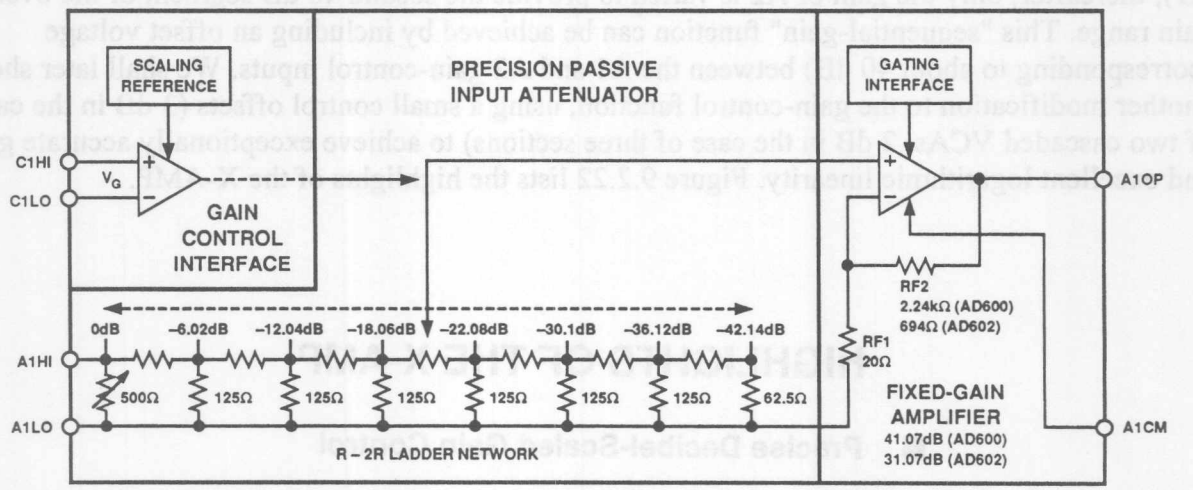


Figure 9.2.23

The input is applied to pins A1HI and A1LO, and may have a maximum value of 1 V RMS (±1.4 V peak), ultimately limited by the common-mode range of the eight g_m stages. The resistance from A1HI to A1LO is trimmed to 100 Ω ± 2 Ω, which allows the introduction of accurate external attenuation by the simple expedient of adding a series resistor. However, it is important to note that these pins do *not* form a fully differential input pair, as a glance at Figure 9.2.23 will show. In fact, A1LO must be always be very *well grounded*, since it carries not only the current in the ladder network but also the current in the feedback resistor RF1, which is about five times lower. Thus, the resistance which would be seen looking into A1LO if A1HI were grounded would be 100 Ω in parallel with 20 Ω, or 16.7 Ω. (Internally, A1LO is connected by multiple bond-wires to lower the impedance in this path.)

The output appears at pin A1OP but is referenced to an independent output ground, A1CM ("common"). A small common-mode voltage can exist between A1LO and A1CM, and this voltage will be rejected by the amplifier. (The details of the circuitry providing this feature are not shown explicitly in Figure 9.2.23.). Thus, if we denote the numerical gain of the amplifier by G, the output can be expressed as

$$V_{A1OP} = G\,(V_{A1HI} - V_{A1LO}) + V_{A1CM} \qquad \text{Eq. 9.2.15}$$

For the AD600, G is accurately controlled from X1 to X100 while for the AD602 the specified range is X0.316 to X31.6.

The peak output voltage into resistive loads greater than 500 Ω, such as a flash A/D converter, is specified as ±3 V when using the recommended ±5 V supplies. For a 200 Ω load, an output of ±1.5V can be supported while still meeting the distortion specifications. Even lower load resistances can be driven if an external pull-down resistor is added between the output and the negative supply; for example, a 1 kΩ resistor would provide an extra current of 5 mA. Considerable load current can occur at high frequencies when the load is purely capacitive; in these cases, a small series resistor (5 to 50 Ω) will improve the overall stability, often with little loss of bandwidth. In most cases, the output will be AC-coupled to the load.

The gain is controlled by the voltage V_G applied to the fully-differential pins C1HI and C1LO, which exhibit an input resistance of about 15 MΩ in shunt with 2 pF. This high resistance makes it an easy matter to control a large number of X-AMPs operating in parallel, as in the ultrasound application. Thus,

$$V_G = V_{C1HI} - V_{C1LO} \qquad \text{Eq. 9.2.16}$$

and has a maximum specified range of ±625 mV.

The decibel gain is simply

$$G_{dB} = 32\ V_G + 20 \quad \text{for the AD600} \qquad \text{Eq. 9.2.17}$$

or

$$G_{dB} = 32\ V_G + 10 \quad \text{for the AD602} \qquad \text{Eq. 9.2.18}$$

where V_G is in Volts.

The differential gain-control interface allows a variety of control schemes to be employed. In the simplest example, the gain can be made to either increase or decrease with a positive voltage, depending on whether C1HI or C1LO is connected to the control voltage. Because these inputs are essentially non-loading, it is a simple matter to provide an offset voltage to shift the control voltage to a particular range, using a resistor network across the supply. Thus, if the control input is connected to C1HI, while C1LO is offset to +625 mV, the control range now runs from 0 to +1.25 V.

If A1 and A2 are used in cascade and the same gain voltage is applied to both control interfaces in simple parallel, the gain factor is doubled to 64 dB/V, because the gains of both amplifiers vary simultaneously. However, if one of the control interfaces is offset by the appropriate

voltage we can arrange for the gain of A1 and A2 to vary sequentially, which keeps the scaling at 32 dB/V but now requires 2.5 V for the full 80 dB range, conveniently supplied by an inexpensive 8-bit DAC, such as the AD558. An example is shown in the next section.

The AD600 and AD602 also provide a TTL-compatible gating feature. When the pin GAT1 (or GAT2) is HI, the channel is shut down, and the output is set to within a few millivolts of the voltage on A1CM (or A2CM) with an attendant large reduction in output noise. This feature is useful in multi-channel synthetic-aperture or beam-forming systems, where channels having a weighting below some threshold can be switched off and their noise contribution to the summed signal thus minimized.

The gain-control range of the last circuit can be extended to 100 dB by using a further VCA section. Fully–tested implementations are shown later; in both, precise gain offsets are used to achieve either (1) a very high gain linearity of ±0.1 dB over the full 100 dB range, or (2) the optimal signal-to-noise ratio at any gain.

9.2.5 A LOW-NOISE AGC AMPLIFIER

Figure 9.2.24 provides an example of the ease with which the AD600 can be connected as an AGC amplifier. A1 and A2 are cascaded, with 6 dB of attenuation introduced by the 100 Ω resistor R1, while a time- constant of 5 ns is formed by C1 and the 50 Ω of net resistance at the input of A2. This introduces a single-pole low-pass filter at about 32 MHz,to ensure stability at maximum gain It also lowers the overall gain range to -6dB to 74dB. C1 blocks the small DC offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high-pass corner at about 8 kHz, eliminating low-frequency noise and spurious signals which may be present at the input.

A half-wave detector is used, based on Q1 and R2. The current into capacitor C2 is just the difference between the current provided by the AD590 (300 μA at 300 K, 27 °C) and the collector current of Q1. In turn, the control voltage V_G is the time-integral of this *error* current. In order for V_G (and thus the gain) to remain stable, the rectified current in Q1 must, on average, exactly balance the current in the AD590. If the output of A2 is too small to do this, V_G will ramp up, causing the gain to increase, until Q1 conducts sufficiently.

First consider the particular case where *R2 is zero* and the output voltage V_{OUT} is a squarewave at, say, 100 kHz, that is, well above the corner frequency of the control loop. During the time V_{OUT} is negative, Q1 conducts; when V_{OUT} is positive, it is cut off. Since the *average* collector current is forced to be 300 μA, and the squarewave has a duty-cycle of 1:1, the current when conducting must be 600 μA. With R2 omitted, the peak value of V_{OUT} is forced to be just the V_{BE} of Q1 at 600 μA, typically about 700 mV, or $2V_{BE}$ peak-to-peak. This voltage, hence the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically –1.7 mV/°C. While this may not be troublesome in some applications, the addition of R2 will render the output stable with temperature.

A SIMPLE BUT ACCURATE AGC AMPLIFIER

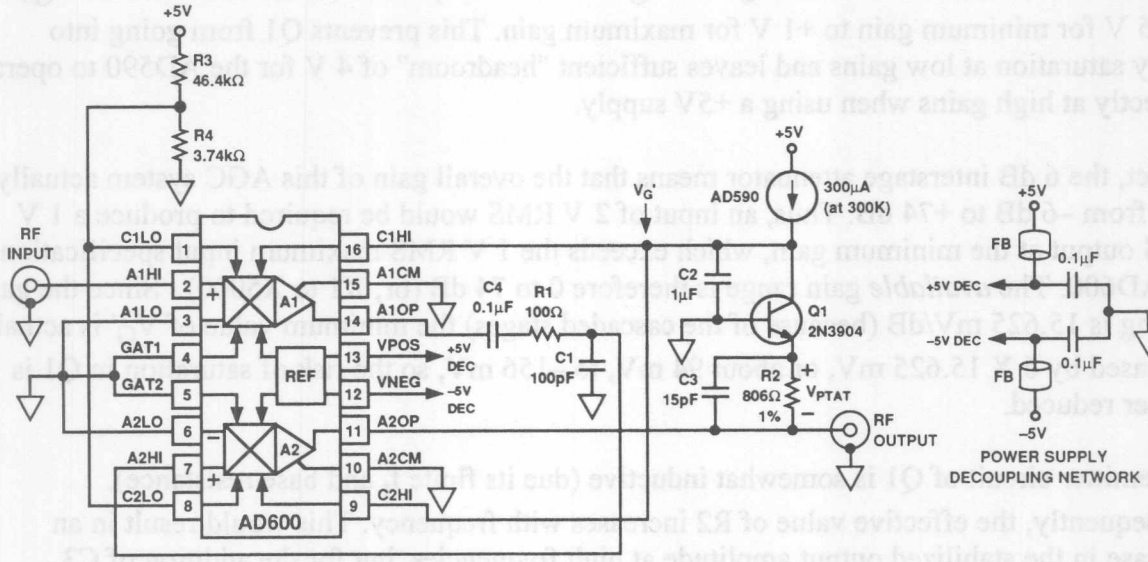


Figure 9.2.24

To understand this, first note that the current in the AD590 is proportional to absolute temperature (PTAT). (The AD590 is a temperature-dependent current source with a 1 μA/K temperature coefficient. At T = 300 K, its output is 300 μA.) For the moment, continue to assume that the signal is a squarewave. When Q1 is conducting, V_{OUT} is now the *sum* of V_{BE} and a voltage which is PTAT and which can be chosen to have an equal but opposite TC to that of the V_{BE}. This is actually nothing more than an application of the "bandgap voltage reference" principle. When R2 is chosen such that the sum of the voltage across it and the V_{BE} of Q1 is close to the bandgap voltage of about 1.2 V, V_{OUT} will be stable over a wide range of temperatures, provided, of course, that Q1 and the AD590 share the same thermal environment.

Since the average emitter current is 600 μA during each half-cycle of the squarewave a resistor of 833 Ω would add a PTAT voltage of 500 mV at 300 K, increasing by 1.66 mV/°C. In practice, the optimum value will depend on the type of transistor used, and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the inexpensive 2N3904 and sinewave signals, the recommended value is 806 Ω. This resistor also serves to lower the peak current in Q1 when more typical signals (usually, sinusoidal) are involved, and the 200-Hz LP filter it forms with C2 helps to minimize distortion due to ripple in V_G. Note that the output amplitude under sinewave conditions will be higher than for a squarewave, since the average value of the current *for an ideal rectifier* would be 0.637 times as large, causing the output

amplitude to be 1.88 (=1.2/0.637) V, or 1.33 V RMS. In practice, the somewhat non-ideal rectifier results in the sinewave output being regulated to about 1.275 V RMS.

An offset of +375 mV is applied to the inverting gain-control inputs C1LO and C2LO. Thus the nominal –625 mV to +625 mV range for V_G is translated upwards (at the node labeled V_G') to –0.25 V for minimum gain to +1 V for maximum gain. This prevents Q1 from going into heavy saturation at low gains and leaves sufficient "headroom" of 4 V for the AD590 to operate correctly at high gains when using a +5V supply.

In fact, the 6 dB interstage attenuator means that the overall gain of this AGC system actually runs from –6 dB to +74 dB. Thus, an input of 2 V RMS would be required to produce a 1 V RMS output at the minimum gain, which exceeds the 1 V RMS maximum input specification of the AD600. The *available* gain range is therefore 0 to 74 dB (or, X1 to X5000). Since the gain scaling is 15.625 mV/dB (because of the cascaded stages) the minimum value of V_G' is actually increased by 6 X 15.625 mV, or about 94 mV, to –156 mV, so the risk of saturation in Q1 is further reduced.

The emitter circuit of Q1 is somewhat inductive (due its finite f_t and base resistance). Consequently, the effective value of R2 increases with frequency. This would result in an increase in the stabilized output amplitude at high frequencies, but for the addition of C3, determined experimentally to be 15 pF for the 2N3904 for maximum response flatness. Alternatively, a faster transistor can be used here to reduce HF peaking. Figure 9.2.25 shows the AC response at the stabilized output level of about 1.3 V RMS. Figure 9.2.26 demonstrates the output stabilization for sinewave inputs of 1 mV to 1V RMS at frequencies of 100 kHz, 1 MHz and 10 MHz.

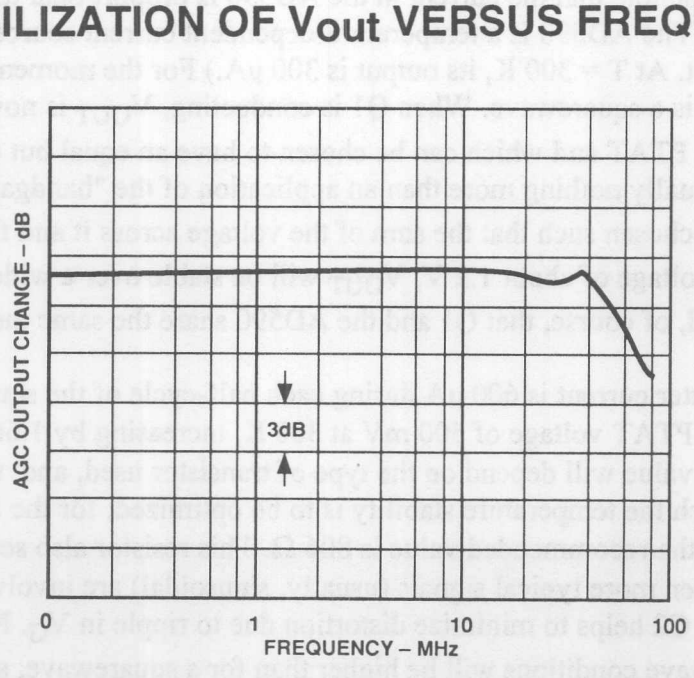


Figure 9.2.25

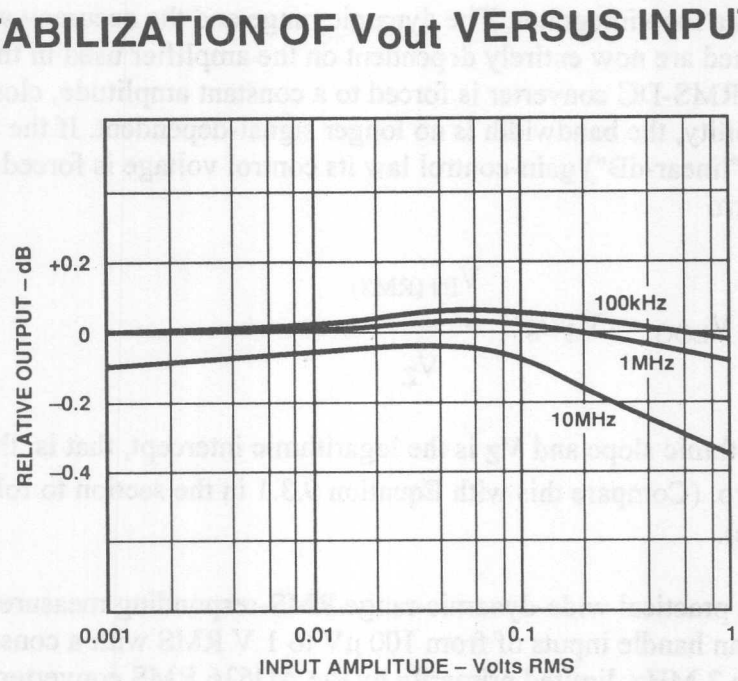


Figure 9.2.26

While the "bandgap" principle used here sets the output amplitude to 1.2 V (for the squarewave case), the stabilization point can be set to any higher amplitude, up to the maximum output of $\pm(V_S - 2)$ V which the AD600 can support. It is only necessary to split R2 into two components of appropriate ratio whose parallel sum remains close to the zero-TC value of 806 Ω. For example, using R2a = 1.62 kΩ from the emitter of Q1 to V_{OUT} and R2b = 1.62 kΩ from the emitter node to ground, the output can be raised to 2 V RMS for sinewave signals, without altering the temperature stability.

9

9.2.7 AN 80 dB RMS-LINEAR-dB MEASUREMENT SYSTEM

Monolithic RMS-DC converters provide an inexpensive means to measure the RMS value of a signal of arbitrary waveform. They also may provide a low-accuracy logarithmic ("decibel-scaled") output. However, they have a fairly small dynamic range – typically only 50 dB. More troublesome is that the bandwidth is roughly proportional to the signal level; for example, the AD636 provides a 3 dB bandwidth of 900 kHz for an input of 100 mV RMS, but only a 100kHz bandwidth for an input of 10 mV RMS. Its "raw" logarithmic output is unbuffered, uncalibrated and not stable over temperature requiring considerable support circuitry, including at least two adjustments and a special high-TC resistor.

All of these problems can be eliminated using an AD636 as *merely the detector element* in an AGC loop, in which the difference between the RMS output of the amplifier and a fixed DC reference are nulled in a loop integrator. The dynamic range and the accuracy with which the signal can be determined are now entirely dependent on the amplifier used in the AGC system. Since the input to the RMS-DC converter is forced to a constant amplitude, close to its maximum input capability, the bandwidth is no longer signal-dependent. If the amplifier has an exactly-exponential ("linear-dB") gain-control law its control voltage is forced by the AGC loop to have the general form

$$V_{LOG} = V_S \; lgt \; \frac{V_{IN\,(RMS)}}{V_Z} \qquad \text{Eq. 9.2.19}$$

where V_S is the logarithmic slope and V_Z is the logarithmic intercept, that is, the value of V_{IN} for which V_{LOG} is zero. (Compare this with Equation 9.3.1 in the section to follow on logarithmic amplifiers).

Figure 9.2.27 shows a practical wide-dynamic-range RMS-responding measurement system using the AD600. It can handle inputs of from 100 µV to 1 V RMS with a constant measurement bandwidth of 20 Hz to 2 MHz, limited primarily by the AD636 RMS converter. Its logarithmic output is a loadable voltage, accurately-calibrated to 100 mV/dB, or 2V per decade, which simplifies the interpretation of the reading when using a DVM, and is arranged to be –4 V for an input of 100 µV RMS input, zero for 10 mV, and +4 V for a 1V RMS input. In terms of Eq. 9.2.19, V_S is 2 V and V_Z is 10 mV.

A COMPLETE 80dB RMS-LINEAR-dB MEASUREMENT SYSTEM

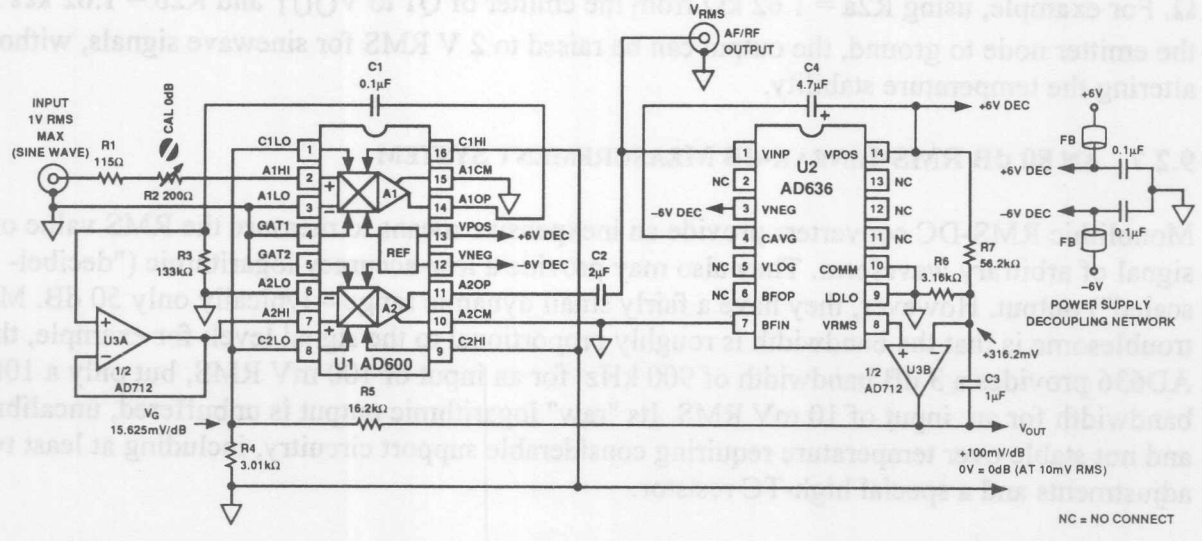


Figure 9.2.27

Note that the peak "log-output" of ±4 V requires the use of ±6 V supplies for the dual op-amp U3 (AD712) although lower supplies would suffice for the AD600 and AD636. If only ±5 V supplies are available it will be either necessary to use a reduced value for V_S (say, 1 V, in which case the peak output would be only ±2 V) or restrict the dynamic range of the signal to about 60 dB.

As in the previous case, the two amplifiers of the AD600 are used in cascade. However, the 6 dB attenuator and low-pass filter found in Figure 9.2.24 are replaced by a unity-gain buffer amplifier U3A, whose modest bandwidth eliminates the risk of instability at the highest gains. The buffer also allows the use of a high-impedance coupling network (C1/R3) which introduces a high-pass corner at about 12 Hz. An input attenuator of 10 dB (X 0.316) is now provided by R1 + R2 operating in conjunction with the AD600's input resistance of 100 Ω. The adjustment provides exact calibration of V_Z in critical applications, but R1 and R2 may be replaced by a fixed resistor of 215 Ω if very close calibration is not needed, since the input resistance of the AD600 (and all other key parameters of it and the AD636) are already laser-trimmed for accurate operation. This attenuator allows inputs as large as ±4 V to be accepted, that is, signals with an RMS value of 1 V combined with a crest-factor of up to 4.

The output of A2 is AC-coupled via another 12 Hz high-pass filter formed by C2 and the 6.7 kΩ input resistance of the AD636. The averaging time-constant for the RMS-DC converter is determined by C4. The unbuffered output of the AD636 (at pin 8) is compared with a fixed voltage of +316 mV set by the positive supply voltage of +6 V and resistors R6 and R7. (V_Z is proportional to this voltage and systems requiring greater calibration accuracy should replace the supply-dependent reference with a more stable source. However, V_S is independent of the supply voltages, being determined by the on-chip band-gap reference in the X-AMP.) Any difference in these voltages is integrated by the op-amp U3B, with a time-constant of 3 ms formed by the parallel sum of R6/R7 and C3.

Now, if the gain of the AD600 is too high, V_{OUT} will be greater than the "set-point" of 316 mV, causing the output of U3B – that is, V_{LOG} – to ramp up (note that the integrator is non-inverting). A fraction of V_{LOG} is connected to the *inverting* gain-control inputs of the AD600, so causing the gain to be reduced, as required, until V_{OUT} is exactly equal to 316 mV (DC), at which time the AC voltage at the output of A2 is forced to be exactly 316 mV (RMS). This fraction is set by R4 and R5 such that a 15.625 mV change in the control voltages of A1 and A2 – which would change the gain of the two cascaded amplifiers by 1 dB – requires a change of 100mV at V_{LOG}. Notice here that since A2 is forced to operate at an output level well below its capacity, waveforms of high crest-factor can be tolerated throughout the amplifier.

To verify the operation, assume an input of 10 mV RMS is applied to the input, which results in a voltage of 3.16 mV RMS at the input to A1, due to the 10 dB loss in the attenuator. If the system performs as claimed, V_{LOG} (and hence V_G) should be zero. This being the case, the gain of both A1 and A2 will be 20 dB and the output of the AD600 will therefore be 100 times (40dB) greater than its input, which evaluates to 316 mV RMS. This is the input required at the AD636 to balance the loop, confirming the basic operation. Note that unlike most AGC circuits,

(which often have a high temperature-coefficient of gain due to the internal "kT/q" scaling – see Eq. 9.2.1) these voltages, and thus the output, of this measurement system is very stable over temperature. This behavior arises directly from the fundamental and exact exponential calibration of the ladder attenuator.

Typical results are presented for a sinewave input at 100 kHz. Figure 9.2.28 shows that the output is held very close to the set-point of 316 mV RMS over an input range in excess of 80dB.

Figure 9.2.29 shows the "decibel" output voltage, V_{LOG}, and Figure 9.2.30 shows that the *deviation* from the ideal output predicted by Eq. 9.2.19 is within ±1 dB for the 80 dB range from 80 μV to 800 mV.

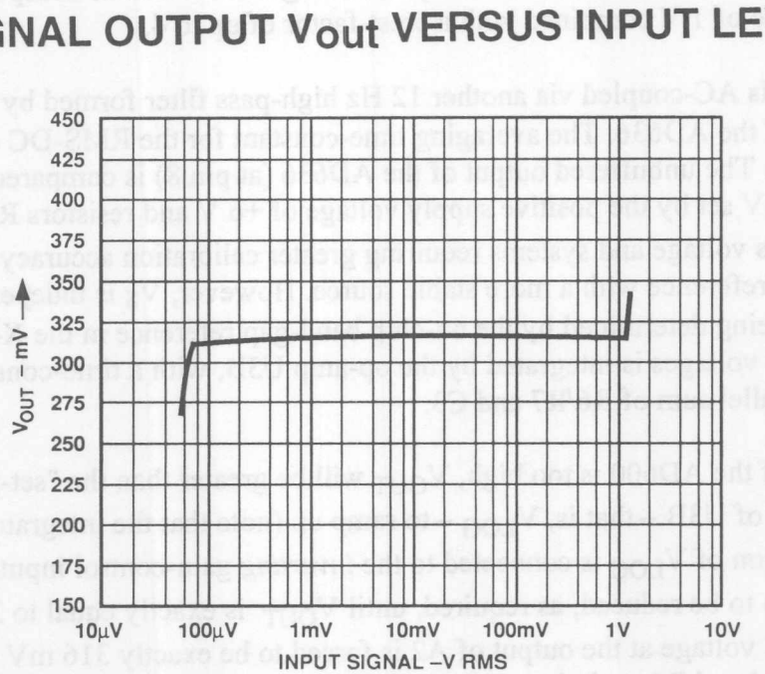


Figure 9.2.28

THE LOGARITHMIC OUTPUT V_{LOG} VERSUS INPUT LEVEL

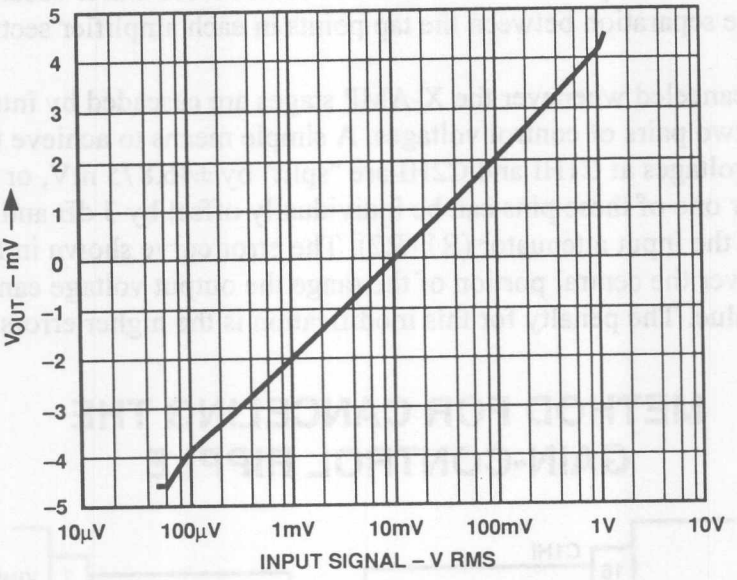


Figure 9.2.29

DEVIATION FROM THE IDEAL LOGARITHMIC OUTPUT

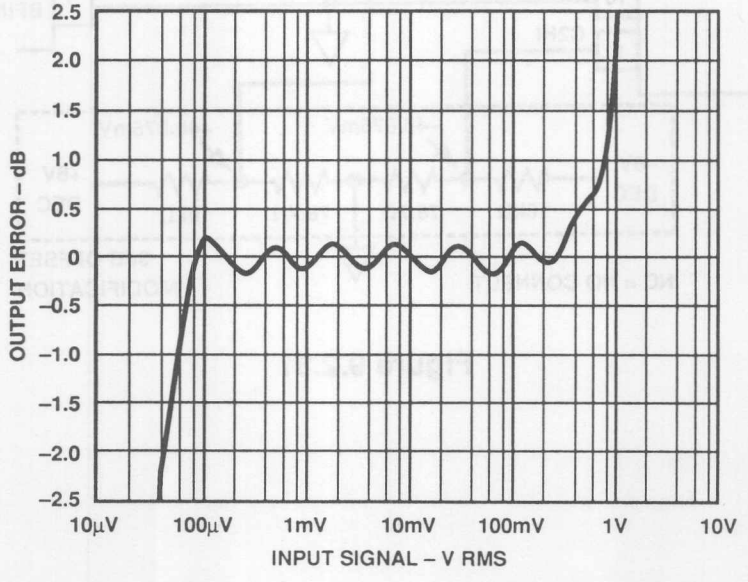


Figure 9.2.30

By suitable choice of the input attenuator R1+R2, this could be centered to cover any range from 25 μV to 250 mV to, say, 1 mV to 10 V, with appropriate correction to the value of V_Z. (Note that V_S is not affected by the changes in the range). The gain ripple of ±0.2 dB seen in this curve is the result of the finite interpolation error of the X-AMP. Note that it occurs with a periodicity of 12 dB – twice the separation between the tap points in each amplifier section.

This ripple can be canceled whenever the X-AMP stages are cascaded by introducing a 3 dB offset between the two pairs of control voltages. A simple means to achieve this is shown in Figure 9.2.31: the voltages at C1HI and C2HI are "split" by ±46.875 mV, or ±1.5 dB. Alternatively, either one of these pins can be individually offset by 3 dB and a 1.5 dB gain adjustment made at the input attenuator (R1+R2). The error curve shown in Figure 9.2.32 demonstrates that over the central portion of the range the output voltage can be maintained very close to the ideal value. The penalty for this modification is the higher errors at the extremities of the range.

METHOD FOR CANCELING THE GAIN-CONTROL RIPPLE

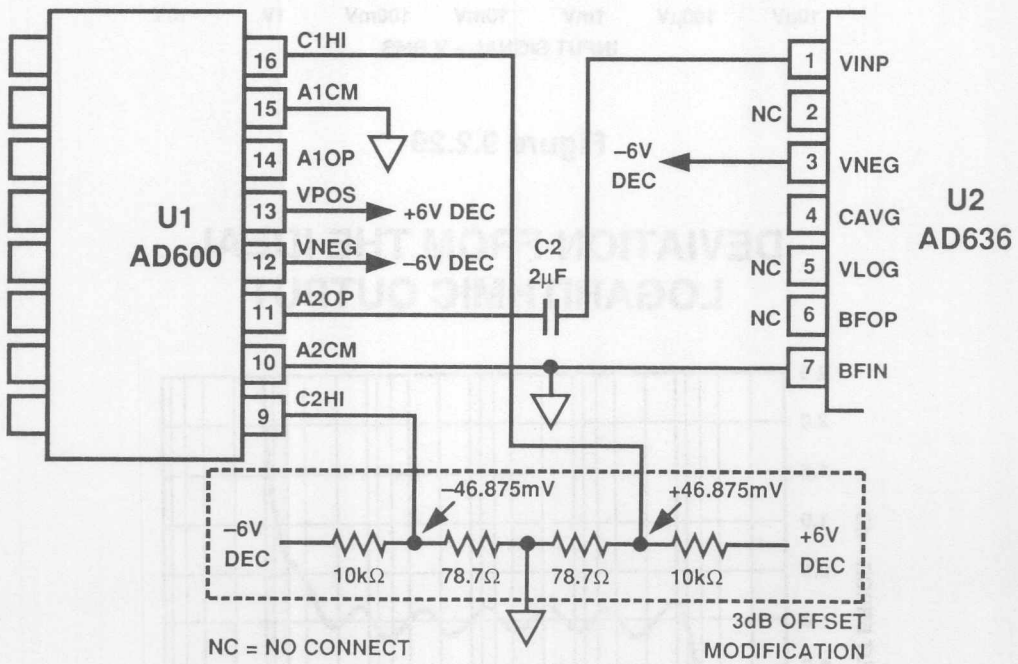


Figure 9.2.31

LOGARITHMIC ERROR USING THE PREVIOUS CIRCUIT MODIFICATION

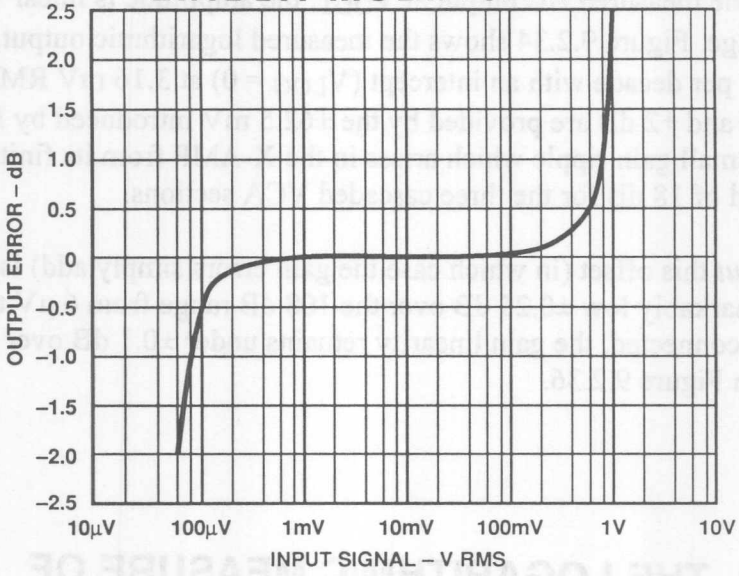


Figure 9.2.32

9.2.8 100 dB RMS/AGC SYSTEM WITH MINIMAL GAIN ERROR

Using three VCA sections, the measurement or AGC range can be extended still further. Figure 9.2.33 shows an RMS-responding AGC circuit which accepts inputs of 10 µV to 1 V RMS (–100dBV to 0 dBV) with generous over-range.

RMS/AGC SYSTEM WITH 100dB RANGE AND MINIMUM ERROR IN V_{LOG}

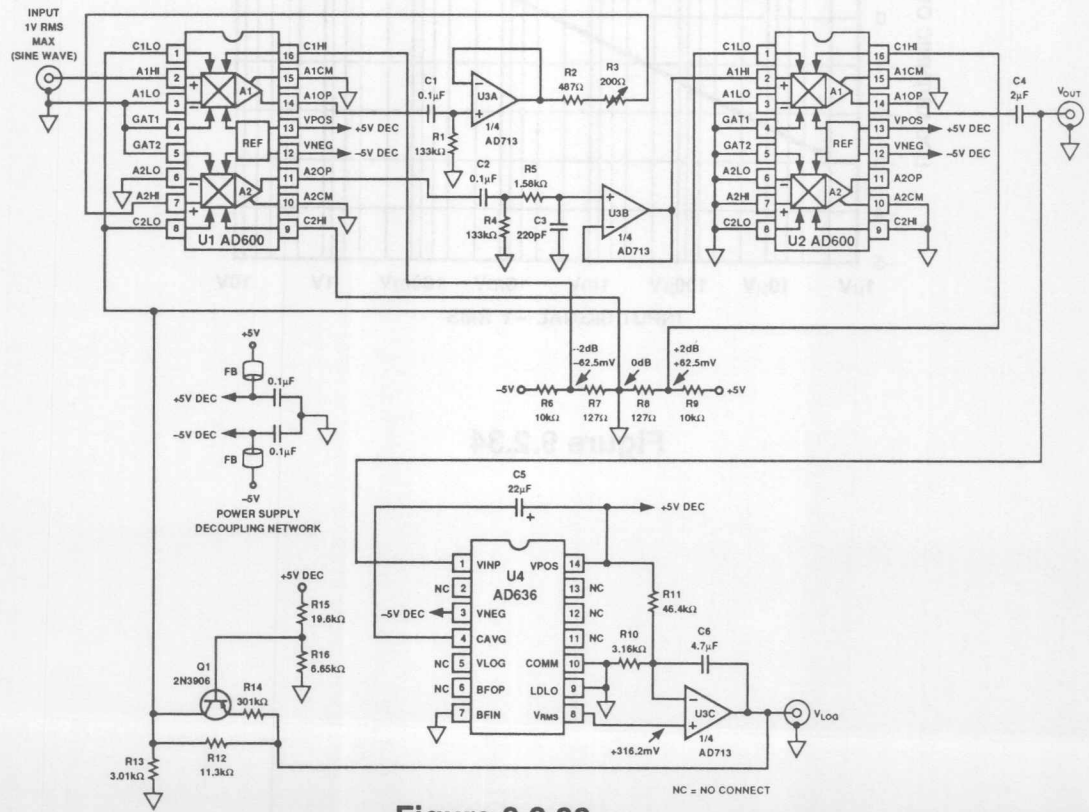


Figure 9.2.33

Figure 9.2.34 shows the measured AC output at V_{OUT}; the amplitude is linear within ±0.2 dB over the full input range. Figure 9.2.34 shows the measured logarithmic output, V_{LOG}, which is accurately-scaled 1 V per decade with an intercept (V_{LOG} = 0) at 3.16 mV RMS (–50 dBV). Gain offsets of –2 dB and +2 dB are provided by the ±62.5 mV introduced by R6–R9. These offsets eliminate the small gain ripple which arises in the X-AMP from its finite interpolation error, and has a period of 18 dB for the three cascaded VCA sections.

The gain ripple *without* this offset (in which case the gain errors simply add) is shown in Figure 9.2.35; it is still a remarkably low ±0.25 dB over the 108 dB range from 6 µV to 1.5 V RMS. With the gain offsets connected, the gain linearity remains under ±0.1 dB over the specified 100 dB range, as shown in Figure 9.2.36.

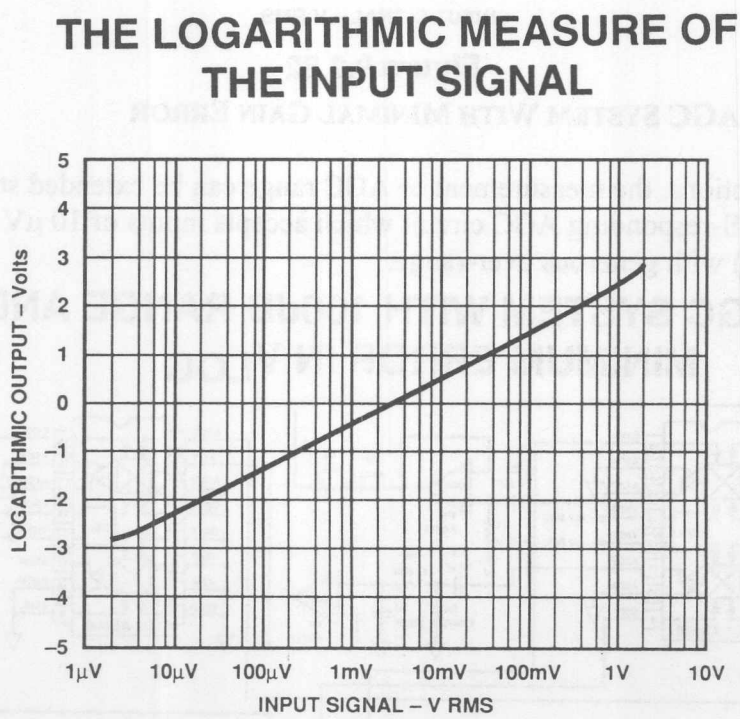


Figure 9.2.34

THE ABSOLUTE ERROR IN V_{LOG} WITHOUT RIPPLE CANCELLATION

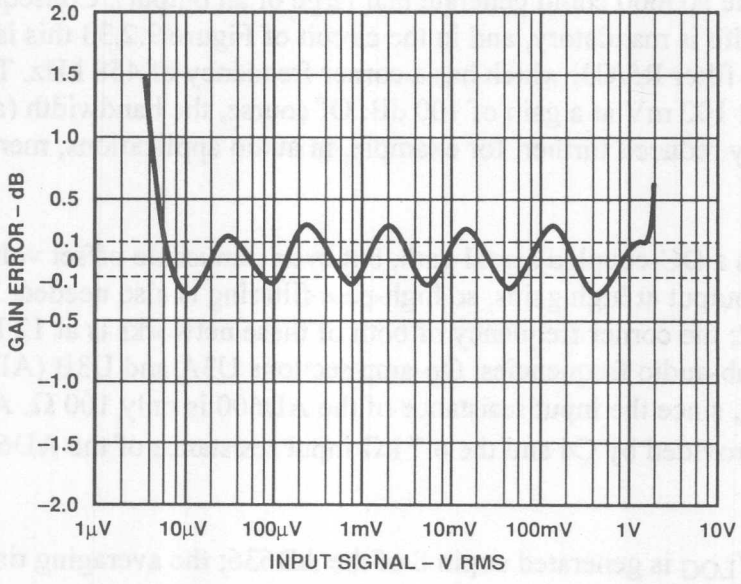


Figure 9.2.35

THE ABSOLUTE ERROR IN V_{LOG} WITH RIPPLE CANCELLATION

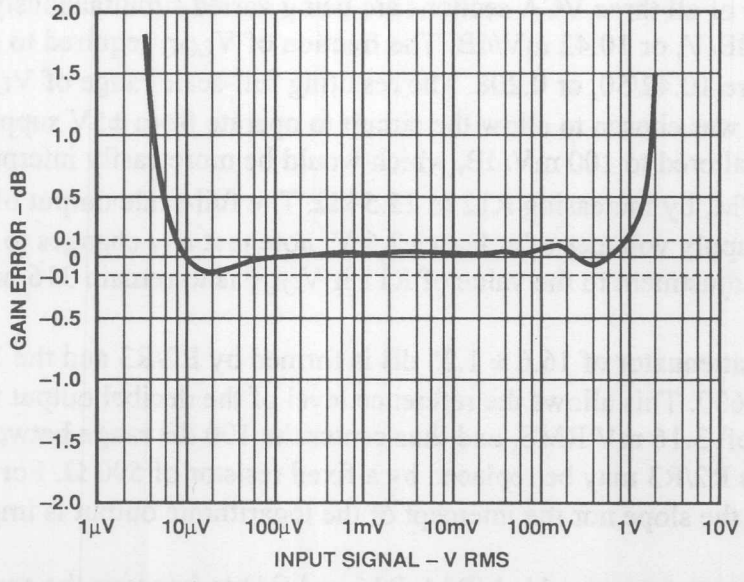


Figure 9.2.36

The maximum gain of the three cascaded amplifiers is 120 dB (one million). If no filtering were used, the noise-spectral-density of the first VCA (1.4 nV/√Hz), which amounts to an input-referred noise of 8.28 μV RMS in the full bandwidth (35 MHz), would amount to over 20 V pk-pk at the output (if the AD600 could generate that large of an output). Consequently, some reduction of bandwidth is mandatory, and in the circuit of Figure 9.2.33 this is provided by a single-pole low-pass filter R5/C3, which has a corner frequency of 458 kHz. This reduces the output noise to about 100 mV at a gain of 100 dB. Of course, the bandwidth (and hence output noise) could be easily reduced further, for example, in audio applications, merely by increasing C3.

The AD600 provides a DC-coupled signal path, but even minuscule offset voltages at the input would overload the output at high gains, so high-pass filtering is also needed. This is provided by R1/C1 and R4/C2; the corner frequency of both of these networks is at 12 Hz, providing operation down to sub-audio frequencies. Op-amp sections U3A and U3B (AD713) provide impedance buffering, since the input resistance of the AD600 is only 100 Ω. A further high-pass section at 12 Hz is provided by C4 and the 6.7 kΩ input resistance of the AD636 RMS converter.

The RMS value of V_{LOG} is generated at pin 8 of the AD636; the averaging time for this process is determined by C5, and the value shown results in less than 1 % RMS error at 20 Hz. The slowly-varying V_{RMS} is compared with a fixed DC reference of 316 mV, derived from the positive supply by R10/R11. Any difference between these two voltages is integrated in C6, in conjunction with op-amp U3C, the output of which is V_{LOG}. A fraction of this voltage, determined by R12 and R13, is returned to the gain-control inputs of all AD600 sections. An increase in V_{LOG} lowers the gain, because this voltage is connected to the *inverting-polarity* control inputs.

Now, since the gains of all three VCA sections are being varied simultaneously, the scaling is not 32 dB/V but 96 dB/V, or 10.42 mV/dB. The fraction of V_{LOG} required to set its scaling to 50 mV/dB is therefore 10.42/50, or 0.208. The resulting full-scale range of V_{LOG} is nominally ±2.5 V. This scaling was chosen to allow the circuit to operate from ±5V supplies. Optionally, the scaling could be altered to 100 mV/dB, which would be more easily interpreted when V_{LOG} is displayed on a DVM, by increasing R12 to 25.5 kΩ. The full-scale output of ±5V then requires the use of supply voltages of at least ±7.5 V; note that any changes to the supply voltages require an adjustment to the value of R11 if V_{OUT} is to remain 316 mV RMS.

A simple adjustable attenuator of 16.6 ± 1.25 dB is formed by R2/R3 and the 100 Ω input resistance of the AD600. This allows the reference level of the decibel output to be precisely set to zero for an input of 3.16 mV RMS, and thus center the 100 dB range between 10 μV and 1 V. In many applications R2/R3 may be replaced by a fixed resistor of 590 Ω. For example, in AGC applications, neither the slope nor the intercept of the logarithmic output is important.

A few additional components are added (R14–R16 and Q1) to improve the accuracy of V_{LOG} at the top end of the signal range (that is, for small gains). The gain starts rolling off when the

input to the first amplifier, U1A, reaches 0 dB. To compensate for this nonlinearity, Q1 turns on when V_{LOG} is approximately +1.5 V and increases the feedback to the control inputs of the AD600s, thereby needing a smaller voltage at V_{LOG} to maintain the input to the AD636 at the set-point of 316 mV RMS.

9.2.9 120 dB RMS/AGC SYSTEM WITH OPTIMAL S/N RATIO

In the last case, all gains were adjusted *simultaneously*, resulting in an output S/N ratio that is always less than optimal. The use of *sequential* gain-control results in a major improvement in S/N ratio, with only a slight penalty in the accuracy of V_{LOG}, and no penalty at all in the stabilization accuracy of V_{OUT}. The idea is simply to increase the gain of the three VCA sections one at a time as the signal level increases, beginning with the first stage. Thus, the highest possible S/N ratio is maintained throughout the amplifier chain. This can be easily achieved with the AD600 because its gain remains accurate even when the control input is overdriven; that is, each gain-control "window" of 1.25 V is used fully before moving to the next amplifier to the right.

Figure 9.2.37 shows the circuit for the sequential control scheme which is only slightly changed from Figure 9.2.33. R6–R9 with R16 provide offsets of 42.14 dB between the individual amplifiers to ensure smooth transitions between the gain of each successive X-AMP, with the sequence of gain increase being U1A first, then U1B and lastly U2A.

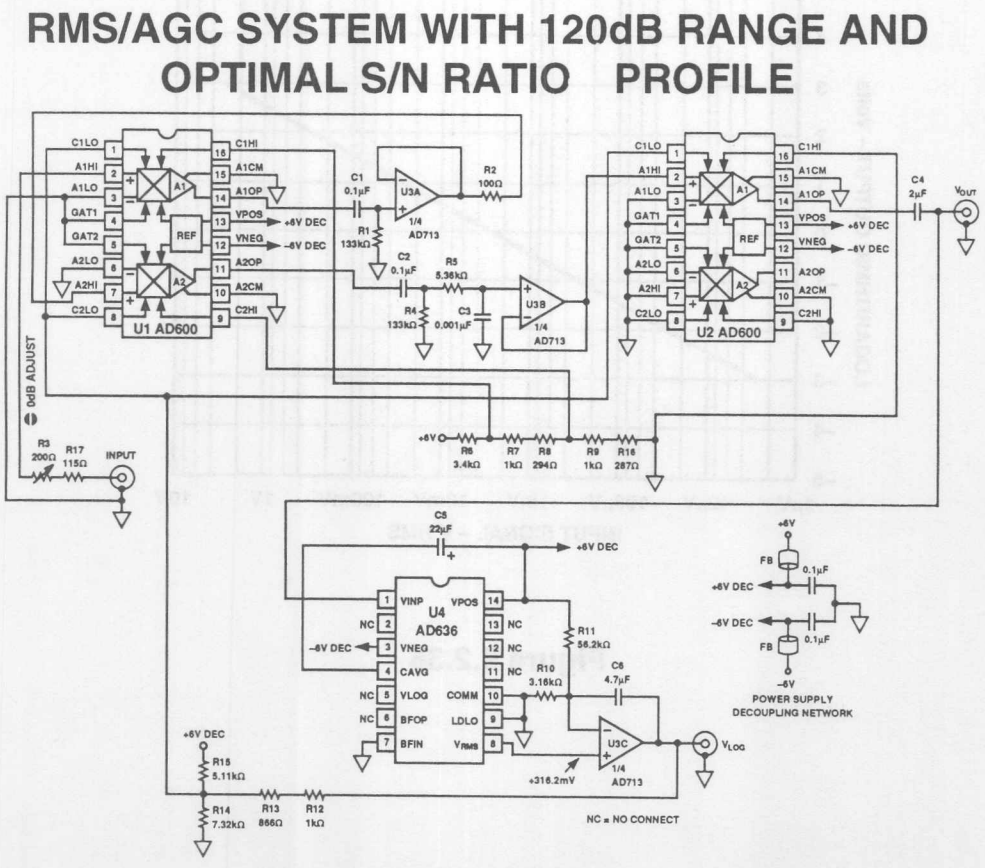


Figure 9.2.37

The precise value of the offset voltages is critical if maximum accuracy is to be maintained.. The adjustable attenuator provided by R3+R17 and the 100 Ω input resistance of U1A, plus the fixed 6dB attenuator provided by R2 and the input resistance of U1B, are included to set V_{LOG} to read 0 dB when V_{IN} is 3.16 mV RMS (–50 dBV) and thus center the 100 dB range between 10 μV and 1 V. R5 and C3 provide a 3 dB bandwidth of 30 kHz. R12–R15 change the scaling from 625 mV/decade at the AD600 gain-control inputs to the more convenient 1 V/decade at the logarithmic output. The increased range of the control voltage (compared to the previous circuit) requires the use of ±6 V supplies. Figure 9.2.38 shows V_{LOG} to be essentially linear over a full 120 dB range.

Figure 9.2.39 shows that the composite error ripple due to the individual gain functions is within ±0.2 dB (dotted lines) from 6 μV to 2 V. The small perturbations at about 200 μV and 20 mV, caused by the impracticality of matching the gain functions perfectly, are the only sign that the gains are now sequential. V_{OUT} remains within less than 1 mV of its set-point value of 316 mV RMS (that is, –10 dBV) for all input levels.

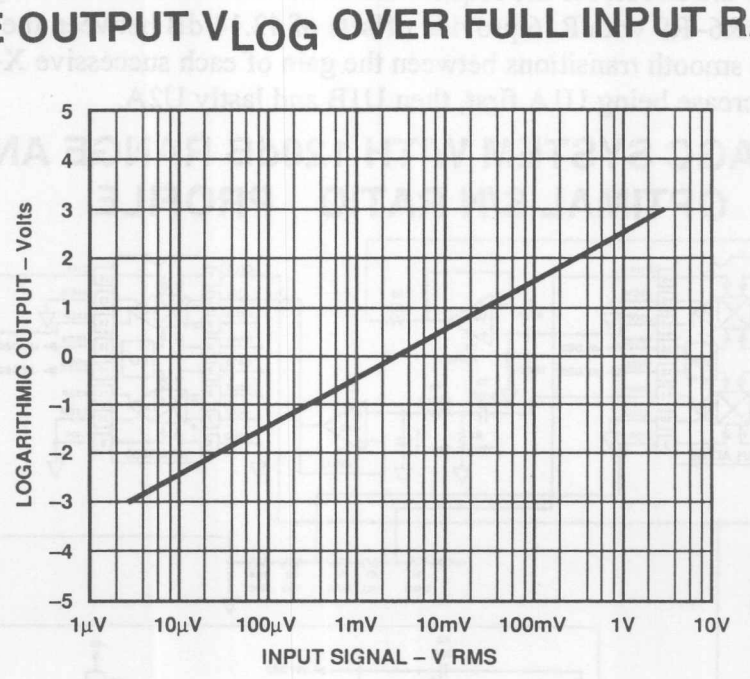


Figure 9.2.38

THE ERROR IN THE LOGARITHMIC OUTPUT V_{LOG}

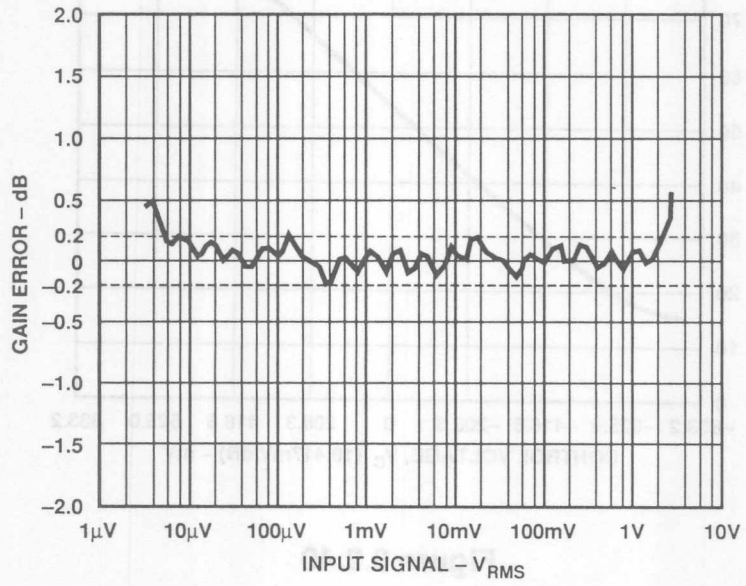


Figure 9.2.39

To more directly compare the signal-to-noise performance in the "simultaneous" and "sequential" modes of operation, all interstage attenuation was eliminated (R2 and R3 in Figure 9.2.33; R2 in Figure 9.2.37), the input of U1A was shorted, R5 was selected to provide a 3 dB bandwidth of 20 kHz (R5 = 7.87 kΩ), and the gain control voltage was varied, using an external source. The RMS value of the noise was then measured at V_{OUT} and expressed as an S/N ratio relative to 0 dBV, this being almost the maximum output capability of the AD600. Results for the simultaneous mode can be seen in Figure 9.2.40. The S/N ratio degrades uniformly as the gain is increased. Note that since the inverting gain control inputs C1LO and C2LO are used, the gain decreases for more positive values of the gain-control voltage.

THE OUTPUT S/N RATIO VERSUS GAIN FOR THE "SIMULTANEOUS" MODE

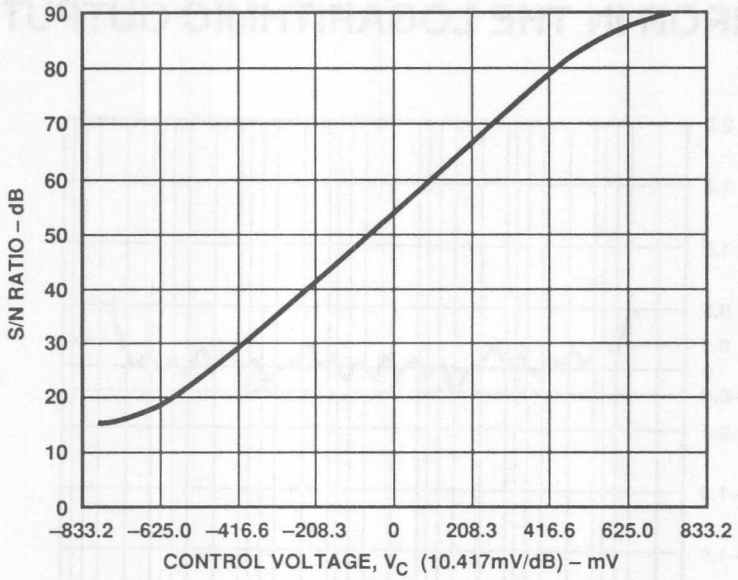


Figure 9.2.40

By contrast, the S/N ratio for the sequential mode is shown In Figure 9.2.41. In this case, U1A always acts as a fixed noise source; varying its gain has no effect on its output noise. (Recall that this is a feature of the X-AMP technique.) Thus, for the first 40 dB of control range (actually slightly more) when only this VCA section is having its gain varied, the S/N ratio remains constant. In this interval, the gains of U1B and U2A are at their minimum value of –1.07 dB. For the next 40 dB, the gain of U1A remains at its maximum value of 41.07 dB while only the gain of U1B is varied and that of U2A remains at its minimum value of –1.07 dB. In this interval, the fixed output noise of U1A is amplified by the increasing gain of U1B and the S/N ratio progressively worsens.

THE OUTPUT S/N RATIO VERSUS GAIN FOR THE "SEQUENTIAL" MODE

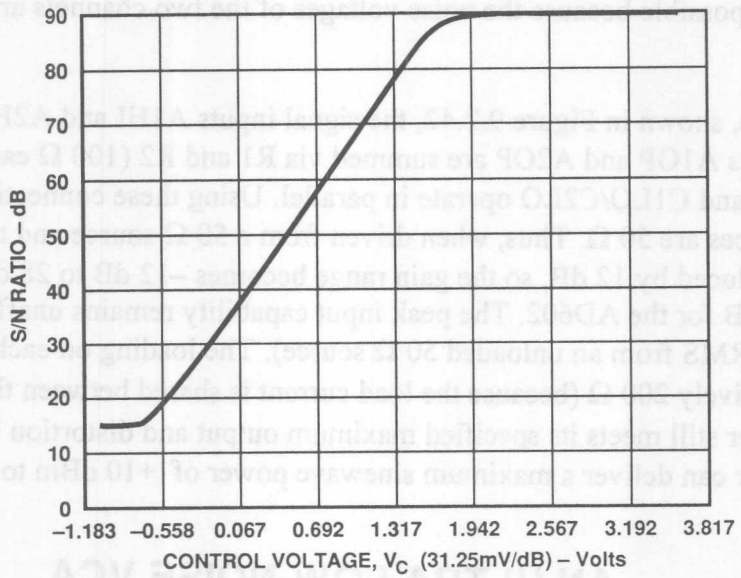


Figure 9.2.41

Once U1B reaches its maximum gain of 41.07 dB its output also becomes a gain-independent noise source. This noise is presented to U2A. As the control voltage is further increased, the gains of both U1A and U1B remain fixed at their maximum value while that of U2A varies from –1.07 dB to 41.07 dB and the S/N ratio continues to worsen, Figure 9.2.41 shows that the S/N ratio remains constant at 90 dB for the first 40 dB of gain range.

This arrangement of staggered gains can be easily implemented because when the control inputs of the AD600 are over-driven, the gain limits to its minimum or maximum value, without side-effects. This avoids the need for awkward nonlinear shaping circuits. It is the somewhat peculiar value of the gain in these over-driven states (–1.07 dB and 41.07 dB, not 0 dB and 40 dB) that explains the rather odd values needed for the offset voltages.

The optimization of the output S/N ratio is of obvious value in AGC systems. However, in applications where these circuits are considered for their wide-range logarithmic measurement capabilities, the inevitable degradation of S/N ratio at high gains need not seriously impair their utility. In fact, the bandwidth of the circuit shown in Figure 9.2.37 was specifically chosen so as to improve measurement accuracy, by using the system noise to alter the shape of the log-error curve at low signal levels.

9.2.10 AN ULTRA-LOW NOISE VCA

The two channels of an AD600 or AD602 may be operated in parallel to achieve a 3 dB improvement in noise level, providing 1 nV/√Hz without any loss of gain-accuracy or bandwidth. This is possible because the noise voltages of the two channels are, of course, uncorrelated.

In the simplest case, shown in Figure 9.2.42, the signal inputs A1HI and A2HI are tied directly together, the outputs A1OP and A2OP are summed via R1 and R2 (100 Ω each) and the control inputs C1HI/C2HI and C1LO/C2LO operate in parallel. Using these connections, both the input and output resistances are 50 Ω. Thus, when driven from a 50 Ω source and terminated in a 50 Ω load, the gain is reduced by 12 dB, so the gain range becomes –12 dB to 28 dB for the AD600 and –22 dB to 18 dB for the AD602. The peak input capability remains unaffected (1V RMS at the IC pins, or 2V RMS from an unloaded 50 Ω source). The loading on each channel, with a 50 Ω load, is effectively 200 Ω (because the load current is shared between the two channels) so the overall amplifier still meets its specified maximum output and distortion levels for a 200 Ω load. This amplifier can deliver a maximum sinewave power of +10 dBm to the load.

AN ULTRA-LOW-NOISE VCA

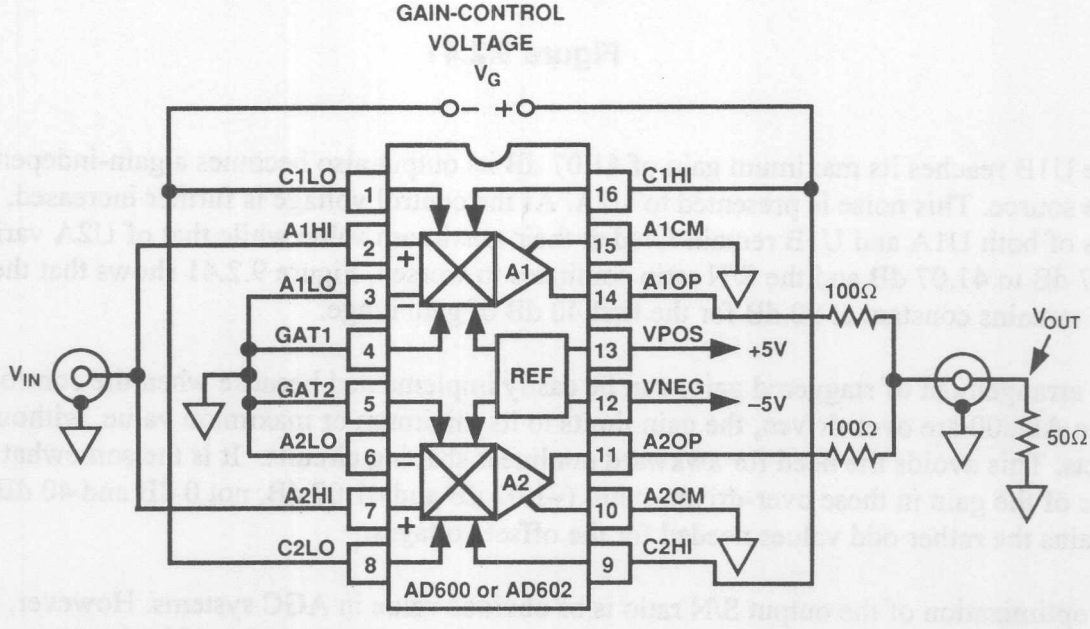


Figure 9.2.42

Figure 9.2.43 shows a couple of modifications. The outputs are now summed actively using the AD844 op-amp, resulting incidentally in a sign-reversal at the final output. Using the minimum feedback resistance of R3 = 806 Ω, the bandwidth is not impaired by the inclusion of this amplifier, and the overall gain may now be altered by R1 and R2. In the example shown, we have included a 50 Ω reverse-termination resistor, and have again assumed a 50 Ω source impedance, so the initial gain deficit is 12 dB. Thus, by using R1 = R2 = 402 Ω, the overall gain, from loaded 50 Ω source to a 50 Ω load, is restored to that of the AD600 or AD602 alone. Note, however, that using these values the AD844 may clip at full gain, unless it is provided with adequate supply voltages. Many useful variants of this arrangement can be devised, providing a near-universal low-noise 35 MHz variable-gain block.

AN ELABORATION OF FIGURE 9.2.42

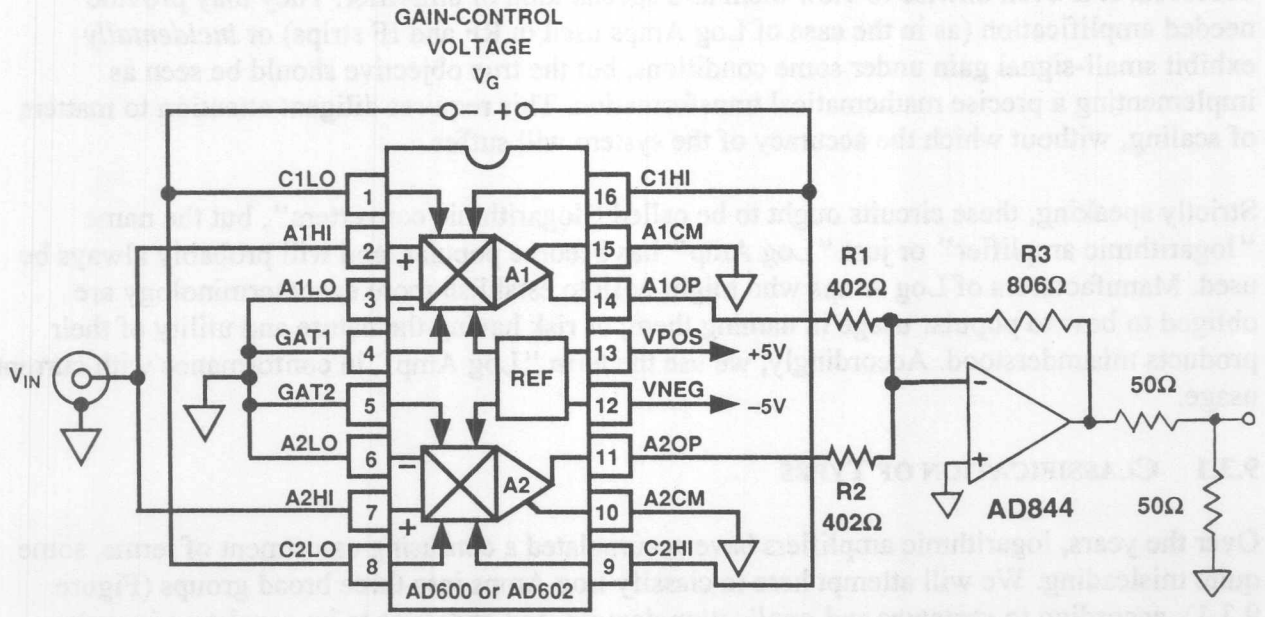


Figure 9.2.43

9. 3 LOGARITHMIC AMPLIFIERS

Logarithmic amplifiers are used wherever a signal of large dynamic range must be compressed down to a signal of substantially smaller dynamic range, without the intervention of an AGC loop. The transfer function need not be logarithmic to achieve useful compression. However, the logarithmic function is valuable because it provides an output which changes by the same amount between application of any given ratio of input amplitudes, rendering the output easy to interpret. The scaling of might be 1 V/decade, in which case the output changes by 1 V for any ten-fold increase of the input.

Specifying logarithmic circuit performance requires care in defining terms. The literature abounds with poorly written explanations of fundamental issues, beginning with the naming of such devices. By calling these circuits "amplifiers" their nonlinear nature is in danger of being obscured. It is even unwise to view them as a special kind of amplifier. They may provide needed amplification (as in the case of Log Amps used in RF and IF strips) or *incidentally* exhibit small-signal gain under some conditions, but the true objective should be seen as implementing a precise mathematical transformation. This requires diligent attention to matters of scaling, without which the accuracy of the system will suffer.

Strictly speaking, these circuits ought to be called "logarithmic converters", but the name "logarithmic amplifier" or just "Log Amp" has become popular, and will probably always be used. Manufacturers of Log Amps who might wish to establish more exact terminology are obliged to bow to popular usage in naming them, or risk having the nature and utility of their products misunderstood. Accordingly, we use the term "Log Amp" in conformance with current usage.

9.3.1 CLASSIFICATION OF TYPES

Over the years, logarithmic amplifiers have accumulated a confusing assortment of terms, some quite misleading. We will attempt here to classify Log Amps into three broad groups (Figure 9.3.1), according to *structure* and *application domain*, and endeavor to be consistent in matters of terminology and nomenclature.

Translinear Log Amps provide a very wide dynamic range in response to a quasi-DC input, that is, one which is static or slowly varying. The design challenge here is to achieve excellent DC accuracy, with little emphasis on dynamic behavior. They are usually based on the *direct* invocation of the logarithmic (or "Translinear") properties of the bipolar transistor, explained later, and such Log Amps will be discussed in depth later. The widest dynamic range is achieved in this case when the input is in the form of a current. Practical translinear Log Amps can be designed to provide dynamic ranges approaching 180 dB. There are basic reasons why the dynamic behavior of such Log Amps is poor, as we shall see later, although the principle can be optimized for use at moderate (a few MHz) frequencies.

Baseband Log Amps, also known as "Video Log Amps" (although they are rarely used in video-display-related applications) respond to the *instantaneous* value of some rapidly-changing input (usually a voltage). This is often achieved using a technique which is best described as

"progressive compression", in which the logarithmic response can be approximated, to any arbitrary accuracy, through the use of cascaded amplifier stages having signal-dependent gain.

Most baseband Log Amps accept inputs having only one polarity and are usually DC-coupled. They are commonly used to compress pulse signals in which the "baseline" must be accurately preserved. When used *after* a microwave detector, (a backward diode), the combination is referred to as a "Detector-Log-Video-Amplifier", or DLVA. In these applications, the smallest input to the Log Amp may be only a few microvolts, calling for extremely low input offset voltages; this is sometimes achieved through some form of auto-nulling or DC restoration technique. Dynamic ranges of typical video Log Amps range from about 40 dB to 85 dB. DLVAs frequently include some deliberate deviation from a strictly-logarithmic response to first-order compensate for nonlinearities in a specific detector.

A special type of baseband Log Amp, called a *True Log Amp*, can accept inputs of *either polarity* and generate an output whose sign follows that of the input. Here, we are faced with typical misnomer, since a "true log" response would require the output to have a singularity of $\pm\infty$ as the input passes through zero, and anyway the log function has no simple meaning for negative arguments. In fact, the output of a practical amplifier of this type passes through zero when the input does, just as for any amplifier providing a bipolar response.

TYPES OF LOG AMPS

- **Translinear Log Amps:**
  - Based on Logarithmic (or translinear) Properties of Bipolar Transistors
  - Wide Dynamic Range, Poor ac Performance
- **Baseband Log Amps:**
  - Respond to Instantaneous Value of Rapidly Changing Input
  - "Progressive Compression" Technique Often Used
  - Sometimes Called "Video Log Amps"
  - "True Log Amp" Accepts Bipolar Inputs Sign of Output Follows Input
- **Demodulating Log Amps:**
  - AC Input Signal is Rectified
  - Output is the Modulated Envelope of the Input
  - Often Called "Successive Detection Log Amp"

Figure 9.3.1

Demodulating Log Amps rectify the AC signals applied to the input and use low-pass filtering to extract the running average – that is – a baseband signal corresponding to the modulated envelope of the input. In a similar fashion to the baseband Log Amp, multiple cascaded amplifier/limiter stages are used to realize this function, which is then called a "Successive Detection Log Amp" (sometimes abbreviated to SDLA). The signal frequency may be at the low megahertz to as high as several gigahertz. The low-frequency limit is invariably determined by AC-coupling components used to block DC bias and offset voltages from preceding gain stages and sometimes to reduce the effects of 1/f noise in the early stages. The resulting high-pass corner frequency is typically between a few tens of kilohertz and several megahertz.

In high-frequency Log Amps, the management of noise poses a major challenge. Bandpass filters are sometimes inserted between stages to limit the noise bandwidth. A bandpass response may also be desirable as part of the overall system function, for example, in the IF amplifier of a spectrum analyzer. However, the design of bandpass Log Amps needs care, since the scaling parameters, which define the logarithmic response, are now unavoidably frequency-dependent. Practical demodulating Log Amps provide dynamic ranges of from 40 dB to as high as 120 dB.

Although demodulating Log Amps were developed primarily for demanding military applications, there is no fundamental reason why they should be either expensive or incapable of operation down to low frequencies, for example, the audio range. One technique which we will discuss later is the use of DC-coupling throughout a monolithic chain of amplifier stages, augmented by a low-pass feedback network around the entire chain to effect a high-pass closed-loop response, whose corner frequency can be arbitrarily low. In fact, the continuous-time filter can be replaced by a sample/hold to correct for offset-induced errors on an occasional basis.

Demodulating Log Amps respond to a voltage input. Note that such amplifiers do *not* respond directly to input power, even though their input may be specified in these terms. In a fixed-impedance system any input voltage will correspond to a certain input power level, and a Log Amp *can be characterized* in terms of its output for this input. But it is important to realize that it is the input *voltage* that determines the output. For example, an RMS voltage of 223.6 mV represents a power of 1 mW when applied to a 50 Ω load, which is conventionally written 0dBm (meaning 0 dB relative to 1 mW). At this input level, a Log Amp would respond with some output, say 1 V. Now, if we were simply to alter the reference impedance at the input to 100 Ω, the input power would halve, but the Log Amp response would be unchanged.

While this classification has tried to avoid excessive mention of techniques, we need to briefly mention a special type of Log Amp, which may be of increasing importance as the integrated circuits needed to implement this approach become available. The key element is a *linear* amplifier whose gain may be controlled in a "direct-decibel" fashion, that is, whose gain is an exponential function of a control input, such as the X-AMP described in the previous section. In that section, we showed how an X-AMP may be used to implement demodulating logarithmic conversion, with the important property that the system may now be RMS-responding and independent of waveform.

9.3.2 SCALING OF LOG AMPS

Logarithmic circuits bring about a profound transformation of the signal, that goes far beyond "compression", and close attention to the details of the scaling of this function is necessary. The need for care in defining the Log Amp transfer function and its scaling parameters is not simply a matter of mathematical rigor. By viewing the device as a precision nonlinear element the designer is forced to think carefully about the source of these scaling voltages. If they cannot be defined with precision it is quite possible, even likely, that the circuit will not be stable with variations in supply voltage and temperature. Indeed, the main reason why commercially-available Log Amps have had such notoriously poor stability in the past is that in the traditional approach to their design was to view them first as amplifiers, second as having some kind of general compressive behavior, and only lastly being made to fit a logarithmic form to an acceptable level of accuracy.

We will therefore try to put the design of *all* types of Log Amps on a firm foundation, beginning with a clear formulation for the function. For all voltage-input, voltage-output logarithmic converters, this function *must* have the form

$$V_W = V_Y \, log\,(V_X / V_Z) \qquad \text{Eq. 9.3.1}$$

where V_W is the output, V_X is the primary signal input, which for now is assumed to be a varying DC voltage, V_Y is the slope voltage and V_Z is the intercept voltage, defined below. This formulation and terminology is consistent with that used in connection with other nonlinear circuits from Analog Devices, such as the multiplier family. Note in this connection that V_Y and V_Z are normally fixed voltages but can, in the most general case, also be signal inputs. The logarithm may be to any base, but in the context of practical Log Amps, whose input levels will often be expressed in decibels, base-ten logarithms are universally assumed. Changing the base of the logarithm in Eq 9.3.1 simply alters the effective value of V_Y. At this point, the function *log* means " logarithm to any base"; later, we will switch to *ln*, that is, natural (base-*e*) logarithms, in order to find certain integrals, and *lgt* will be used where we wish to specifically to refer to logarithms to base ten.

In general, V_W increases by an amount V_Y for each unit increase in the quantity $log(V_X / V_Z)$. When the logarithm is to base ten, that statement translates to "for each decade increase in V_X ", so in that case V_Y has the meaning of "Volts per decade". Figure 9.3.2 shows this function. The dotted regions correspond to those input levels for which the actual transfer function may be in error due to practical limitations. For example, at low input levels, noise and offset voltages will cause major errors, while at high input levels the finite signal-handling capability of the circuit will reach its limit.

GENERAL FORM OF A LOGARITHMIC TRANSFER FUNCTION

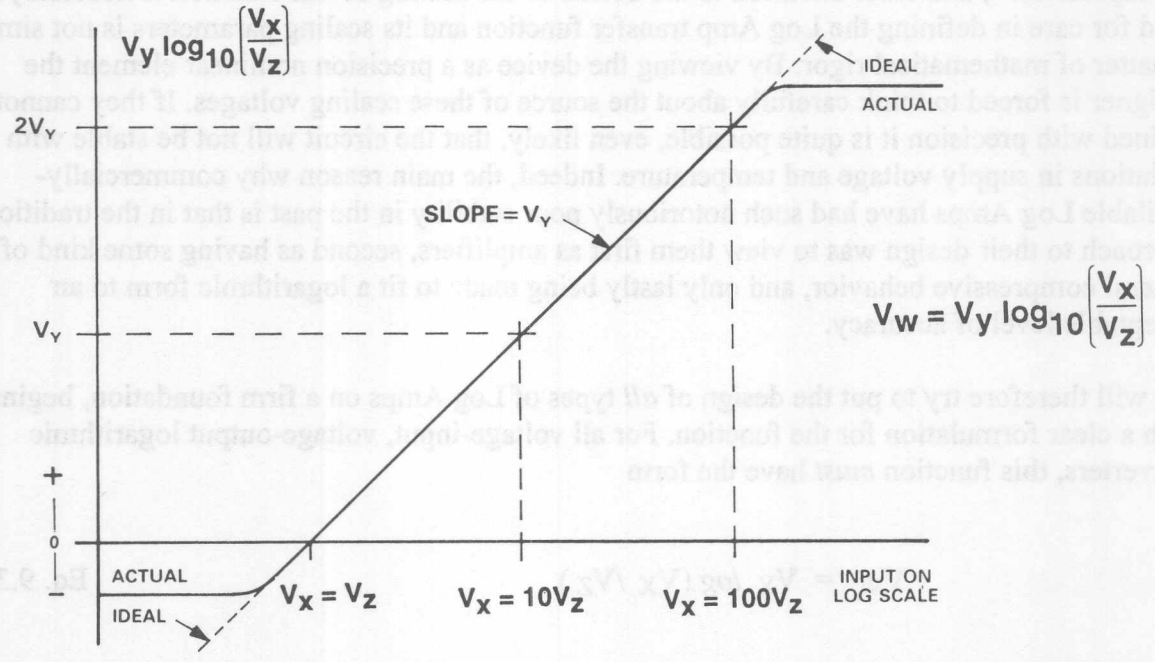


Figure 9.3.2

Eq. 9.3.1 is completely general and dimensionally consistent. V_W would be zero when $V_X = V_Z$, that is, V_Z defines the intercept of the transfer function on the horizontal axis. Note that we say "would be", because this may not actually occur, that is, V_Z may be the *extrapolated* intercept, and for reasons of design its value may be so small that the lower boundary on V_W will be first limited by noise or offsets. In fact, it is quite easy to set the intercept of a Log Amp to have *any* desired value of V_Z. This voltage need not be physically realizable; it could, for example, be as low as 1 nV. This can be readily appreciated by the following expansion:

$$V_W = V_Y \, log \, (V_X \, V_X / V_Z \, V_Z)$$

$$= V_Y \, log \, (V_X / V_Z) + V_A \qquad \text{Eq. 9.3.2}$$

where V_Z is the new value of the intercept achieved by adding some constant V_A to the output of the log-converter, having the value

$$V_A = V_Y \, log \, (V_X / V_Z) \qquad \text{Eq. 9.3.3}$$

Clearly, V_A, and therefore V_Z, can have any value we wish.

A well-designed Log Amp has at least one high-accuracy DC reference source, from which both V_Y and V_Z are derived. A good example of a Log Amp designed with attention to the matter of calibration accuracy is the Analog Devices AD640. It actually has two laser-trimmed reference generators, one of which (a full band-gap circuit) sets V_Y and the other (a PTAT cell) which determines the accuracy of both V_Y and V_Z. These reference generators play a role every bit as important as those in an A/D converter, V/F converter, or analog multiplier.

We can just as easily cast Eq. 9.3.1 in terms of a current-input and voltage-output device:

$$V_W = V_Y \log (I_X / I_Z) \qquad \text{Eq. 9.3.1a}$$

where V_Y, I_X and I_Z have equivalent specifications. This is the case for the translinear Log Amp, described in the next section. Alternatively, *all* signals may be in current form:

$$I_W = I_Y \log (I_X / I_Z) \qquad \text{Eq. 9.3.1b}$$

This is less common, but certainly quite practical. Finally, the function may be in the form of voltage-input/current-output:

$$I_W = I_Y \log (V_X / V_Z) \qquad \text{Eq. 9.3.1c}$$

This is the form found in RF Log Amps which use transconductance cells for demodulation; in these cases, the intermediate output current is converted back to a voltage.

9.3.3 SMALL-SIGNAL BEHAVIOR

Note that the above equations predict that V_W approaches $-\infty$ as V_X approaches zero. Of course, quite apart from the impracticality of this, there will be other limitations, particularly DC offsets at the input in the case of a baseband Log Amp, which limit the low-level accuracy. If we differentiate Eq. 9.3.1, using in this case base-*e* logarithms, with appropriate modification to V_Y, we find that the *incremental gain* of a Log Amp approaches $+\infty$ as V_{IN} approaches zero:

$$\frac{dV_W}{dV_X} = \frac{d}{dV_X} V_Y' \left\{ \ln (V_X) + \ln (V_Z) \right\}$$

$$= \frac{V_Y'}{V_X} \qquad \text{Eq. 9.3.4}$$

Thus, V_Z does not enter into the expression for incremental gain; this is consistent with the fact that we can arbitrarily alter V_Z after logarithmic conversion by the addition or subtraction of a

DC term at the output, as already shown. The notion that the gain must be infinite for zero-amplitude inputs should lead us to realize that the low-level accuracy of a demodulating Log Amp will be ultimately limited by (a) its maximum small-signal gain (determined in part by the number of stages) and (b) the noise level of the first stage. Of course, when the amplifier stages are DC-coupled the first stage offset might also be a limiting factor, but this can always be reduced by adjustment or the use of automatic offset control, as will be discussed later. Figure 9.3.3 shows the actual gain (from simulation) as a function of V_X for a high-performance multi-stage RF Log Amp. The reduction in gain for very small inputs is an artifact, due to an imperfection of the detectors: they are not exact absolute-value circuits with an "infinitely sharp" vertex, but become parabolic in this region, thus having zero gain. The tremendous variation in the incremental gain of a Log Amp should also serve as a reminder of the need for great caution in using small-signal analysis and simulation methods when dealing with Log Amps. Note in passing that the incremental gain is unity when the input voltage is equal to the scaling voltage.

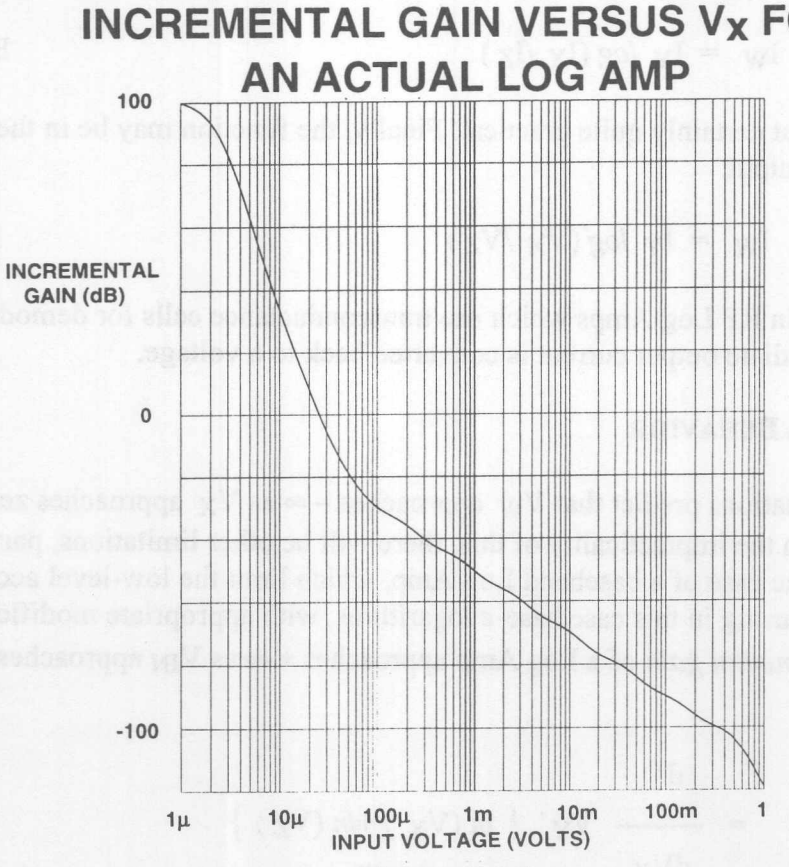


Figure 9.3.3

In discussing the scaling of Log Amps, the form of V_X is rarely mentioned. In the case of baseband converters this will often be a unipolar DC or quasi-DC (pulse) input, so Eq. 9.3.1 can be used without further consideration. But what happens when V_X becomes negative? There is no simple meaning to the log function when its argument is negative. Fortunately, we do not have to consider the mathematical consequences of this, because practical baseband Log Amps can be easily designed to handle inputs of either polarity with similar response. We can adapt Eq. 9.3.1 to handle this situation, by assuming that the circuit is arranged in some way to respond only to the magnitude of V_X and then restore its sign at the output:

$$V_W = sgn\,(V_X)\, V_Y\, ln\,(|V_X| / V_Z) \qquad \text{Eq. 9.3.5}$$

This is still not practical, however, because it requires that the output undergoes a transition from $-\infty$ to $+\infty$ as V_X diminishes and passes through zero. In fact, it is most likely in practical amplifiers intended to handle bipolar inputs that V_W will pass through *zero* when $V_X = 0$, because of the finite gain of its component sections. The situation described in Eq. 9.3.5 and its practical limitations can be handled by replacing the logarithmic function by the inverse hyperbolic sine function $sinh^{-1}$:

$$sinh^{-1}(u) = ln\,\{u + \sqrt{(u^2 + 1)}\} \qquad \text{Eq. 9.3.6}$$

$$= ln\,(2u) \quad \text{for } u >> 1$$

and

$$sinh^{-1}(-u) = -sinh^{-1}(u) \qquad \text{Eq.9.3.7}$$

Therefore, the "AC log" function may be written as

$$V_W = V_Y\, sinh^{-1}(V_X / 2V_Z) \qquad \text{Eq. 9.3.8}$$

Note the factor of two in the denominator of the argument. Figure 9.3.4 compares the ideal logarithmic transfer function with the hyperbolic sine in the region near $V_{IN} = 0$.

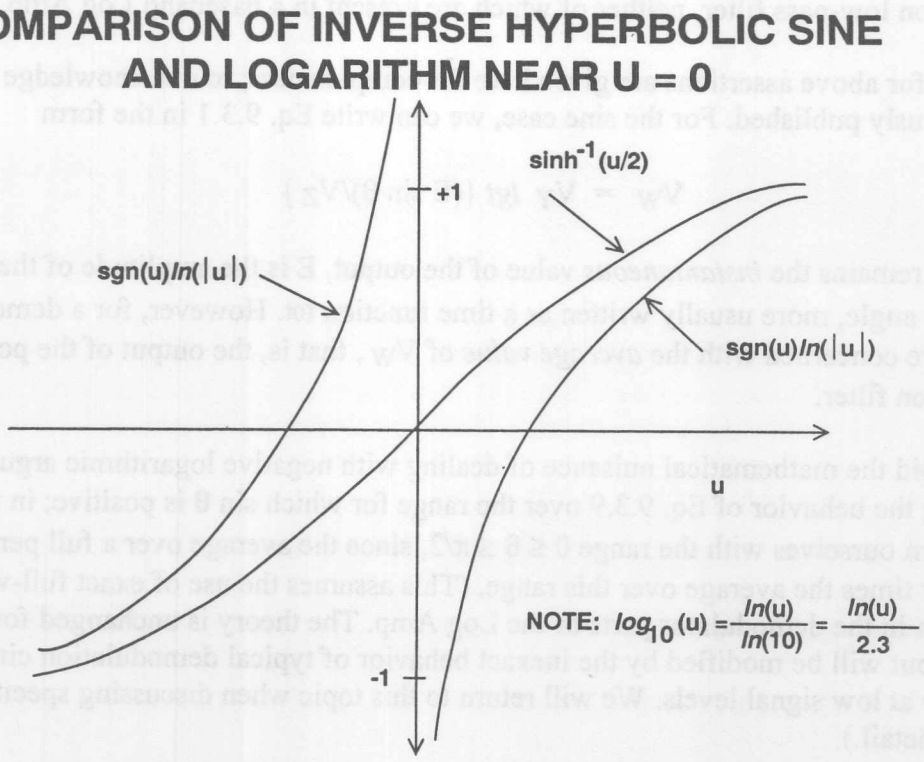


Figure 9.3.4

9.3.4 EFFECT OF WAVEFORM ON INTERCEPT

For the case of a demodulating Log Amp, having some kind of AC input, we must consider not just the amplitude of V_X , but its waveform, which has important practical consequences. In the performance specifications for a RF Log Amp, the signal is invariably presumed to be sinusoidal, and the intercept, usually specified in dBm (see above), applies to that implied operational mode. But for all other waveforms, the effective value of the intercept will be different. Note that the waveform has no effect on the slope (V_Y or I_Y).

For the case where the input is an amplitude-symmetric square wave, the rectification inherent in this type of Log Amp results in a response which is the same as that for a DC level. For a sinusoidal input where V_X is specified as the sine amplitude (not the RMS value), it will be exactly double this value. For an amplitude-symmetric triangle wave V_Z will be effectively increased by a factor of 2.718 (*e*). For a noise input with some prescribed probability density function (PDF) it will have a value dependent on the PDF: when this is Gaussian, V_Z is increased by a factor of 1.887.

These issues only became of interest with the advent of a fully-calibrated demodulating Log Amp (the Analog Devices AD640). Prior to that time, the intercept (often misleadingly called "log offset") had to be adjusted by the user, and most RF Log Amps could not be used at low enough frequencies where the response to a precise waveshape would be a matter of concern. Of course, the waveform-dependence of intercept does not arise in the case of video (baseband) Log Amps because it is a consequence of the signal rectification and averaging behavior of the post-demodulation low-pass filter, neither of which are present in a baseband Log Amp.

The proofs for above assertions are given here for completeness; to our knowledge they have not been previously published. For the sine case, we can write Eq. 9.3.1 in the form

$$V_W = V_Y \, lgt \{(E \sin \theta)/V_Z\} \qquad \text{Eq. 9.3.9}$$

where V_W remains the *instantaneous* value of the output, E is the amplitude of the sine input and θ is the angle, more usually written as a time function ωt. However, for a demodulating Log Amp, we are concerned with the *average value* of V_W , that is, the output of the post-demodulation filter.

We can avoid the mathematical nuisance of dealing with negative logarithmic arguments by just considering the behavior of Eq. 9.3.9 over the range for which sin θ is positive; in fact, we need only concern ourselves with the range $0 \le \theta \le \pi/2$, since the average over a full period will be simply four times the average over this range. (This assumes the use of exact full-wave rectification in the demodulator parts of the Log Amp. The theory is unchanged for half-wave operation, but will be modified by the inexact behavior of typical demodulation circuits, particularly at low signal levels. We will return to this topic when discussing specific Log Amp circuits in detail.)

The demodulated and filtered output is

$$AVE\,(V_W) = \frac{2}{\pi}\int_0^{\pi/2} V_Y\ lgt\ \{(E \sin\theta)/V_Z\}\,d\theta \qquad \text{Eq. 9.3.10}$$

$$= \frac{2V_Y}{\pi}\int_0^{\pi/2} \{lgt\,(\sin\theta) + lgt\,(E/V_Z)\}\,d\theta$$

$$= \frac{2V_Y}{\pi\ ln(10)}\int_0^{\pi/2} \{ln\,(\sin\theta) + ln\,(E/V_Z)\}\,d\theta$$

The definite integral of $ln(\sin\theta)$ over the range of interest is $-(\pi/2)\ ln\ 2$ and the complete integral yields

$$AVE\,(V_W) = \frac{2V_Y}{\pi\ ln(10)}\{-(\pi/2)\ ln\ 2 + (\pi/2)\ ln\,(E/V_Z)\}$$

$$= \frac{V_Y}{ln(10)}\{ln\,(E/V_Z) - ln\ 2\} \qquad \text{Eq. 9.3.11}$$

$$= V_Y\ lgt\,(E/2V_Z) \qquad \text{Eq. 9.3.12}$$

Simply stated, the response to a sine *amplitude* of E would be the same as for a *constant* DC input of E/2, that is, the entire logarithmic transfer function (Figure 9.3.1) is shifted to the right by 6.02 dB. The form of Eq. 9.3.11 deserves further attention. Inside the brackets we have the difference between a log term with the "standard argument" E/V_Z and a second term, in this

case *ln*(2), which is a function of the waveform, in the case, sinusoidal. This term can be viewed as a *waveform signature.*

Using a similar approach for the triwave input, we can write

$$V_W = V_Y \; lgt \{ (E / V_Z)(4t / T) \} \qquad \text{Eq. 9.3.13}$$

to describe the instantaneous output, where E is the amplitude of a triwave of period T. The demodulated and filtered output is now

$$AVE\,(V_W) = \frac{4}{T} \int_0^{T/4} V_Y \; lgt\,(4E\,t / V_Z\,T)\,dt \qquad \text{Eq. 9.3.14}$$

$$= \frac{4V_Y}{T} \int_0^{T/4} \{ lgt\,(t) + lgt\,(4E / V_Z\,T) \}\,dt$$

$$= \frac{4V_Y}{T\,ln(10)} \int_0^{T/4} \{ ln\,(t) + \ln\,(4E / V_Z\,T) \}\,dt$$

The integral of *ln*(t) is simply $t\,ln(t) - t$ and the complete integral yields

$$AVE\,(V_W) = \frac{4V_Y}{T\,ln(10)} \{ (T/4)\,ln\,(T/4) - T/4 + (T/4) \ln\,(4E / V_Z\,T) \}$$

$$= \frac{V_Y}{ln(10)} \{ ln\,(E/V_Z) - 1 \} \qquad \text{Eq. 9.3.15}$$

In this case, the "waveform signature" is just 1, and since this may be written as *ln*(e), the output becomes

$$= V_Y \; lgt\,(E/eV_Z) \qquad \text{Eq. 9.3.16}$$

Thus, a triangle wave input will effectively cause the intercept to shift up by a factor of *e*, or 8.69 dB.

For a noise input having a Gaussian PDF with an RMS value of E, the effective intercept is most easily calculated by first reducing the formulation to a generalized form. Thus, the average value, μ, of a variable, x, having a unit standard deviation, which has been subjected to a logarithmic transformation, can be expressed as

$$\mu = \frac{\int_0^\infty e^{-x^2/2}\, ln(x)dx}{\int_0^\infty e^{-x^2/2}\, dx} \qquad \text{Eq. 9.3.17}$$

Note that the variable x represents the *instantaneous* value of the input noise voltage variable (so it's actually, x(t), but the time dimension is an unnecessary complication for this calculation). The numerator and denominator are both standard forms[1]:

$$\int_0^\infty e^{-\alpha x^2}\, ln(x)dx = (\gamma + ln\, 4\alpha)\, \sqrt{\pi/4\alpha}$$

where γ is Euler's constant, and

$$\int_0^\infty e^{-\alpha x^2}\, dx = \sqrt{\pi/4\alpha}$$

Hence

$$\mu = (\gamma + ln\, 2)/4$$

which evaluates to *ln*(1/1.887).

Therefore, the average value of the logarithmic output in response to a Gaussian input of "unit" RMS value is equivalent to a "DC" input of 1/1.887, that is

$$AVE(V_W) = V_Y\, lgt\, (E_{RMS}/1.887V_Z) \qquad \text{Eq. 9.3.18}$$

1 "Tables of Integrals, Series and Products", I.S. Gradshteyn and I.M. Ryzhik, Academic Press, 1980; Art 3.321.3 (page 307) and Art 4.333 (page 574)

This corresponds to an upward intercept shift of 5.52 dB. It is interesting to note that this is only 0.5 dB different from the calibration for a sinewave input, and it is quite likely to be ascribed to measurement error in the evaluation of the noise performance of practical Log Amps. These results have been carefully verified using the AD640 Log Amp.

9.3.5 THE TRANSLINEAR LOG AMP

Logarithmic converters intended for use at DC or low frequencies generally use a *translinear* technique. The term refers to the remarkably exact logarithmic relationship between the collector current I_C and the base-emitter voltage V_{BE} in a bipolar junction transistor (BJT). This simple fact has profound consequences in the design of analog bipolar circuits. Most importantly, it results in the transconductance being linear with I_C. This interesting but seemingly prosaic property is actually at the heart of the behavior of inumerable circuits, and is important enough to deserve the special term.

Reduced to essentials, this relationship can be written as

$$V_{BE} = V_T \, ln \{ I_C/I_S + 1 \} \qquad \text{Eq. 9.3.19}$$

where I_S is a basic scaling parameter for the BJT, called the saturation current. It is never *accurately* known for design purposes and is a strong function of temperature, roughly doubling every 8 °C. Furthermore, there is a direct dependence of the thermal voltage $V_T = kT/q$ on temperature. So it might first seem that the use of this aspect of BJT behavior in accurate logarithmic conversion circuits is unpromising. As we shall see, the concept can be developed to a considerable degree of refinement.

First, let's convert Eq 9.3.19 to base-10 logarithms to bring it into line with our Log Amp theme:

$$V_{BE} = V_Y \, lgt \{ (I_C + I_S)/ I_S \} \qquad \text{Eq. 9.3.20}$$

where

$$V_Y = V_T \, ln(10) \qquad \text{Eq. 9.3.21}$$

Thus, the logarithmic slope V_Y is proportional to absolute temperature (PTAT). It evaluates to 59.5 mV/decade at T = 300 K. The logarithmic intercept is simply the saturation current, I_S, typically between 10^{-17} and 10^{-15} Amperes at room temperature. Note that the "signal" input I_C is augmented by this tiny current; we later address the consequences of this slight anomaly in the otherwise straightforward Log Amp form of the equation.

It is important to note that V_{BE} bears this valuable relationship to the *collector* current. The finite beta of the transistor has no effect on the accuracy of these equations, although more will be said about this later. Some texts have erroneously ascribed errors in logarithmic converters of this type to the current-dependence of beta, by starting with expressions for V_{BE} that are functions of the *emitter* current I_E. Note that a current-driven *diode-connected* transistor would exhibit anomalies in logarithmic behavior due to this effect.

THE PATTERSON OR TRANSDIODE LOG AMP

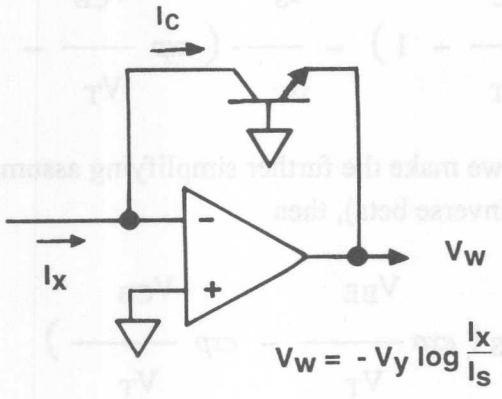


Figure 9.3.5

Figure 9.3.5 shows a typical scheme to force I_C to equal I_X, the signal current. This is sometimes called a "transdiode connection" or "Paterson diode". We show here the usual NPN form, but it is obvious that use of a PNP transistor would simply reverse the required polarity of input current and the resulting polarity of output voltage. In practice, monolithic PNP transistors of sufficient quality are only available in a few complementary bipolar processes.

The op-amp forces the collector current of the transistor to equal the input current I_X while maintaining its collector-base voltage very close to zero. The $V_{CB} = 0$ condition is not essential: for *most* purposes little harm will result if the collector junction is strongly reversed-biased (this effectively increases I_S), or even becomes slightly forward biased. Later, we will show that it is actually advantageous to use a specific value of reverse collector bias ($V_{CB} \approx +100$ mV) in certain applications.

The logarithmic output is taken from the emitter node, and the op-amp allows this to be loaded quite heavily while preserving accuracy. In most cases, I_S will be much less than I_X and, replacing I_C by I_X we can simplify Eq. 9.3.20 to

$$V_W = -V_Y \, lgt \, (I_X / I_S) \qquad \text{Eq. 9.3.22}$$

9.3.5.1 ERRORS AT HIGH TEMPERATURE

In the special case of operation at high temperatures and very low currents, the simplification used in Eq. 9.3.22 is inappropriate, since I_S is now roughly comparable with the input current. Eq. 9.3.20 correctly predicts that V_{BE} should approach zero as I_C approaches zero, for any I_S. However, the departure from a strictly logarithmic response in this region can be corrected by using a particular reverse bias at the collector. To understand this, we need to go back to the

basic Ebers-Moll modeling of collector current. For a transistor having a forward alpha α_F close to unity

$$I_C = I_S\left(exp\frac{V_{BE}}{V_T} - 1\right) - \frac{I_S}{\alpha_R}\left(exp\frac{-V_{CB}}{V_T} - 1\right) \qquad \text{Eq. 9.3.23a}$$

where α_R is the inverse alpha. If we make the further simplifying assumption at this point that α_R is also is close to unity (high inverse beta), then

$$I_C = I_S\left(exp\frac{V_{BE}}{V_T} - exp\frac{-V_{CB}}{V_T}\right) \qquad \text{Eq. 9.3.23b}$$

Now, when $V_{CB} = 0$ this reduces to the expression from which Eq. 9.3.19 follows directly, but when the collector is strongly reverse-biased the second terms vanishes, and Eq. 9.3.22 becomes exact. Even for modest amounts V_{CB} of the second term quickly becomes negligible.

At this point an interesting observation can be made. For the practical case of α_R less than unity, there is a unique value of V_{CB} to achieve exactly logarithmic operation. This is easily shown from Eq.9.3.23a to be

$$V_{CB} = V_T\, ln\,(1 - \alpha_R) \qquad \text{Eq. 9.3.24}$$

For an α_R of 0.5 the ideal V_{CB} would be $V_T\, ln\,(2)$, or 24.9 mV at T = 150 °C; for $\alpha_R = 0.8$ it would be 58.7 mV.

For a given monolithic process, α_R is quite consistent, so it would be an easy matter to provide the correct PTAT voltage required by Eq. 9.3.24 to ensure accurate operation right down to, and beyond, the theoretical intercept. This voltage is not particularly critical and may be introduced either at the op-amp non-inverting input node or at the base of the transistor. In the first case, by elevating the voltage at the summing node it might cause errors in the input current I_X if this does not originate from a perfect current-source.

Even the few millivolts of V_{OS} of a MOS-input op-amp could create serious errors due to leakage resistance from the input node to ground. The relatively large 60 mV "inverse-alpha fix" across a leakage resistance of 100 MΩ would cause an error in I_X of 600 pA. Guarding is essential to prevent leakage paths to even more hazardous bias sources, such as the supplies. In the second case, the correction voltage would not affect the summing node potential, but would slightly alter the output voltage.

Remember, these details are only of importance in Log Amps which must operate accurately with picoampere inputs and at high temperatures. We of course assume that the op-amp has extremely small input currents, using a junction FET or MOS input stage.

9.4 LOG-AMP DESIGN

9.4.1 THE PROGRESSIVE COMPRESSION LOG-AMP

Almost without exception, high-frequency log-amps distribute their total dynamic range over many stages, each of which has low gain, and they achieve their function through a process of *progressive compression*. The theory is not especially well developed in the literature, particularly with regard to the all-important matter of scaling, that is, a comprehensive consideration of the fundamentals on which the accuracy of this nonlinear function depend. In developing a theory from first principles, we will be paying close attention to this topic.

We begin with the "target" function

$$\mathbf{V_W} = V_Y \log(\mathbf{V_X}/V_Z) \qquad \text{Eq. 9.4.1}$$

where $\mathbf{V_W}$ is the output voltage, $\mathbf{V_X}$ is the input voltage, V_Y will be called the *slope* voltage and V_Z the *intercept* voltage. Note at the outset that we are careful to use variables of the correct dimensions (all voltages, in this case) throughout. Since at this point we're considering *baseband* (non-demodulating) log-amps, $\mathbf{V_X}$ and $\mathbf{V_W}$ (shown in **bold** throughout this section to differentiate them from constants and internal voltages) are the *instantaneous* values of the input and output. The choice of logarithmic base is arbitrary; to preserve generality, it is not defined in Eq. 9.4.1. A change of base merely results in a change in V_Y. Later, we will use base-10 logarithms, in keeping with the decibel-oriented context.

THE LOGARITHMIC TRANSFER FUNCTION

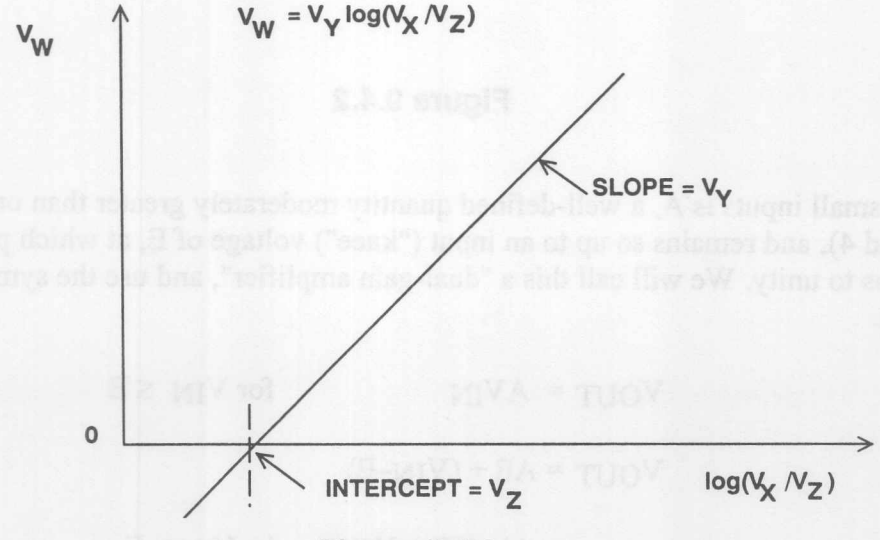


Figure 9.4.1

Figure 9.4.1 shows a plot of this function, Our objective is to find the scaling parameters V_Y and V_Z for specific circuits, of increasing complexity, as a foundation for a full theory of demodulating logarithmic amplifiers.

Imagine an amplifier stage having the DC transfer function shown in Figure 9.4.2. For the time being, we will be concerned only with its response to positive inputs, but the theory is completely applicable to a symmetrical response. Throughout this analysis, we will not be concerned with frequency-dependent aspects of the amplifier.

DC TRANSFER FUNCTION OF A DUAL-GAIN AMPLIFIER SECTION

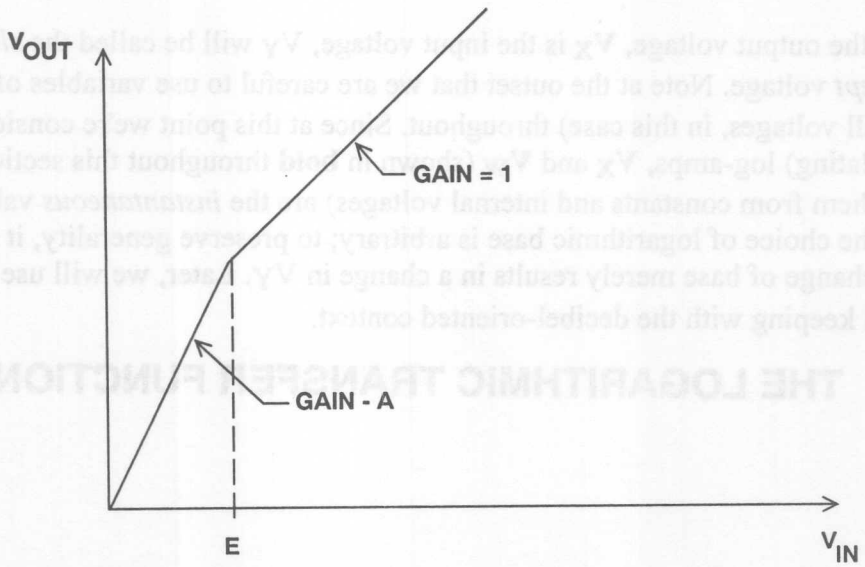


Figure 9.4.2

The gain for small inputs is A, a well-defined quantity moderately greater than one (typically between 2 and 4), and remains so up to an input ("knee") voltage of E, at which point the gain abruptly drops to unity. We will call this a "dual-gain amplifier", and use the symbol A/1 in the figures. Thus

$$V_{OUT} = AV_{IN} \qquad \text{for } V_{IN} \leq E \qquad \text{Eq. 9.4.2a}$$

and

$$V_{OUT} = AE + (V_{IN}-E)$$

$$= (A-1)E + V_{IN} \qquad \text{for } V_{IN} > E \qquad \text{Eq. 9.4.2b}$$

Without any analysis, we can immediately reach some conclusions about the behavior of a log-amp built from a series-connected set of such amplifier sections.

First, because the transfer function just defined is piecewise-linear, it follows that the overall function, although more complicated, can never be anything but a piecewise-linear approximation. Clearly, the more stages of lower gain that are used to cover a given dynamic range, the closer this approximation can be; put another way, we can expect the approximation error to be some increasing function of the gain stage, A. We will find later that practical circuits, having a softened gain transition, or even gain which varies continuously with V_{IN}, can provide arbitrarily close approximations to a true logarithmic response.

Second, we can be certain that the logarithmic slope V_Y and intercept V_Z in the target function must both be *directly proportional* to the knee voltage, E, that is, we can expect them to have the general form

$$V_Y = y\,E$$

and

$$V_Z = z\,E$$

where y and z are some functions of A and (certainly in the case of the intercept) N which control the magnitude of the slope and intercept, respectively. We can predict this simple proportionality with total assurance, because if some polynomial in E were needed, there would have to be other parameters with the dimension of voltage to restore dimensional consistency, that is, we cannot blithely propose something like

$$V_Y = a_1E + a_2E^2 + a_3E^3 \ .....$$

without giving due thought to where the coefficients of the higher-order terms in E derive *their* dimensionality[1].

The immediate challenge, then, is to find the functions y and z for the cascade of N dual-gain amplifier sections shown in Figure 9.4.3. This turns out to be easier that might at first seem; the reader is encouraged to follow this analysis through, step by step, because it provides a firm foundation for understanding all classes of log-amps using piecewise-linear progressive compression methods.

9

[1] The reader is urged to apply this type of reasoning, and constant vigilance to matters of scaling, in the development or application of any nonlinear analog processing block. It is usually risky (although occasionally unavoidable) to use "constants" in which dimensional quantities are embedded.

A BASEBAND LOG AMP COMPRISING A CASCADE OF DUAL-GAIN AMPLIFIER SECTIONS

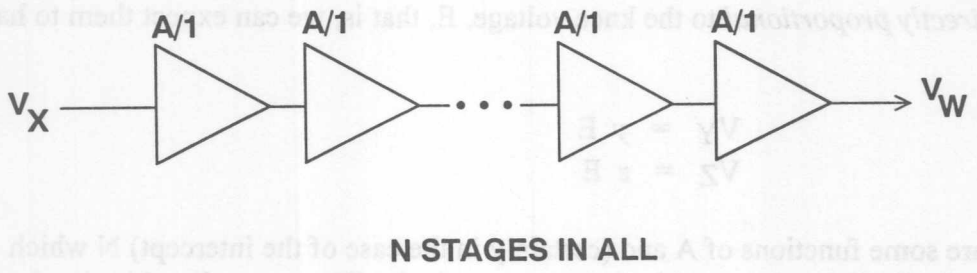


Figure 9.4.3

The overall input is labeled V_X and the output V_W in observance of the nomenclature used in the target function of Eq 9.4.1. For very small inputs, the overall gain is simply A^N. At a critical value of V_X, the input to the last (N-th) stage reaches its knee voltage, E. Since the gain of the preceding N–1 stages is A^{N-1}, this must occur at a voltage

$$V_X = E/A^{N-1}$$

This is sometimes called the "lin-log" transition, because for smaller inputs the cascade is simply a linear amplifier, while for larger inputs it enters a region of approximately logarithmic behavior. Above this point, the overall incremental gain falls to A^{N-1}. As the input is raised further, a second critical point is reached, when the input to the (N–1)-th stage reaches *its* knee. Then

$$V_X = E/A^{N-2}$$

which is simply A times larger than the first critical voltage. We can call this the first "mid-log" transition. Above this point, the incremental gain falls by a further factor of A, to A^{N-2}, and so on.

It will be apparent that the cascade is characterized by a total of N transitions, the last occurring at V_X = E. Figure 9.4.4 shows the voltages at all exposed nodes in this system at all the transition points.

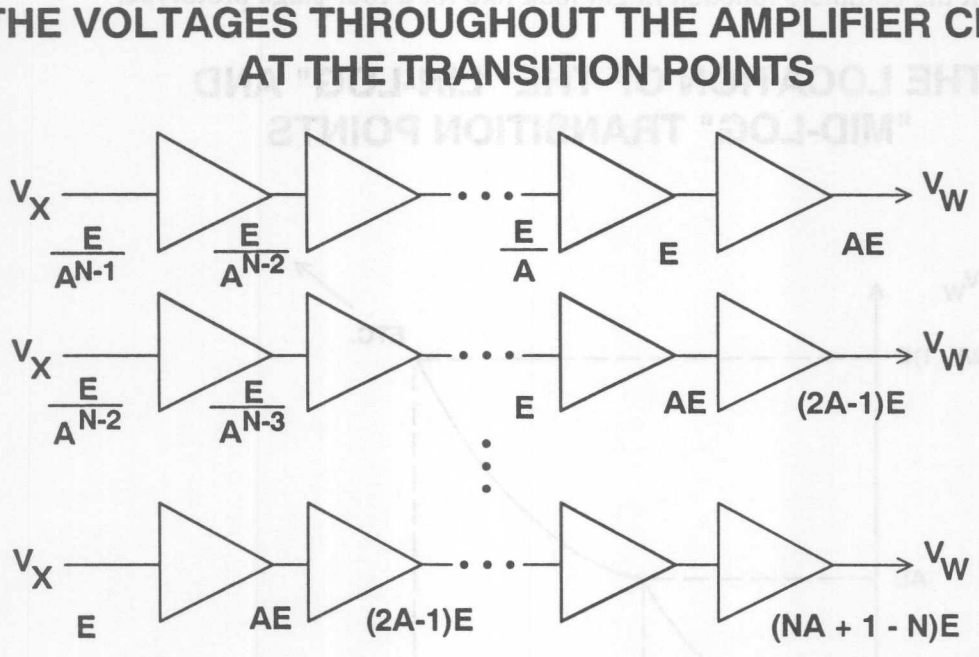


Figure 9.4.4

The key point here is that these transitions are at voltages separated by a *constant ratio*, equal to the gain A of each amplifier section. This already looks promising, since if V_X is represented along a logarithmic axis, these transitions occur at equal linear increments.

The next step is to find the corresponding values of V_W for all intervals above the lin-log transition and up to V_X = E. Eq. 9.4.2b can quickly adapted for the first interval:

$$V_W = (A-1)E + V_N \qquad \text{Eq. 9.4.3}$$

where V_N is the input to the N-th stage. Precisely at the lin-log transition, V_N = E, and therefore V_W = AE. Up to the second transition, V_N is just $V_X A^{N-1}$, so for the interval between the lin-log transition and the first mid-log transition,

$$V_W = (A-1)E + V_X A^{N-1} \qquad \text{Eq. 9.4.4}$$

We can use this starting point to find an expression for V_W for all values of V_X. However, we really don't need to delineate all possible values of V_W, since our aim at this juncture is just to find the effective slope and intercept of the overall piecewise-linear function. This task will be aided by using Figure 9.4.5, which shows the critical points and their coordinates, with an estimate of what the complete function might look like for a four-stage prototype.

THE LOCATION OF THE "LIN-LOG" AND "MID-LOG" TRANSITION POINTS

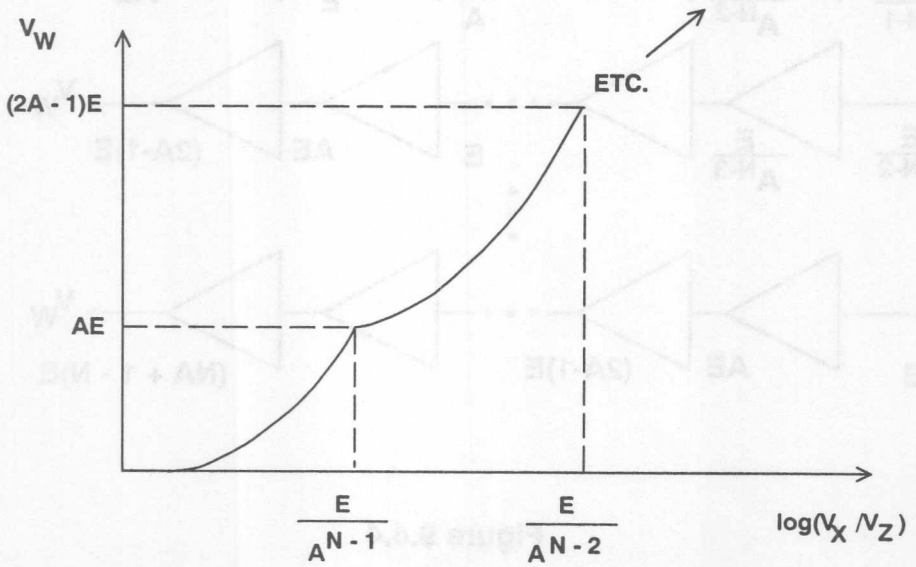


Figure 9.4.5

Right at the first mid-log transition, the output of the (N–1)-th stage is simply AE, so the output of the next stage, which is also the final output, is, from Eq. 9.4.4,

$$V_W = (A–1)E + AE$$

$$= (2A–1)E \qquad \text{Eq. 9.4.5}$$

So the output increased from AE to (2A–1)E, an amount (A–1)E, for a *ratio* change of A in V_W. Continuing this line of reasoning, we can demonstrate that at the next transition $V_W = (3A–2)E$, and so on: ***the change in V_W is always by the fixed amount (A–1)E as V_X increases by each factor of A.***

Now, a "factor of A" can be stated as "some fractional part of a decade"; but that is just *lgt*A, where *lgt* denotes "logarithm to base 10". For example, a ratio of 4 is slightly over six-tenths of a decade, since *lgt*4 = 0.602.

We can therefore state that the slope of the output function, corresponding to a line drawn through all the transition points, is

$$V_Y = \frac{\text{Absolute voltage change in } V_W}{\text{Ratio change in } V_X} = \frac{(A-1)E}{lgtA} \qquad \text{Eq. 9.4.6}$$

As expected, is V_Y proportional to E. What may be a little surprising is that the slope is unaffected by the number of stages, N.

Since we are now using base-10 logarithms V_Y can in this case be read as "Volts per decade", but it will be more generally referred to as the "Slope voltage", because any base may be used in the formal function of Eq. 9.4.1.

To determine the intercept, we need only to insert one point into the target equation and use the known value of slope. We can conveniently choose the lin-log transition, at which point $V_X = E/A^{N-1}$ and $V_W = AE$. Thus

$$AE = \frac{(A-1)E}{lgtA} \; lgt \left\{ \frac{E}{V_Z A^{N-1}} \right\} \qquad \text{Eq. 9.4.7}$$

which solves to

$$V_Z = \frac{E}{A^{N + 1/(A-1)}} \qquad \text{Eq. 9.4.8}$$

N finally makes an appearance in the expression for the intercept! And, as we should expect, for each added stage this intercept just moves to the left (in Figure 9.4.5), to a voltage A times lower. Our original task has therefore been accomplished. There remain only a few loose ends before we are ready to design a practical baseband log-amp along these lines. But before proceeding, let us apply "sanity checks" to the results so far.

Suppose A = 4, N = 8 and E = 1 V. We only have a dim idea at this point that these might be suitable numbers, but they can be roughly rationalized in the following way: a gain of 4 for each section is consistent with high accuracy and wide bandwidth in a simple amplifier cell; using 8 stages and this gain, the useful dynamic range will be of the order of 4^8 which corresponds to 96dB; E = 1 V is just a starting-point.

With these figures, the slope works out to about 5 V per decade and the intercept is about 10 μV. Clearly, in a practical amplifier handling several decades and operating within the constraints of typical supplies, a lower value of E would be required. Figure 9.4.6 shows the simulated output of an 8-stage system. for which E = 392.7 mV and A = 4.145, choices relating to a particular practical design not presented here. The scale is 2 V per decade, a convenient 100 mV/dB; the

intercept is at 2.86 μV. Note that the intercept could readily be shifted to 10 μV by the simple expedient of including a ×3.5 attenuator ahead of the log-amp's input.

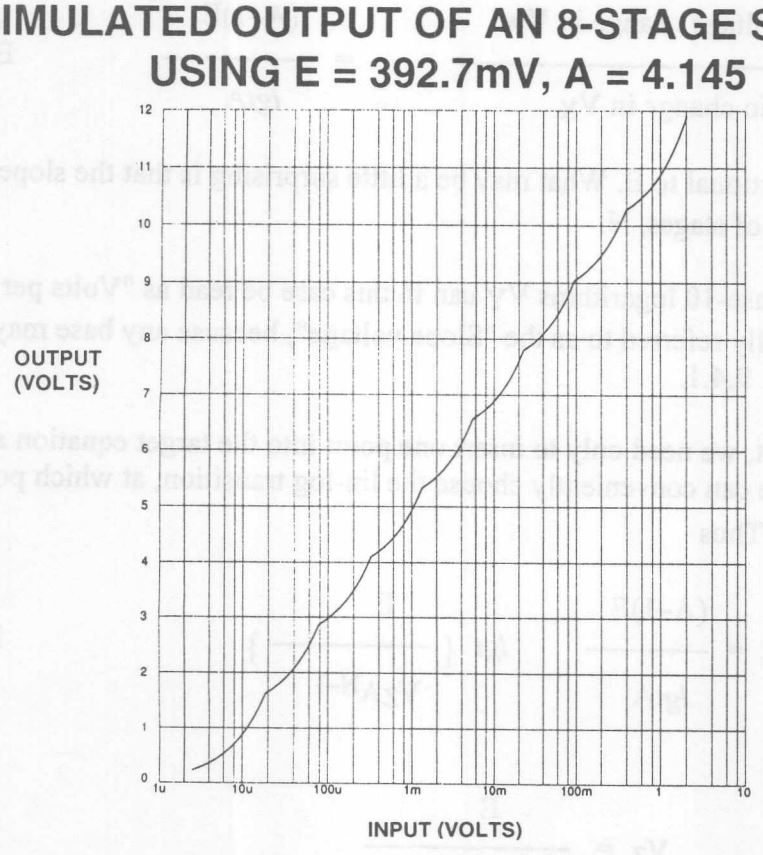


Figure 9.4.6

9.4.2 DYNAMIC RANGE, MAXIMUM OUTPUT AND PEAK ERROR

At inputs much below the lin-log transition at $V_X = E/A^{N-1}$ or much above the top transition, at $V_X = E$,corresponding to a dynamic range of A^{N-1}, the deviation of the piecewise-linear approximation from the ideal logarithmic line rapidly becomes excessive. However, examination of the transfer function in Figure 9.4.6 quickly reveals that it extends to at least a factor of A above and below these outer transition points. Thus, the practical dynamic range is actually rather more than A^{N+1}, depending on the allowable error at the extremities of the range.

Beyond the top transition, the output can readily be shown to be

$$V_W = N(A-1)\,E + V_X \qquad \text{Eq. 9.4.9}$$

Thus, in our example, the output at $V_X = 2$ V is 11.88 V, a value consistent with a traditional IC op-amp context, although not appropriate to RF log-amps. Figure 9.4.7 shows the error

computed by subtracting the ideal output from the actual output and presenting the result in equivalent decibels:

$$Error_{dB} = 20 \{ V_W/V_Y - lgt\,(V_X/V_Z) \} \qquad \text{Eq. 9.4.10}$$

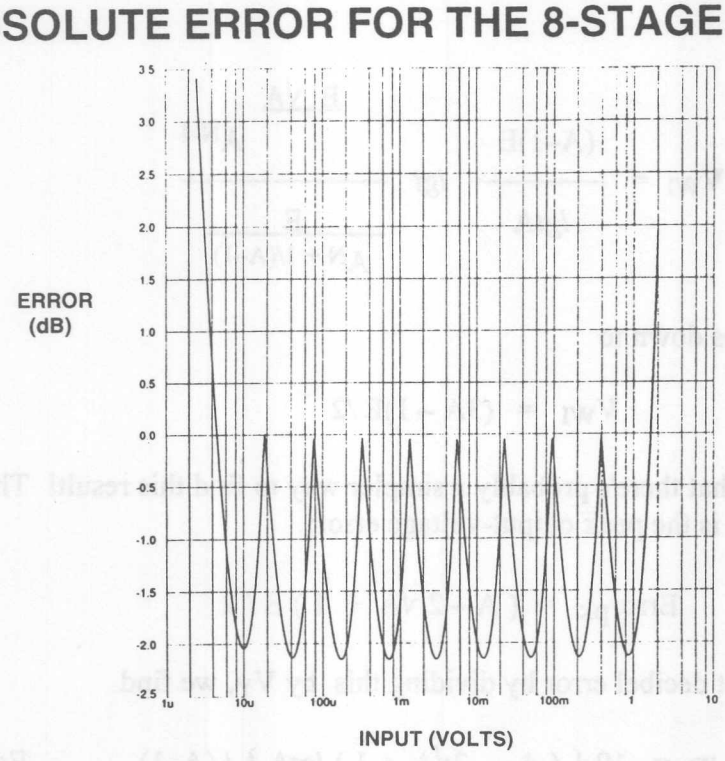


Figure 9.4.7

Rigorous analysis of the ripple is straightforward, but the solution lacks immediate impact. An alternative is presented here which makes only the assumption that the maximum deviation occurs at the mid-point between the transitions, that is, at an input level $\sqrt{A}$ greater than the lower point of any interval, which of course is also a factor $\sqrt{A}$ below the upper point.

The first of these mid-points occurs between the lin-log transition and the first mid-log transition, in other words, at

$$V_X = E/A^{N-1}\sqrt{A} \qquad \text{Eq. 9.4.11}$$

at which point the *actual* output is

$$V_{WA} = E\,(A + \sqrt{A} - 1) \qquad \text{Eq. 9.4.12}$$

The *ideal* output is

$$V_{WI} = V_Y \, lgt(V_X/V_Z)$$

which, for this particular input and using the complete values for V_Y and V_Z from Eqs. 9.4.6 and 9.4.8 respectively, is

$$V_{WI} = \frac{(A-1)E}{lgtA} \, lgt \, \frac{\dfrac{E\sqrt{A}}{A^{N-1}}}{\dfrac{E}{A^{N+1/(A-1)}}} \qquad \text{Eq. 9.4.13}$$

The fact that this simplifies down to

$$V_{WI} = (3A - 1)E/2$$

should lead us to suspect that there's probably a simpler way to find this result! The difference between V_{WA} and V_{WI} is the peak output-voltage error:

$$Error_{pk} = (A - 2\sqrt{A} + 1)E/2 \qquad \text{Eq. 9.4.14}$$

Converted to its equivalent decibel error by dividing this by V_Y, we find

$$Error_{pk\,dB} = 10\{(A - 2\sqrt{A} + 1)\,lgtA\}/(A-1) \qquad \text{Eq. 9.4.15}$$

As might be expected, *the error expressed in decibels is dependent only on the stage gain* A. For A = 4.145, the value used to generate the error plot of Figure 9.4.7, this evaluates to 2.11dB, in excellent agreement with that simulation. Other values are 0.52 dB for A = 2, 1 dB for A = 2.65, 1.40 dB for A = $\sqrt{10}$, 1.72 dB for A = 3.6 and 2 dB for A = 4. Using more practical amplifier transfer functions, having continuously-varying gain as a function of their input voltage, the error ripple is much lower in amplitude and roughly sinusoidal in form, rather than parabolic as in this case.

Numerous circuit arrangements are possible to implement a near-ideal dual-gain stage at low frequencies. However, an even simpler topology, eminently suitable for monolithic integration (in a somewhat revised form) can achieve precisely the same function, and, in practice, equal or better accuracy.

9.4.3 LOG-AMPS USING AMPLIFIER/LIMITER STAGES

A somewhat different approach uses an amplifier-limiter stage, for which the gain remains A for small signals, but drops to *zero* for inputs above the knee voltage, E. This can be called an amplifier/limiter stage, and denoted on the figures by the symbol A/0. Figure 9.4.8 shows the transfer function of this stage; in this case, we have chosen to show the symmetry of the response to inputs of either polarity, because we'll be making use of this later. The basic equations are

$$V_{OUT} = AV_{IN} \qquad \text{for } -E \le V_{IN} \le E \qquad \text{Eq. 9.4.16a}$$

$$V_{OUT} = AE \qquad \text{for } V_{IN} > E \qquad \text{Eq. 9.4.16b}$$

and

$$V_{OUT} = -AE \qquad \text{for } V_{IN} < -E \qquad \text{Eq. 9.4.16c}$$

DC TRANSFER FUNCTION OF AN AMPLIFIER/LIMITER SECTION

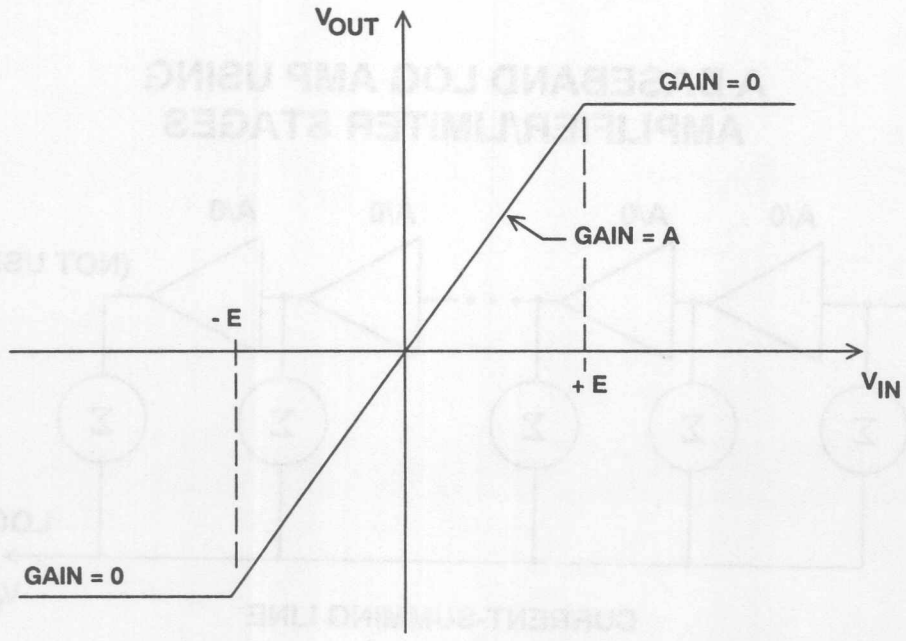


Figure 9.4.8

As before, a logarithmic function will be synthesized using the piecewise-linear behavior of a cascade of N stages, first to realize a baseband log-amp and later in a demodulating log-amp. We will establish the theory for idealized stages having abrupt limiting, then adapt it to more realistic wideband circuit cells, which have "soft" limiting and a knee voltage which is a strong function of temperature, so that special means are required to stabilize the scaling attributes.

Figure 9.4.9 shows the general structure of a baseband log-amp made up of N such A/0 stages. Now, it will immediately be apparent that we can no longer just use the output of the *final* stage, since as soon as this stage goes into limiting, which happens when $V_X = E/A^{N-1}$, the output will simply limit at AE and be unable to respond to further increases in V_X.

Instead, *the outputs of all stages must be summed*, usually, though not necessarily, with equal weighting, to form the logarithmic output V_X. This only slightly complicates the mathematics, and having conquered the analysis of the A/1 cascade, we should not have too much difficulty in tackling this new situation. As before, the approach will be to methodically work toward finding the basic scaling parameters V_Y and V_Z in the transfer function

$$V_W = V_Y \log (V_X/V_Z) \qquad \text{(quoting Eq. 9.4.1)}$$

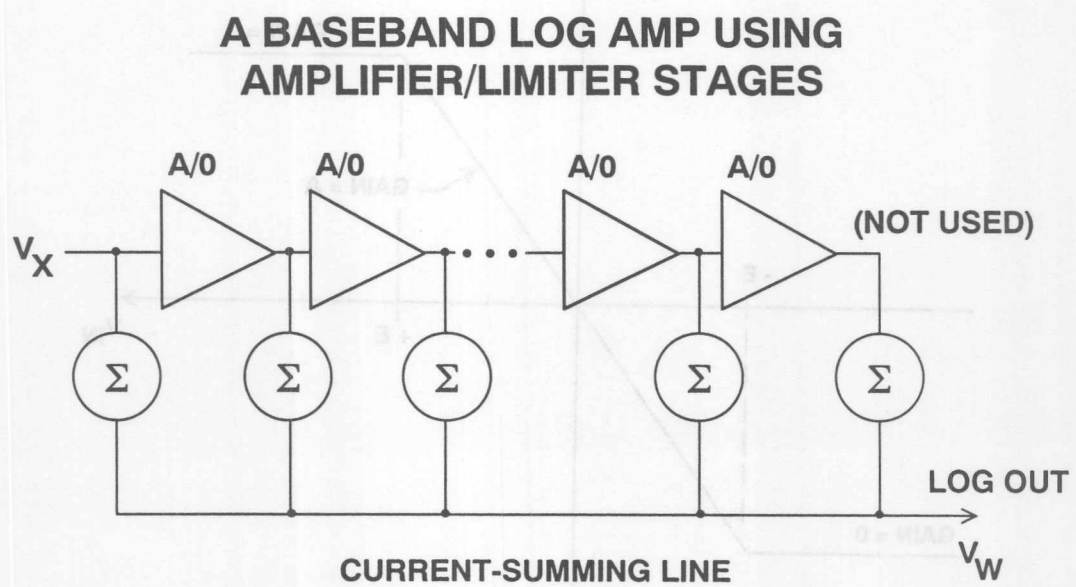


Figure 9.4.9

We are now well-enough informed to know that the slope voltage V_Y and the intercept voltage V_Z must both be simply proportional to E.

For very small values of input, the gain to the output of the k-th stage is simply A^k. At a critical value of V_X, the input to the N-th stage reaches its knee voltage, E. Since the gain of the first N–1 stages is A^{N-1}, this must occur at a voltage

$$V_X = E/A^{N-1}$$

We earlier called this the "lin-log" transition, because for smaller inputs the cascade behaves a linear amplifier, while for larger inputs it becomes pseudo-logarithmic. As the input is raised further, a second critical point is reached, when the input to the (N–1)-th reaches its knee.

This happens when

$$V_X = E/A^{N-2}$$

which is just A times larger than the first critical voltage. This the first "mid-log" transition. Just as for the cascade of A/1 stages, this system is characterized by a total of N transitions, the last occurring at $V_X = E$, and therefore the milestones along the log-input axis are at exactly the same values of V_X. As before, these transitions are at voltages separated by a *constant ratio*, equal to the gain A of each amplifier section.

Now we have to find the corresponding values of the output V_W for all values of input V_X up to, and slightly beyond, E. For small inputs, below the lin-log transition, and for equal weighting of the limiter outputs

$$V_W = A^N V_X + A^{N-1} V_X + \ldots\ldots\ldots\ldots\ldots + V_X$$

$$= (A^N + A^{N-1} + \ldots\ldots\ldots\ldots + 1)\, V_X \qquad \text{Eq. 9.4.17}$$

Precisely at the lin-log transition

$$V_W = (A^N + A^{N-1} + \ldots\ldots\ldots\ldots + 1)\, E/A^{N-1}$$

$$= (A + 1 + \ldots\ldots\ldots\ldots + 1/A^{N-1})\, E \qquad \text{Eq. 9.4.18}$$

At the first mid-log transition

$$V_W = (A + A + 1 + \ldots\ldots\ldots + 1/A^{N-2})\, E \qquad \text{Eq. 9.4.19}$$

Between these two inputs, the output has changed by

$$\Delta V_W = (A - 1/A^{N-2}) E$$

while the input increased by a factor A, or *lgt*A decades. Thus, the slope for this first interval, measured on the transition coordinates, is

$$V_{Y1} = \frac{(A - 1/A^{N-2}) E}{lgt A} \qquad \text{Eq. 9.4.20}$$

For typical values of A and N, this is very close to AE/*lgt*A.

At the second mid-log transition

$$V_W = (A + A + A + 1 + \ldots\ldots + 1/A^{N-3}) E \qquad \text{Eq. 9.4.21}$$

So over this interval the slope is

$$V_{Y2} = \frac{(A - 1/A^{N-3}) E}{lgt A} \qquad \text{Eq. 9.4.22}$$

Again, for typical values of A and N, this remains close to AE/*lgt*A. For example, if A = 4 and N = 8, the exact value of V_{Y2} is 6.6422E while the "simplified" value is 6.6438E. It is therefore reasonable to use the expression

$$V_Y = \frac{AE}{lgt A} \qquad \text{Eq. 9.4.23}$$

for the slope of this log-amp over the entire lower portion of its dynamic range. At the top transition V_W = NAE while at the penultimate transition

$$V_W = \{ (N-1) A + 1 \} E \qquad \text{Eq. 9.4.24}$$

so the slope between the two *uppermost* transitions is

$$V_{YN} = \frac{(A - 1) E}{lgt A} \qquad \text{Eq. 9.4.25}$$

which is the same value as for the cascade of A/1 stages, while the next pair from the top have a slope

$$V_{YN-1} = \frac{(A - 1/A)\,E}{lgt A} \qquad \text{Eq. 9.4.26}$$

Thus, we conclude that there is a slight reduction in the slope over the last few transition intervals, that is, at the top end of the dynamic range. As we shall see in just a moment, this artifact can be corrected, and the top-end logarithmic conformance in a high-accuracy design can thereby be improved, by simply using a higher summation weighting on the output from the first stage.

To determine the intercept, we follow the procedure used earlier, and insert one input/output point into the target equation and use the known value of slope. As before, we can use the lin-log transition, at which point $V_X = E/A^{N-1}$ and

$$V_W = (A + 1 + \ldots\ldots + 1/A^{N-1})\,E \qquad \text{(quoting Eq. 9.4.18)}$$

Thus

$$(A + 1 + \ldots\ldots + 1/A^{N-1})\,E = \frac{AE}{lgt A}\, lgt \left\{\frac{E}{V_Z A^{N-1}}\right\} \qquad \text{Eq. 9.4.27}$$

Multiplying both sides by (A–1)/A and reducing

$$A + 1/A^N = \frac{A-1}{lgt A}\, lgt \left\{\frac{E}{V_Z A^{N-1}}\right\} \qquad \text{Eq. 9.4.28}$$

This equation is almost identical with Eq. 9.4.7 and for practical purposes has the same solution

$$V_Z = \frac{E}{A^N + 1/(A-1)} \qquad \text{(Eq. 9.4.8)}$$

The simulated results for an 8-stage system, using ideal A/0 cells, are shown in Figures 9.4.10. The theoretical slope and intercept are 1.661 V and 2.4 μV respectively.

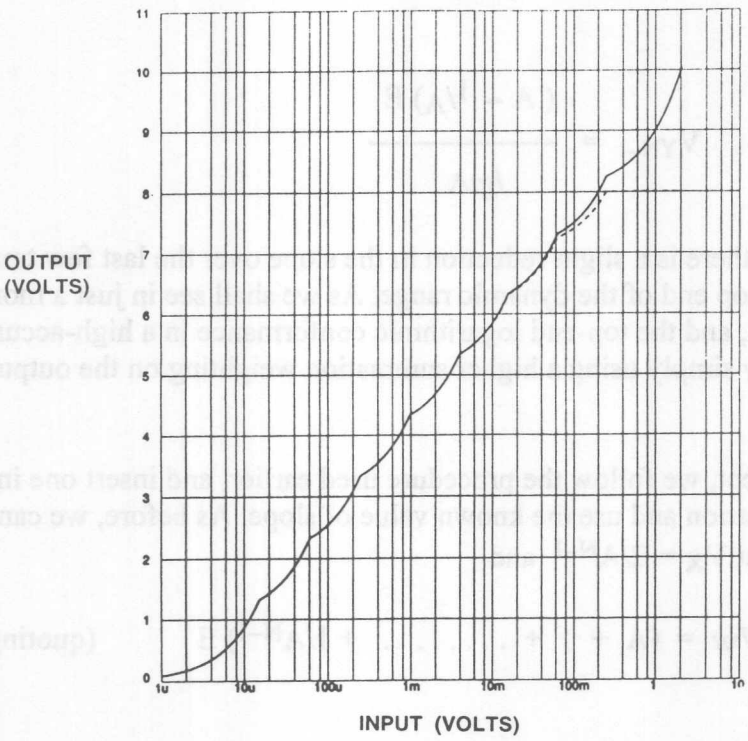


Figure 9.4.10

The ripple calculation for this system follows the same approach as used above and yields essentially identical results, that is

$$\text{Error}_{\text{pk dB}} = 10 \{ (A - 2\sqrt{A} + 1) \, lgt A \} / (A-1) \qquad \text{(quoting Eq. 9.4.15)}$$

For the stage gain of A = 4 used in the above examples, this evaluates to 2 dB.

9.4.3.1 A Nice Trick

Now, supposing that we alter the summation weighting of *just the input term*, from 1 to A/(A–1). Then, at the lin-log transition

$$\begin{aligned} V_W &= \{ (A^N + A^{N-1} + \ldots\ldots + A/(A-1) \} \, E/A^{N-1} \\ &= \{ \quad A \quad + 1 \quad + \ldots\ldots + 1/(A-1)A^{N-2} \} \, E \end{aligned} \qquad \text{Eq. 9.4.29}$$

which collapses to

$$V_W = \{ A^2/(A-1) \} \, E \qquad \text{Eq. 9.4.30}$$

At the first mid-log transition

$$V_W = \{ A + A + 1 + \ldots + A/(A-1)A^{N-2} \} E \qquad \text{Eq. 9.4.31}$$

which reduces to $V_W = \{ (2A^2-A)/(A-1) \} E$ Eq. 9.4.32

Between these two inputs, the output now changes by *exactly*

$$\Delta V_W = AE$$

Thus, the slope for this first interval is now *exactly*

$$V_{Y1} = \frac{AE}{lgtA} \qquad \text{Eq. 9.4.33}$$

By continuing this process it will be found that the difference in V_W between each transition is *now always AE*. In other words, by this simple measure, we have eliminated the annoying variation in slope at the top end of the dynamic range.

9.4.4 SUMMATION VIA G/0 STAGES

Next we need to consider any effects on the mathematics which may arise when the summation is performed by transconductance (*gm*) cells which exhibit similar "amplifier/limiter" behavior as the gain stages.

The use of *gm* stages is appealing, because current-mode signals can be summed by simply connecting the outputs of all stages together; conversion back to voltage form is easily accomplished using a simple resistive load or a transresistance stage. Further, they provide unilateral transmission to this output, minimizing the likelihood of unwanted reverse coupling to sensitive early nodes in the signal path. More importantly, they provide the means to *separate the slope calibration from the parameters which control the behavior of the main amplifier*. This last benefit is central to the scaling of monolithic log-amps using differential bipolar pairs as the gain cells, since their knee voltage is a strong function of temperature (in fact, as shown in Section 9.4.6, it's proportional to absolute temperature, or PTAT) and, as we've learned, it is this voltage that controls the slope in all the structures considered up to this point.

For a *gm* stage, the parameter corresponding to the dimensionless gain A is now the small-signal transconductance G: a voltage input V_K (the signal at any node K) generates a current output, GV_K. In the most general case, the knee voltage at which this *gm* abruptly drops to zero could be different from the corresponding voltage for the A/0 amplifier stage, but we will not pursue that general analysis here because (a) we anticipate that the practical circuit form which will be used for the G/0 stages has exactly the same (PTAT) knee voltage, E, as the A/0 stages and (b) the clarity of the mathematics and the intuitive appreciation of the system behavior are both needlessly impaired by retaining this redundant generality. The maximum output from a G/0

stage (that is, when $V_K \geq E$) is GE, analogous to AE for the gain stage. However, the dimensional change inherent in the *gm* stage means that this peak output is simply a current, which will here be called I_Y (the "Y" referring to the logarithmic slope in Eq. 9.4.1, since it is obvious that it will be this current which controls the slope). Therefore, $I_Y = GE$.

Figure 9.4.11 shows the new scheme. The summed currents from the G/0 stages are converted back to voltage by the resistor R_Y, to which the logarithmic slope is also proportional. It's safe to assume that the basic operation of this system will be similar to that we've encountered already, but we will nevertheless use a step-by-step procedure to put the scaling of this revised form on a firm foundation.

As before, we begin by considering the circumstances at the lin-log transition. The input to the last *gm* stage (numbered N+1) is the output from the N-th amplifier stage, so this first transition now occurs at a system input V_X which is A times lower than in either of the two earlier log-amp structures.

A/0 LOG AMP STRUCTURE USING AUXILLARY G/0 STAGES FOR SUMMATION

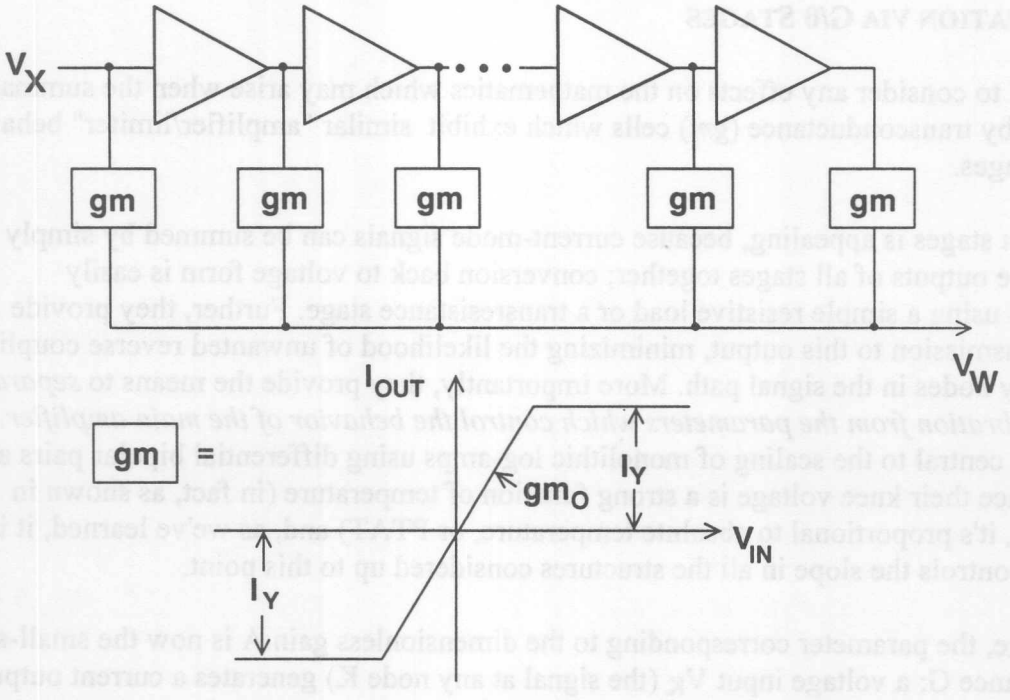


Figure 9.4.11

Thus, at the lin-log transition

$$V_X = E/A^N \qquad \text{Eq. 9.4.34}$$

Summing the outputs of the G/0 stages, starting at the last stage (whose output is the largest) and progressing back to the input stage the output is

$$V_W = R_Y \{ GE + GE/A + \ldots\ldots + GE/A^N \} \qquad \text{Eq. 9.4.35}$$

As previously noted, the product GE is the peak current output I_Y of the G/0 stage, so the repeated products $R_Y GE$ can be contracted to a simple constant scaling voltage $V_S = I_Y R_Y$. Note that this is not yet the slope voltage V_Y of the target equation 9.4.1. Hence, at the lin-log transition

$$V_W = V_S \{ 1 + 1/A + \ldots\ldots + 1/A^N \} \qquad \text{Eq. 9.4.36}$$

The next condition of interest is the first mid-log transition. This occurs when the input to the N-th A/0 stage reaches its knee voltage, E, which is also the voltage at which the N-th G/0 stage reaches this condition. The system input voltage at which this occurs is

$$V_X = E/A^{N-1} \qquad \text{Eq. 9.4.37}$$

and the output at this point is

$$V_W = R_Y \{ GE + GE + GE/A + \ldots\ldots + GE/A^{N-1} \}$$

$$= V_S \{ 1 + 1 + 1/A + \ldots\ldots + 1/A^{N-1} \} \qquad \text{Eq. 9.4.38}$$

By subtracting the voltage at the lin-log transition (Eq. 9.4.36) from this voltage, we find that the output has changed by

$$\Delta V_W = V_S (1 + 1/A^N) \qquad \text{Eq. 9.4.39}$$

For the interval between this transition and the next mid-log point, similar reasoning shows that

$$\Delta V_W = V_S (1 + 1/A^{N-1}) \qquad \text{Eq. 9.4.40}$$

We've been here before. The slope is going to end up being dependent on just which interval we consider, unless we use "The Trick" to fix things up. In fact, we will carry out the algebra more slowly here, like a benign magician, to show how the trick is done.

Let's go back to Eq. 9.4.36, but apply a weighting A/(A–1) to the *gm* of the first stage (last term). Since the knee voltage has not be altered, the peak output current of that stage is also increased by the same factor. Hence:

$$V_W = V_S \{ \quad 1 \quad + \quad 1/A \quad + \quad \ldots\ldots \quad + \quad 1/A^{N-1} \quad + \quad A/(A-1)A^N \quad \}$$

$$= V_S \{ \quad 1 \quad + \quad 1/A \quad + \quad \ldots\ldots \quad + \quad 1/A^{N-1} \quad + \quad 1/(A-1)A^{N-1} \} \qquad \text{Eq. 9.4.41}$$

where we have spaced out the terms and also included the penultimate one, in anticipation of the nest step. As before, we now multiply all the terms by (A–1), and bring this factor outside the brackets, to get a series of the form

$$V_W = V_S \{ (A-1) + (A-1)/A + \quad \ldots\ldots\ldots \quad + \quad (A-1)/A^{N-1} + 1/A^{N-1} \}/(A-1)$$

$$= V_S \{ A - 1 + 1 - 1/A + 1/A + \ldots - 1/A^{N-2} + 1/A^{N-2} - 1/A^{N-1} + 1/A^{N-1} \}/(A-1)$$

The reduced-size terms show how *all* the internal products generate cancelling pairs, leaving just

$$V_W = V_S A/(A-1) \qquad \text{Eq. 9.4.42}$$

as the output at the lin-log transition.

Now let's carry out the expansion for the first mid-log transition, with the A/(A–1) weighting of the first *gm* stage included:

$$V_W = V_S \{ \quad 1 \quad + \quad 1 \quad + \quad 1/A \quad + \quad \ldots\ldots \quad + \quad 1/A^{N-2} \quad + \quad A/(A-1)A^{N-1} \}$$

$$= V_S \{ \quad 1 \quad + \quad 1 \quad + \quad 1/A \quad + \quad \ldots\ldots \quad + \quad 1/A^{N-2} \quad + \quad 1/(A-1)A^{N-2} \}$$

$$= V_S \{ \quad A-1 \quad + \quad A-1 \quad + \quad (A-1)/A \quad + \quad \ldots\ldots \quad + \quad (A-1)\ 1/A^{N-2} \quad + \quad 1/A^{N-2} \}/(A-1)$$

After generating the inner products, this collapses to just

$$V_W = V_S (2A-1)/(A-1) \qquad \text{Eq. 9.4.43}$$

for the output at the first mid-log transition. The change in V_W between the mid-log and lin-log transitions is thus

$$\Delta V_W = V_S (2A-1)/(A-1) - V_S A/(A-1)$$

$$= V_S \qquad \text{Eq. 9.4.44}$$

At the next mid-log transition, the same process yields

$$V_W = V_S\,(3A-2)/(A-1) \qquad \text{Eq. 9.4.45}$$

and the change in V_W is thus

$$\Delta V_W = V_S\,(3A-2)/(A-1) - V_S\,(2A-1)/(A-1)$$

$$= V_S$$

Continuing on this way, it is apparent that, with the modified weighting on just the first G/0 stage, the change in V_W between *any* adjacent pair of transitions is always exactly V_S .

The logarithmic slope voltage V_Y can now be calculated. As before, between any two transitions the input changes by a ratio of A, which can be expressed as *lgt*A. (see Section 9.4.1)

Thus

$$V_Y = \frac{V_S}{lgt\,A} \qquad \text{Eq. 9.4.46}$$

A valuable consequence of the use of the G/0 stages, therefore, is that the slope voltage can be controlled independently of the knee voltage, E, through the bias currents I_Y and the load resistor R_Y.

The result expressed in Eq. 9.4.46 could perhaps have been reached by the following intuitive argument: The inputs to the G/0 stages are separated by amplifiers having a gain A; the outputs of these stages starts at zero and limits at I_Y, so the voltage output V_W increments by $V_S = I_Y R_Y$ for a ratio increase of A at the system input V_X. But, if it's that simple, why does the first stage have to have a higher *gm*?

The explanation is to be found by examining the individual outputs of the *gm* stages as shown in Figure 9.4.12. Note that for the lower-signal region the output at each transition point includes contribution from all of the "higher" detector stages. It can easily be shown that these secondary terms have relative magnitudes which form a series $1/A + 1/A^2 + 1/A^3$ .... which sums to $1/(A-1)$. Thus, when added to the "main" term, of unit magnitude, we find the complete output at these "low-end" transitions is $1 + 1/(A-1)$, which can be written $A/(A-1)$. On the other hand, the top transition does not have the benefit of these additional terms, so *all* of the output must come from just the one detector, which must thus have a weighting $A/(A-1)$.

CURRENT STEPS FROM EACH OF THE G/0 STAGES WITH THE A/(A-1) FIX

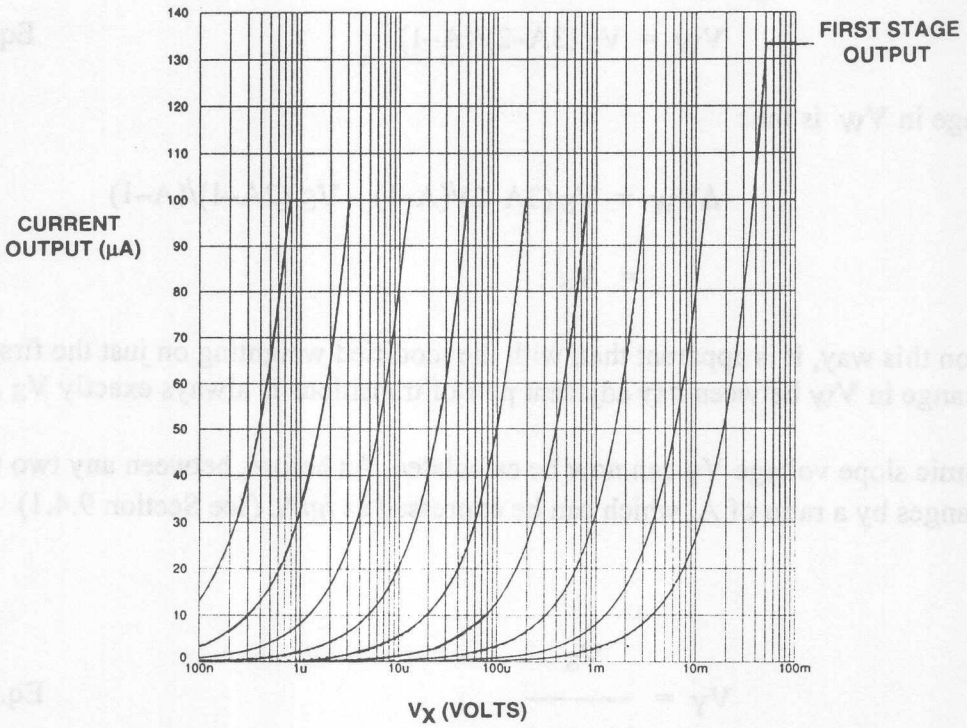


Figure 9.4.12

The intercept V_Z is determined as in all previous cases, that is, by inserting a known V_X, V_W pair into the general equation, in which all but V_Z are known. We will once again use the lin-log transition point. Combining Eqs. 9.4.1, 9.4.34, 9.4.42 and 9.4.46 we have

$$\frac{AV_S}{A-1} = \frac{V_S}{lgtA}\, lgt\, \frac{E/A^N}{V_Z} \qquad \text{Eq. 9.4.47}$$

which yields

$$V_Z = \frac{E}{A^N + A/(A-1)} \qquad \text{Eq. 9.4.48}$$

Compare Eq. 9.4.48 with Eq. 9.4.8.

Thus, the intercept voltage V_Z is traceable to the knee of the A/0 and G/0 stages, while the slope voltage V_Y depends on a decoupled variable, I_Y.

9.4.5 CONVERSION TO DIFFERENTIAL FORM

It is quite feasible to build log-amps using the single-sided prototypes we have been considering up to this point. In fact, some manufacturers have for years been doing that, although it is immediately apparent from a casual glance at their schematics that very little thought has been put into the matter of scaling calibration or temperature stability of the basic cells. All single-sided structures are very prone to HF problems caused by signals on the supply lines (that is, they have poor power-supply rejection).

Suffice it to say that fully-differential topologies have several advantages, one of which is a high degree of immunity to power-supply sensitivity. All signals, including the summation signals from the G/0 stages, have completely-defined current-circulation paths, keeping unwanted signals away from "common" and "supply" lines. At the very high gains and bandwidths typical of multistage log-amps, only a very small amount of feedback from a down-stream stage to the input can easily cause oscillation. The problem, of course, becomes severe in a monolithic implementation, which is one reason why there are practically no multistage monolithic amplifiers available. For example, a 90 dB amplifier chain, with an overall bandwidth of 100MHz has a gain-bandwidth product of about 3200 GHz! Fastidious management of all signal routing is imperative, even when differential technique are employed throughout.

Figure 9.4.13 shows the same log-amp system discussed in the last section, but in fully differential form. It will be apparent that, with appropriate care in the specification of variables, that the mathematics is unaffected by this modification of structure.

A FULLY DIFFERENTIAL REALIZATION OF A PROGRESSIVE-COMPRESSION LOG AMP

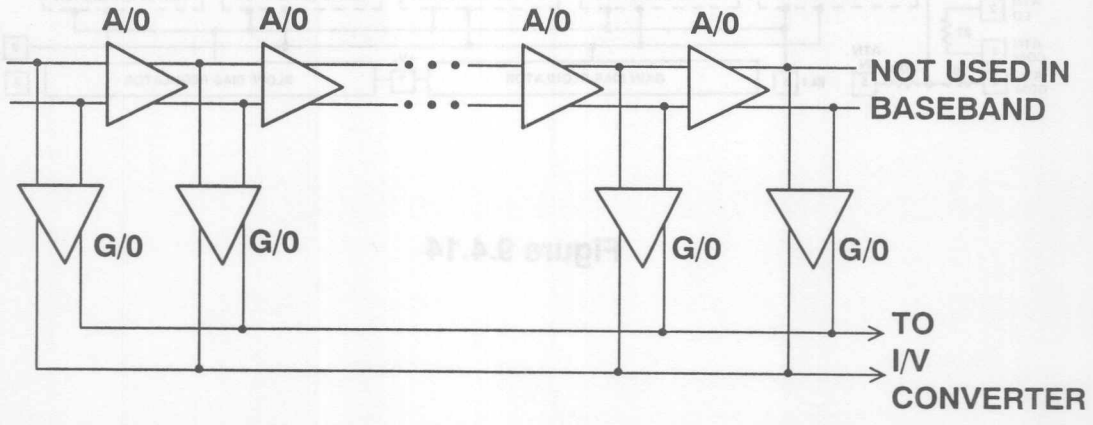


Figure 9.4.13

9.4.6 THE AD640 LOG AMP

In the past, it has been necessary to construct high performance, high frequency successive detection log amps using a number of individual limiting amplifiers. These are typically assembled in complex and costly hybrids. Recent advances in IC processes have allowed this complete function to be integrated into a single chip.

The AD640 log amp contains five limiting stages (10dB per stage) and five full-wave detectors in a single IC package, and its logarithmic performance extends from dc to 145MHz. Furthermore, its amplifier and full-wave detector stages are balanced so that, with reasonable well-considered layout, instability from feedback via supply rails is unlikely. A block diagram of the AD640 is shown in Figure 9.4.14.

BLOCK DIAGRAM OF THE AD640 LOG AMP

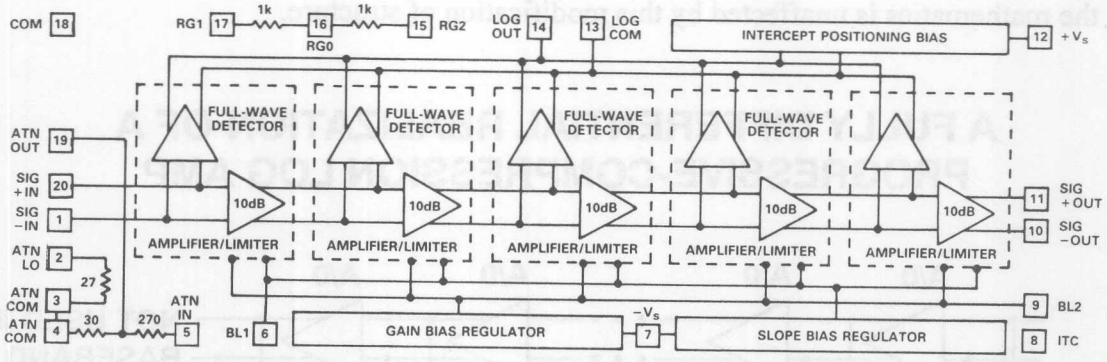


Figure 9.4.14

Unlike all previous integrated circuit log amps, the AD640 is laser trimmed to a high absolute accuracy of both slope and intercept, and is fully temperature compensated. Key features of the AD640 are summarized in Figure 9.4.15.

AD640 LOG AMP FEATURES

- 45dB Dynamic Range - Two AD640s Cascadable to 95dB
- Bandwidth dc to 145MHz - 120MHz when Cascaded
- Laser-Trimmed Slope of 1mA/decade - Temperature Stable
- Less than 1dB Log Non-Linearity
- Balanced Circuitry for Stability
- Minimal External Component Requirement

Figure 9.4.15

Each of the five stages in the AD640 has a gain of 10dB and a full-wave detected output. The transfer function of the device is shown in Figure 9.4.16 along with the error curve. Note the excellent log linearity over an input range of 1 to 100mV (40dB). Although well suited to rf applications, the AD640 is dc-coupled throughout. This allows it to be used in LF and VLF systems, including audio measurements, sonar, and other instrumentation applications requiring operation to low frequencies or even dc.

DC LOGARITHMIC TRANSFER FUNCTION AND ERROR CURVE FOR SINGLE AD640

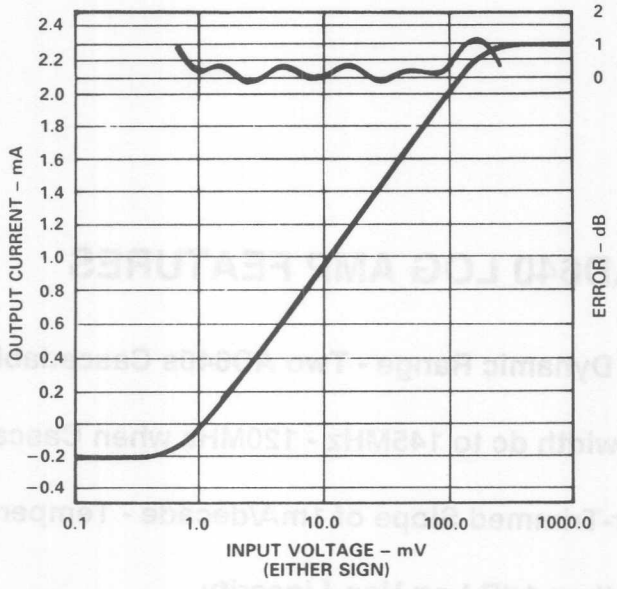


Figure 9.4.16

When two AD640s are cascaded, the second will be delivering an output from the noise of the first. If the full potential dynamic range is to be realized, the bandwidth must be limited because of noise. This may be done with high-pass, low-pass, or band-pass filters, depending on the required response, but, the voltage gain of these filters in their passband must be unity, or there will be a kink in the log response. Figure 9.4.17 shows a 70dB log amp for broadband operation from 50 to 150MHz. The 100MHz passband limits the possible dynamic range, but the performance is still exceptional. Figure 9.4.18 shows a 95dB 10Hz to 100kHz log amp using two cascaded AD640s.

70dB LOG AMP FOR 50-150MHz USING TWO AD640s

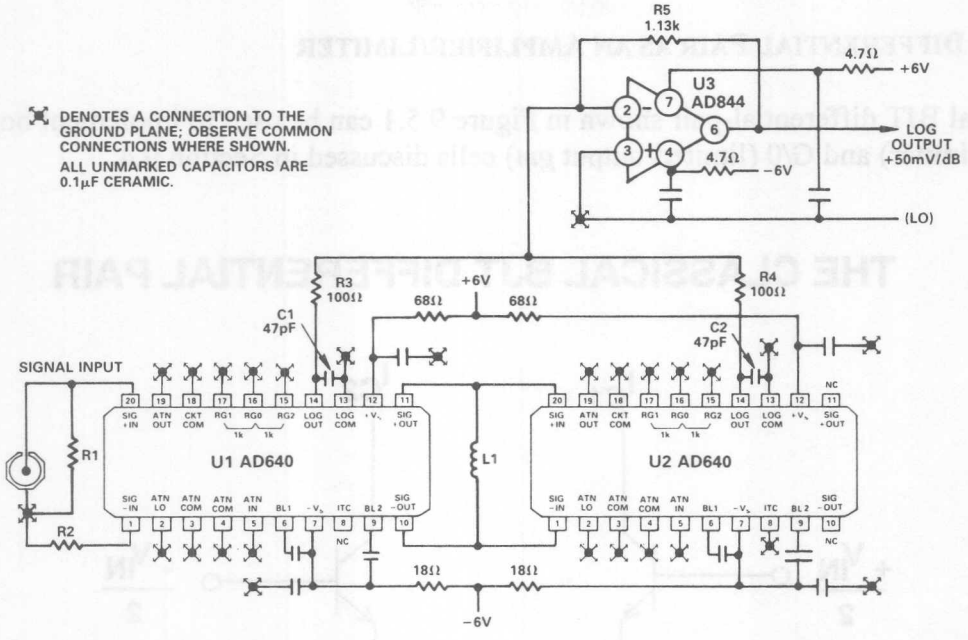


Figure 9.4.17

95dB LOW FREQUENCY LOG AMP (10Hz - 100KHz) USING TWO AD640s

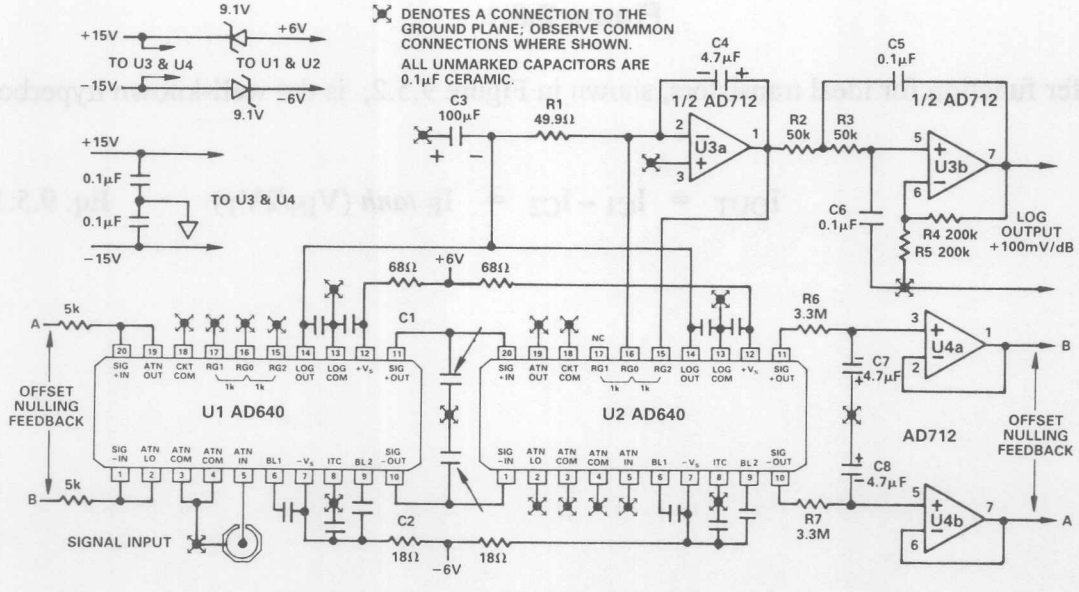


Figure 9.4.18

9.5 LOG-AMPS BASED ON BIPOLAR DIFFERENTIAL STAGES

9.5.1 THE DIFFERENTIAL PAIR AS AN AMPLIFIER/LIMITER

The classical BJT differential-pair shown in Figure 9.5.1 can be used to implement both the A/0 (amplifier/limiter) and G/0 (limited-output *gm*) cells discussed in Section 9.4.

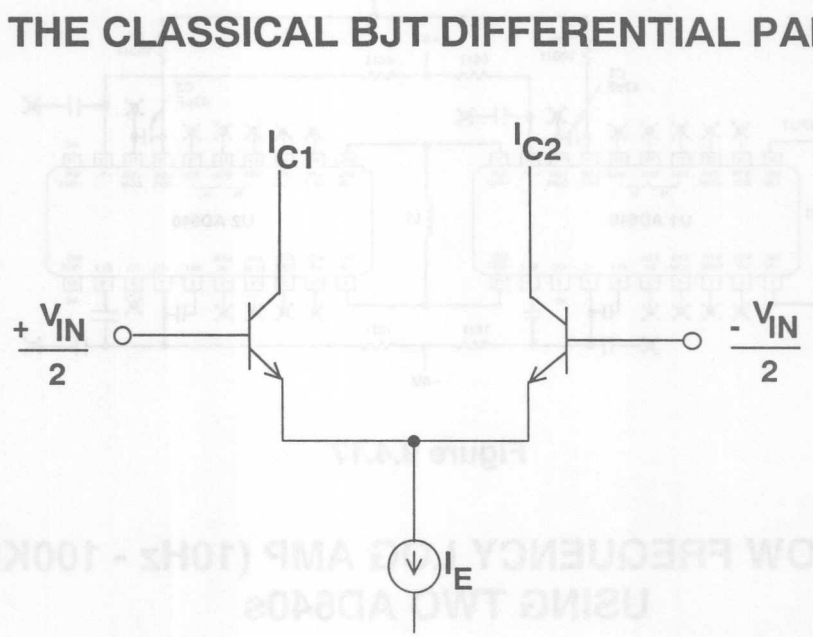


Figure 9.5.1

The transfer function for ideal transistors, shown in Figure 9.5.2, is the well-known hyperbolic tangent:

$$I_{OUT} = I_{C1} - I_{C2} = I_E \tanh (V_{IN}/2V_T) \qquad \text{Eq. 9.5.1}$$

DC TRANSFER FUNCTION OF CLASSICAL BJT PAIR

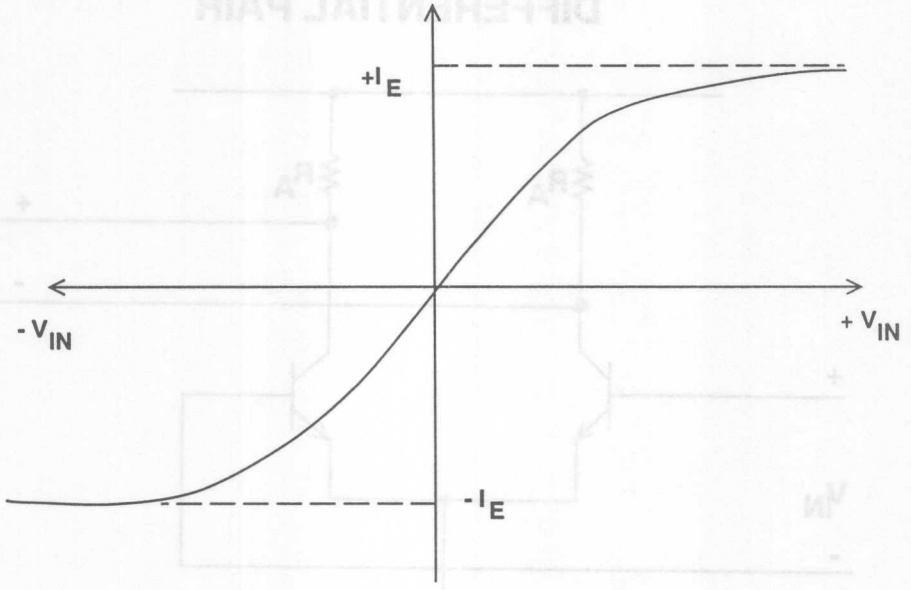


Figure 9.5.2

It follows that

$$gm = \frac{dI_{OUT}}{dV_{IN}} = \frac{I_E}{2V_T} sech^2(V_{IN} / 2V_T) \qquad \text{Eq. 9.5.2}$$

The *gm* therefore has a value of $gmo = I_E/2V_T$ for $V_{IN} = 0$ and falls asymptotically to zero for large inputs. A differential amplifier/limiter can be realized by simply the addition of load resistors, as shown in Figure 9.5.3.

AN A/0 AMPLIFIER BASED ON THE BIPOLAR DIFFERENTIAL PAIR

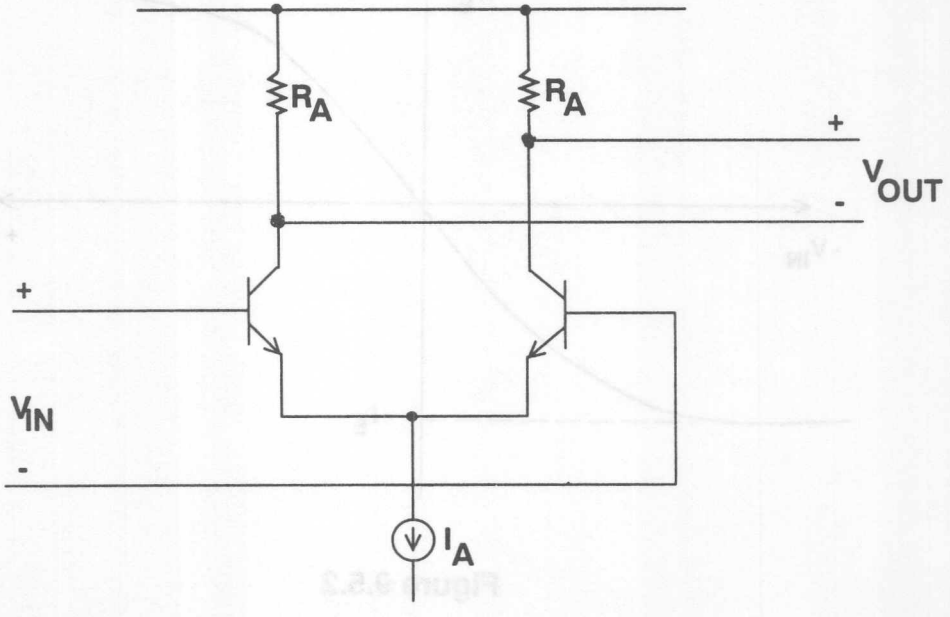


Figure 9.5.3

The small-signal gain A of the amplifier cell is simply

$$A = gmo\, R_A = I_A R_A / 2V_T \qquad \text{Eq. 9.5.3}$$

from which it is immediately apparent that the tail current I_A must be PTAT (proportional to absolute temperature) to cancel the PTAT form of V_T (= kT/q) if the gain, and thus, the system dynamic range, is to be stable with temperature. Unlike the highly-abstracted stages discussed in Section 9.4, this stage does not have a clearly-defined knee voltage at which the gain exhibits an abrupt transition. In fact, the *gm* diminishes continuously with increasing $|V_{IN}|$, as implied by Eq. 9.5.2.

Nonetheless, the theory which the abstractions of Section 9.4 made possible turns out to be remarkably robust, and we can find appropriate values for all of the parameters used up to this point to correctly predict the behavior of log-amps built with these more practical A/0 and G/0 stages.

Thus, for both the amplifier/limiter cell and the limited-output *gm* cell the *effective* knee voltage is just that voltage which, at a fixed *gm* = *gmo*, would take the output to its limiting value. This makes

$$E = 2V_T \qquad \text{Eq. 9.5.4}$$

that is, about 52 mV at 27 °C. This is shown in Figure 9.5.4.

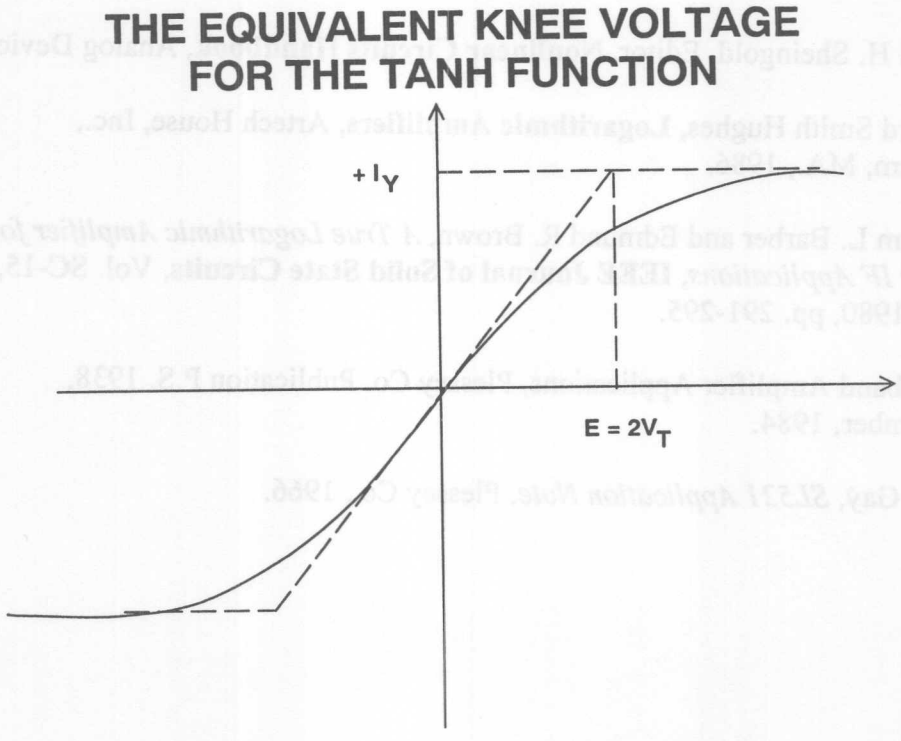


Figure 9.5.4

Now, recalling the lessons taught in Section 9.4, the scaling voltages V_Y and V_Z of a basic logarithmic amplifier are both proportional to this voltage. However, using the later system based on A/0 gain stages (with knee voltage = E) and G/0 summing stages (with peak current = I_Y), the slope voltage V_Y can be rendered arbitrarily accurate and temperature-stable, leaving just the intercept V_Z highly temperature-dependent. It's important to understand that this problem isn't helped by making the tail current of the gain stage (that is, I_E) proportional to absolute temperature: that measure only stabilizes the *small-signal gain* over temperature. The end result is that log-amps based on bipolar differential pairs unavoidably require temperature-compensation of the intercept voltage, V_Z.

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ANALOG DEVICES

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APPLICATION NOTE

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Using the AD834 in DC to 500 MHz Applications: RMS-to-DC Conversion, Voltage-Controlled Amplifiers, and Video Switches

by Mark Elbert and Barrie Gilbert

INTRODUCTION

The AD834 is the fastest four quadrant multiplier available, having a useful bandwidth of 800 MHz, compared to the 60 MHz bandwidth of the AD539 two-quadrant multiplier, the 10 MHz bandwidth of the AD734 four-quadrant multiplier, or the 1 MHz bandwidth of the industry-standard AD534 four-quadrant multiplier. Its monolithic construction and high speed makes the AD834 a candidate for such HF applications as balanced modulation-demodulation, power measurement, gain control, and video switching, at frequencies that were previously beyond the scope of analog multipliers.

The AD834 does not sacrifice accuracy to achieve its speed. In common with all of the Analog Devices multipliers, laser trimming is used during manufacture to null input and output offsets and to establish precise scaling. In typical applications the total static error can be held to less than ±0.5%.

It is available in 8-pin plastic DIP, SOIC, and ceramic packages for the commercial, industrial, and military temperature ranges and operates from ±5 V supplies.

The main challenge in using the AD834 arises from its current-mode output stage. In order to maintain the highest possible bandwidth, the AD834's outputs are in the form of a pair of differential currents from open collectors. This is an inconvenience when a more conventional ground-referenced voltage output is needed. Thus, this application note discusses methods for the accurate conversion of these currents to a single-sided ground-referenced voltage.

These applications include a wideband mean-square detector, an rms-to-dc converter, two wideband voltage-controlled amplifiers, a high-speed video switch, and transformer-coupled output circuits. These applications provide the user with a complete and proven solution, in many cases including recommended sources for critical components.

OVERVIEW OF THE AD834

The AD834, shown in block schematic form in Figure 1, is the outcome of Analog Devices' continuing dedication to high-accuracy analog signal processing. In particular,

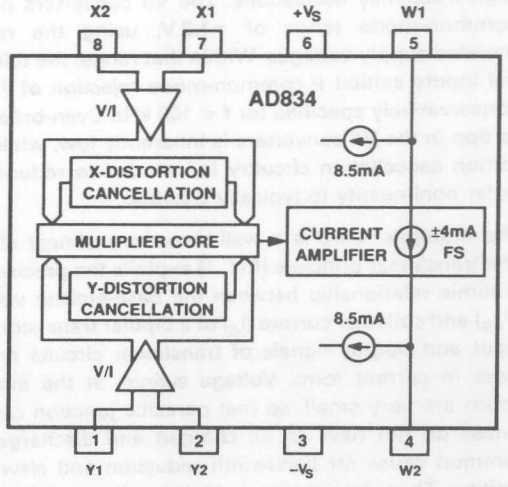


Figure 1. AD834 Block Diagram

it incorporates the experience gained in twenty years of manufacturing analog multipliers. The part is constructed on a 3 GHz epitaxial bipolar transistor process using laser-trimmed thin-film resistors. Attention to many subtle details has resulted in unusually low distortion and noise. Figure 2 shows a more detailed, but still simplified, circuit schematic.

The X- and Y-inputs are applied to high-speed voltage-to-current (V/I) converters, having a transresistance of 285 Ω and a small-signal input resistance of about 25 kΩ. The full-scale input voltage is ±1 V for both inputs. The input bias currents are typically 45 μA. Therefore, the dc resistance seen by both inputs of a differential pair must be equal to minimize offset voltages, just as for an op amp. Resistors at the inputs also minimize the risk of

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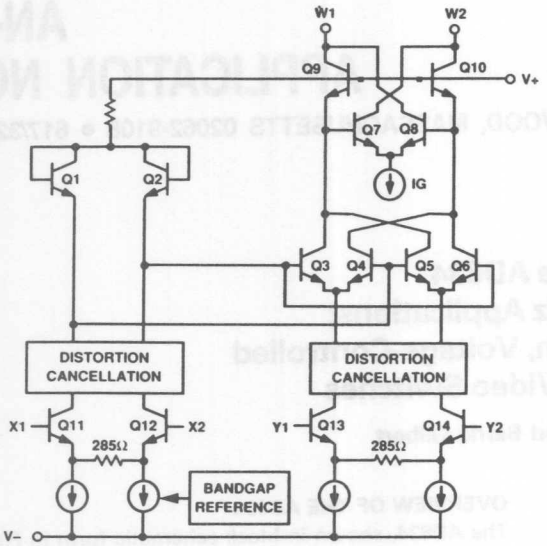


Figure 2. Simplified AD834 Schematic

high frequency oscillations. The V/I converters have a common-mode range of ±1.2 V, using the recommended supply voltages. Within that range, the differential inputs exhibit a common-mode rejection of 70 dB, conservatively specified for f < 100 kHz. Even-order distortion in the V/I converters is inherently low, while distortion cancellation circuitry is included to reduce odd order nonlinearity to typically ±0.05%.

The *multiplier core* is a well-known translinear circuit. The translinear principle [Ref. 1] exploits the precise logarithmic relationship between the base-emitter voltage (V_{BE}) and collector current (I_C) of a bipolar transistor. The input and output signals of translinear circuits are always in current form. Voltage swings at the internal nodes are very small, so that parasitic junction capacitances do not have to be charged and discharged, a common cause for bandwidth reduction and slew-rate limiting. Thus, translinear multiplier cells are inherently fast; they are also readily implemented in monolithic form. However, they can introduce distortion if not carefully designed.

This distortion is due primarily to emitter area mismatches and ohmic resistances in the core transistors (Ref. 2). Using the traditional convention in naming the channels, as shown in Figure 2, the X channel is susceptible to these effects, while the Y signal-path is essentially linear (the four output devices, Q3 through Q6; behaving in many respects like common-base stages, or cascodes). Therefore, the signal requiring the lowest possible distortion should always be handled by the Y channel. For example, in a balanced modulator application, the carrier (local oscillator voltage) should be applied to the X input and the baseband signal to the Y input.

The output from the core is in the form of a pair of differential currents. Now, the scaling of these currents is customarily controlled by adjustment of the bias currents in the V/I converter used on the X-input, which also determines the currents in the diode-connected transistors, Q1 and Q2.

In classical voltage-output multipliers, the range of adjustment needed to absorb the inevitable resistor mismatches is small, and this method of trimming the scaling factor is acceptable. In the AD834, however, the transfer function involves the two input voltages V_X and V_Y, the scaling voltage (generated in the band-gap reference circuit, and trimmed to an accurate value which is assumed here to be 1 V) and the output current, I_W:

$$I_W = \frac{V_X V_Y}{1V} \cdot \frac{I}{R} \qquad (1)$$

In this expression, the value of a resistance, R, determines the calibration of the output current. As fabricated, thin-film resistors have an initial uncertainty which can be as large as ±20%, and the customary methods of trimming the scale factor would result in other compromises (for example, erosion of the available signal range in the X-input V/I converter).

Therefore, the AD834 uses a "Gilbert gain-cell" [Reference 3] after the core to provide the needed adjustment of the effective value of R, which, in fact, is achieved by varying the current gain of this cell through trimming the current I_G. R, after the I_G trim, has an effective value of 250 Ω, resulting in a full-scale output current of ±4 mA when both inputs are at their full-scale value of ±1 V. The typical current-gain is 1.6, and because this type of amplifier is very fast and buffers the core outputs, the overall bandwidth of the multiplier is actually enhanced over that which would be obtained using the core outputs directly.

The bias currents from the core, and the gain-setting current I_G, result in a fairly large standing current—typically 8.5 mA—which flows into the outputs W1 and W2 (Pins 4 and 5). Only the *differential* output is precisely specified to be ±4 mA.

The output currents can be converted back to voltages in a variety of ways. In the simplest case, load resistors connected to the positive supply might be used, but these do not convert the (two) differential outputs to a single-sided voltage.

For the AD834 to operate properly, the output Pins (4 and 5) must be pulled above V+ to avoid saturation of Q7–Q10. To avoid using a separate supply to do this, several of the circuits included here use a voltage-dropping resistor in series with the positive supply Pin (6) of the AD834; this is a higher value than necessary for decoupling purposes.

This dropping resistor lowers the voltage at Pin 6 to provide an extra margin of bias for the output transistors. For example, in the mean-square circuit in Figure 3, 11 mA of quiescent current across the 169 Ω dropping resistor creates 1.86 V of headroom. The decoupling re-

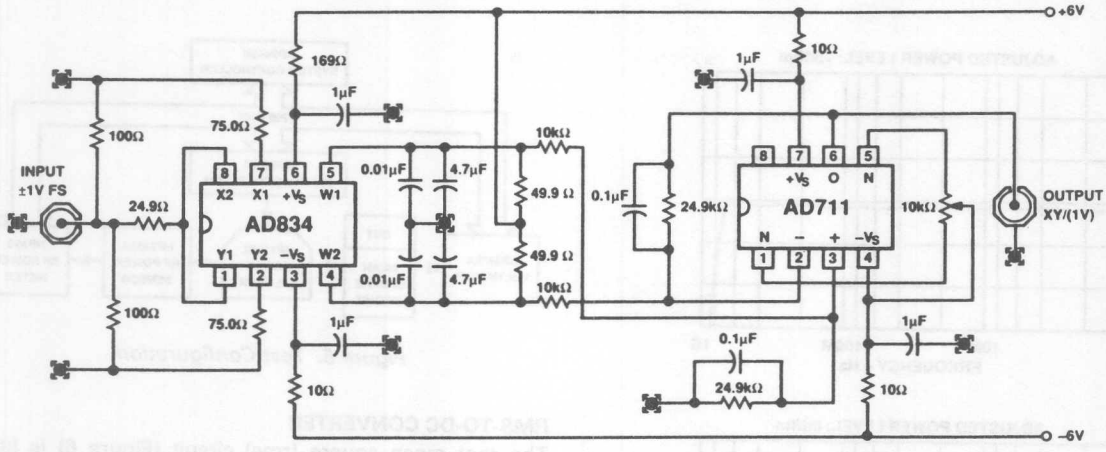


Figure 3. A DC to 500 MHz Mean Square Circuit

sistor in series with the negative supply to Pin 3 is only 10 Ω, since it is included just to decouple the supplies.

Much of this application note, however, is concerned with *more effective ways* of loading the outputs. For example, because they are fully calibrated, the outputs of two or more AD834's can be accurately summed by simply connecting them in parallel, as is done in the rms application discussed later in this application note.

MEAN-SQUARED DETECTOR

We will begin with a discussion of a mean square detector (Figure 3), whose output is a dc voltage proportional to the input power. This circuit is useful in that it requires only a calibrated signal generator and a dc voltmeter to demonstrate the very high speed of the AD834.

The input signal is applied to the X- and Y-inputs connected in parallel. The *instantaneous* output current is thus proportional to the square of the input voltage. The square of a sinusoidal input voltage of amplitude A is an offset cosine at twice the frequency:

$$A(\sin\omega t)^2 = A^2(1 - \cos 2\omega t)/2 \qquad (2)$$

If the input to the AD834 has this sinusoidal form, then the instantaneous output current (using Equation 1) is simply

$$I_W = 2A^2(1 - \cos 2\omega t)\ mA \qquad (3)$$

the average value of which is just 2 mA for the maximum 1 V amplitude sinusoid.

The full-scale differential voltage which would be measured across Pins 4 and 5 of the AD834 is, therefore, 2 mA × (50 Ω + 50 Ω), or 200 mV. This average is extracted by the low-pass filter formed by the 4.7 μF 22 μF (AVX part #SR505E475MMAA and #SR505a223JAA) capacitors in conjunction with the 50 Ω collector load resistors, having a −3 dB frequency of about 650 Hz.

Two capacitors are used in parallel since the 4.7 μF capacitor uses the compact but lossy Z5U dielectric material while the 22 μF capacitor uses a high Q NPO dielectric which ensures good filtering at the highest frequencies. Note that the 4.7 μF capacitors have a −20% to +80% tolerance, so their −3 dB frequency is not accurate, nor does it usually need to be. Further filtering is performed by the capacitors in shunt with the feedback resistors of the AD711 operational amplifier, configured to have a −3 dB frequency of 65 Hz.

Due to finite averaging of the circuit, there will be some ripple for low frequency inputs. For the circuit shown, a 1 kHz input will produce the mean-square plus a −42 dB 2 kHz ripple; for 100 kHz input, the ripple will be only −80 dB. Since the output is band limited, we can use a generic low speed op amp with ample common-mode range, obviating the need for level shifting. The differential gain of the amplifier can be chosen to provide a convenient scale factor.

The full-scale gain of the circuit in Figure 3 is calculated as follows. The average output current is ±2 mA for 1 V (peak) sinusoidal input, which creates ±100 mV across each 50 Ω output load resistor or 200 mV differential. The amplifier is configured for a differential gain of 2.5 (feedback resistance over source resistance), yielding a circuit gain of 0.5 V dc output for 1 V rms input.

The bandwidth of this circuit is limited by package capacitance and inductance. In the 8-pin cerdip, the multiplier's response normally starts to rise at 500 MHz due to package resonance and peaks at 800 MHz before rolling off. A 24.9 Ω resistor at the input dampens the resonance yielding an essentially flat response out to 800 MHz. (The package inductance will be different for a surface mount AD834.) Figure 4 shows the results over frequency for three different power levels using the test configuration shown in Figure 5.

Neglecting the 24.9 Ω in series with the high impedance inputs, the input resistance to the mean square circuit in Figure 3 is 50 Ω. Since the full-scale input range is ±1 V, the maximum measurable power with a 50 Ω input load is 10 mW (20 dBm), assuming a sinusoidal input.

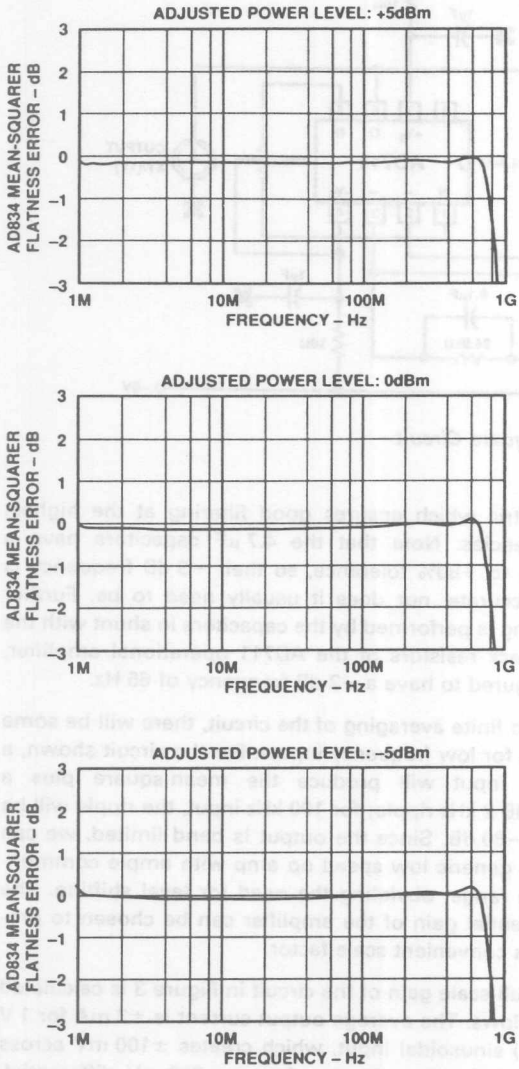


Figure 4. Frequency Response of Mean Square Circuit for Input Power Levels of −5 dBm, 0 dBm, and +5 dBm

For greater input ranges, a voltage divider with a series resistance of 50 Ω at the input will scale down the voltage seen by the AD834 while maintaining a proper termination resistance. For example, if the input signal is applied to a 45 Ω resistor in series with a 5 Ω resistor to ground, then taking the AD834's input from the middle node of the voltage divider provides 20 dB attenuation of the input signal, while maintaining a termination resistance of 50 Ω (45 Ω + 5 Ω).

Detection of low power signals is limited by dc offsets and the common-mode rejection of the op amp. For example, a −20 dBm signal, corresponding to 22.4 mV rms across 50 Ω, would result in a 4.5% error in the presence of only 1 mV of offset in the op amp. A 10% error can occur if the AD834's X channel offset is just 2 mV.

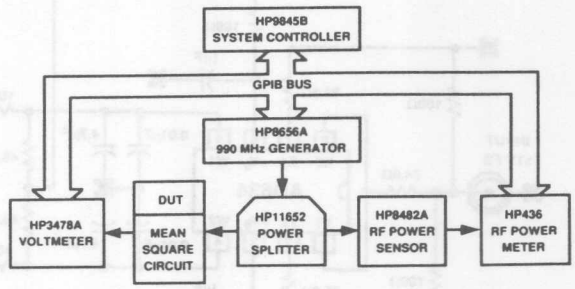


Figure 5. Test Configuration

RMS-TO-DC CONVERTER

The root mean square (rms) circuit (Figure 6) is little more than the mean square detector circuit described above followed by a square root circuit. The frequency response is determined by the front end squarer and output filter. From the mean-square discussion, the squarer functions well past 500 MHz, while the lower −3 dB frequency response is 340 Hz (100 Ω and 4.7 μF). Note that a resistor divider network at the input determines the full-scale input voltage to be ±2 V peak.

The square root function is performed by a squaring AD834 in the feedback loop of an AD711 operational amplifier. The 2N3904 transistor functions as a buffer. The resistive divider network (two 100 Ω) between the buffered output and the X and Y channel inputs of the AD834 used in the square root section determines the output scaling to be ±2 V full scale.

The outputs of the two AD834s are current-differenced. Accurate output differencing and summing is possible owing to the precision of the laser trimmed AD834 output signal current scaling. The AD711 forces the difference between the two AD834 signal current to zero. Any error in the nulling generates a voltage across the two 100 Ω pull-up resistors.

After additional filtering and level shifting by the 15 kΩ, 85 kΩ, and 0.1 μF network, the residual error is amplified by the full AD711 open loop gain. The amplified error signal forces the AD834 in the feedback loop to match its output to the mean-squaring AD834's output. The error is nulled when the rms circuit's output is equal to the square-root of the circuit's input mean-squared, hence the rms function.

The accuracy of the circuit at small signal levels is limited by inevitable offset voltages. While a nominal 0 V input with a 1 mV error to a mean-square function generates a 1 μV output error, the same input error generates a 31.6 mV output error through a square root circuit.

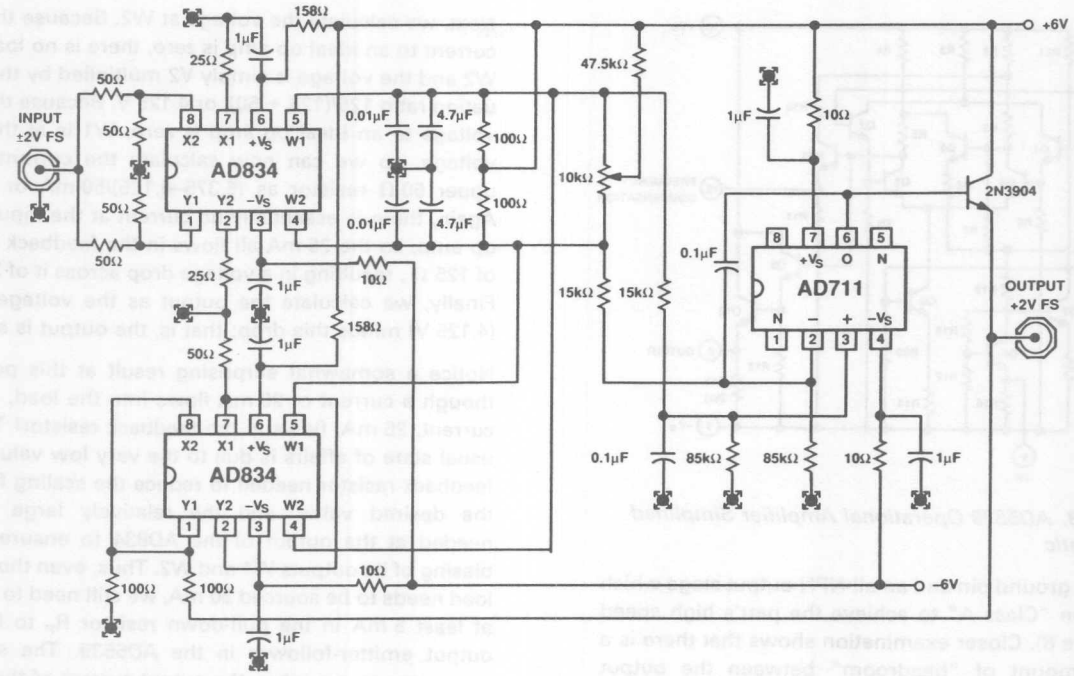


Figure 6. DC to 500 MHz RMS-to-DC Converter

DC COUPLED VCA APPLICATIONS

Where the dc response of the AD834 cannot be discarded, some form of level shifting, either passive or active must be employed, since high speed op amps often have inadequate common-mode range. The following applications show the use of active and passive level shifting circuits in the implementation of wideband voltage-controlled amplifiers.

A DC TO 60 MHz VOLTAGE-CONTROLLED AMPLIFIER USING PASSIVE LEVEL SHIFTING

Figure 7 shows the schematic of a circuit employing a passive network as a level shifter. The op amp chosen here is the AD5539.

The AD5539 is built on the same process as the AD834 and provides a 2 GHz gain-bandwidth product at high closed-loop gain. Unlike most op amps, the AD5539

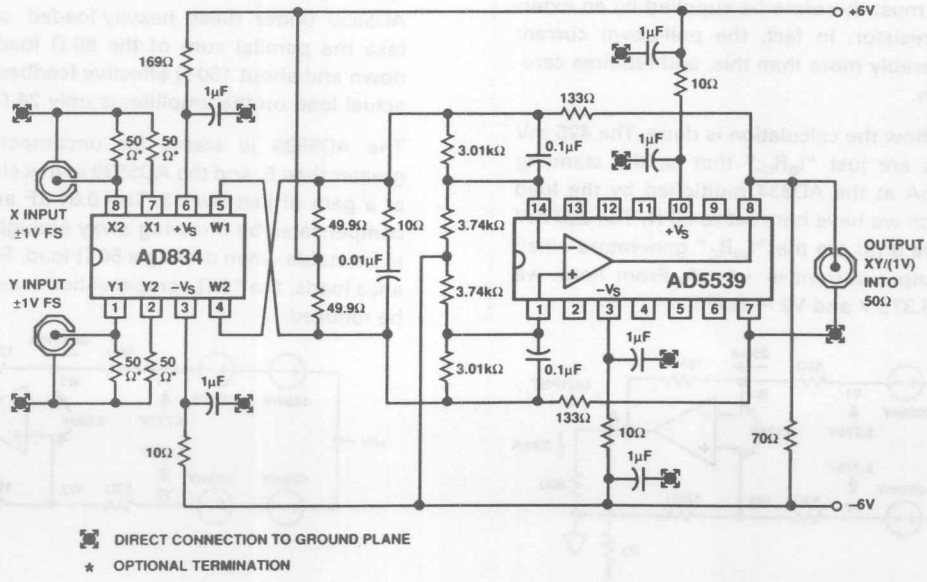


Figure 7. DC to 60 MHz Voltage-Controlled Amplifier Using Passive Level Shifting

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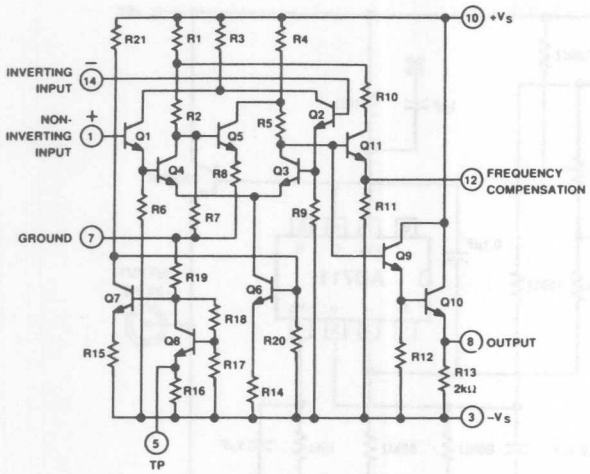


Figure 8. AD5539 Operational Amplifier Simplified Schematic

features a ground pin and an all-NPN output stage which operates in "Class A" to achieve the part's high speed (see Figure 8). Closer examination shows that there is a limited amount of "headroom" between the output node and the inputs, and between these voltages and ground. This, its high speed, and other unusual attributes of the AD5539 require special care in its use.

First, consider the consequences of its Class A output stage. In most op amps, the output can both "pull up" and "pull down" on the load, but the NPN emitter-follower output stage can only pull up. The AD5539 has an internal pull-down resistor (R11) of 2 kΩ, which can only supply two or three milliamps. A general-purpose high-speed multiplier must be able to swing to at least ±1 V while driving the minimum likely load resistance of 50 Ω. At this output level, the load current will be ±20 mA, which must therefore be supplied by an external pull-down resistor. In fact, the pull-down current must be considerably more than this, and requires careful consideration.

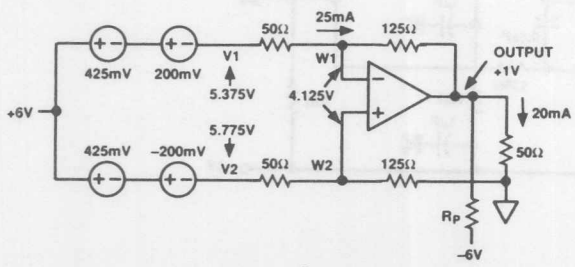
Figure 9 shows how the calculation is done. The 425 mV voltage sources are just "I_BR_C," that is, the standing current of 8.5 mA at the AD834 multiplied by the load resistor R_C, which we have here set to 50 Ω. The 200 mV sources in Figure 9 (a) are the "I_WR_C" generators when the full-scale output current is +4 mA. From here, we calculate V1 – 5.375 V and V2 – 5.775 V.

Next, we calculate the voltage at W2. Because the input current to an ideal op amp is zero, there is no loading at W2 and the voltage is simply V2 multiplied by the attenuation ratio 125/(125 + 50), or 4.125 V. Because the input voltage to an ideal op amp is zero, W1 is at the same voltage, so we can now calculate the current in the upper 50 Ω resistor as (5.375–4.125)/50 mA or 25 mA. Again, there is essentially no current at the input of the op amp, so the 25 mA all flows in the feedback resistor of 125 Ω , resulting in a voltage drop across it of 3.125 V. Finally, we calculate the output as the voltage at W1 (4.125 V) minus this drop; that is, the output is at +1 V.

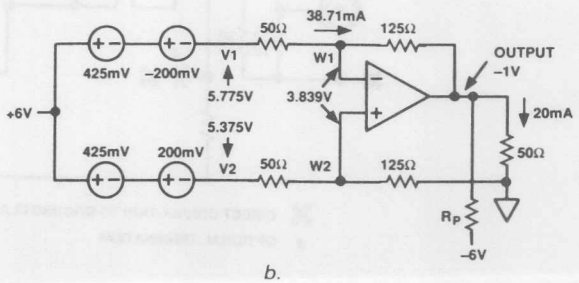
Notice a somewhat surprising result at this point: although a current of 20 mA flows into the load, a larger current, 25 mA, flows in the feedback resistor! This unusual state of affairs is due to the very low value of the feedback resistor needed to reduce the scaling factor to the desired value, and the relatively large voltage needed at the output of the AD834 to ensure proper biasing of its outputs W1 and W2. Thus, even though the load needs to be sourced 20 mA, we still need to provide at least 5 mA in the pull-down resistor R_P to bias the output emitter-follower in the AD5539. The situation gets more severe when the output current of the AD834 is reversed, because we now need to sink 20 mA in the 50 Ω load and the voltage across the feedback resistor is now even higher.

This situation is shown in Figure 9(b). The calculation is exactly as before, and we discover that the current in the feedback resistor is now 39.7 mA. So R_P needs to provide the load current of 20 mA and an additional 40 mA or so in the feedback path, while the voltage across it is 5 V. This would require R_P = 83 Ω. In practice, it should be slightly lower to prevent slew rate limiting the fall time. Also, the feedback resistor will be raised from 125 Ω to 133 Ω to make up for the finite gain of the AD5539 under these heavily-loaded conditions. If we take the parallel sum of the 50 Ω load, the 70 Ω pull-down and about 150 Ω effective feedback resistance, the actual load on the amplifier is only 24 Ω!

The AD5539 is stable for uncompensated gains of greater than 5, and the AD5539 in this circuit is operating at a gain of just over 3. The 0.01 μF and 10 Ω network compensates by throwing away enough open loop gain to be stable when driving a 50 Ω load. For higher impedance loads, the 10 Ω compensation resistor may need to be reduced.



a.



b.

Figure 9. Equivalent Circuits for Calculating the Value of the Pull-Down Resistor

A level-shifting network is included between the nodes W1 and W2, whose average voltage is about +4 V, to the input of the AD5539 which must be close to ground. With the values shown, the op amp inputs are set slightly below ground (about −460 mV). This network halves the low frequency open-loop gain, which has some effect on the dc accuracy in the presence of offset voltages at the input to the AD5539. If output offset is important, a 500 Ω potentiometer should be inserted in series with the 3.74 kΩ resistors and its slider taken to −6 V. It is then adjusted for zero output with both X and Y inputs set to zero.

Note also that the "inner" Pins X1 and Y2 on the AD834 are grounded to minimize HF feedthrough; the resulting phase-reversal at the X input is corrected by swapping W1 and W2.

Figure 10 shows the pulse response with the input pulse applied to the X input and the Y input set to +1 V, indicating a rise time of 6 ns.

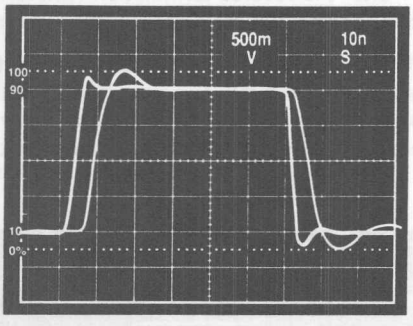


Figure 10. Pulse Response of the DC to 60 MHz Voltage-Controlled Amplifier

Figure 11 shows a set of frequency responses taken on an HP8753B network analyzer for Y inputs of +1 V, 316 mV, +100 mV, and 0 V. In the case of 0 V, the Y input is adjusted to null the input offsets. Note that the high frequency feedthrough is less than −65 dB of full scale (f < 3 MHz).

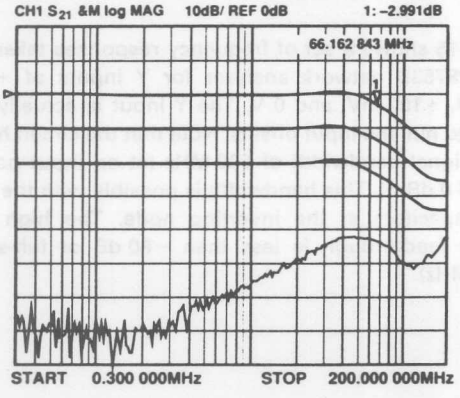


Figure 11. Frequency Response of the DC to 60 MHz Voltage-Controlled Amplifier

A DC TO 480 MHz VOLTAGE-CONTROLLED AMPLIFIER USING ACTIVE LEVEL SHIFTING

Figure 12 (a) shows an active level shifter, using a PNP transistor as a common base stage or cascode. Here, the AD834 is modeled by three ideal current sources, two for the 8.5 mA bias currents and one for the ±4 mA differential signal current. The transistors' bases are tied to +5 V, setting the emitter potential stays at 5.7 V resulting in a voltage of 3.3 V across the resistors R1 and R2 in the absence of signal. Figure 12 (b) shows an equivalent circuit.

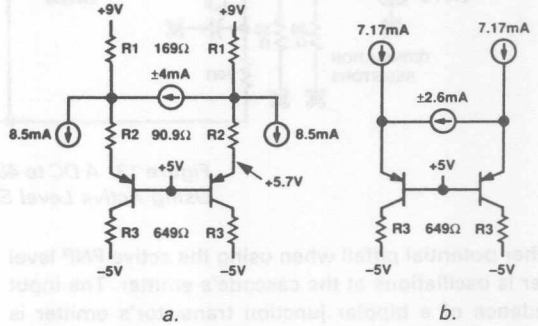


Figure 12. An AD834 Output Stage Using Active Level Shifting

The equivalent dc bias current of 7.17 mA is found by solving for the current flowing into the emitter when the signal current generator is zero. In the ac domain, the signal current generator sees R1 and R2 both tied to low impedance nodes. By inspection, the original signal current has been scaled by:

$$\pm 2.6mA = \pm 4\ mA \times \frac{R1}{R1 + R2} \quad (4)$$

Since AD834's outputs have very high output impedances, the equivalent series resistance can be ignored. The entire 7.17 mA flowing into the cascode's emitter flows out the cascode's collector, assuming a good α, and across R3. The voltage across R3 is:

$$4.65\ V = 7.17\ mA \times 649\ \Omega \quad (5)$$

The operational amplifier's inputs are 350 mV below ground and are within the common-mode range of a wideband amplifier.

The bandwidth of a transistor configured as a cascode is the unity gain frequency (f_T) of the transistor, provided that the user does not create any spurious poles. Choosing an R1 and R2 such that their parallel sum is too large for the transistor's parasitic emitter-base capacitance or an R3 too large for the transistor's parasitic collector-base capacitance will create unwanted poles that lower the frequency response of the circuit.

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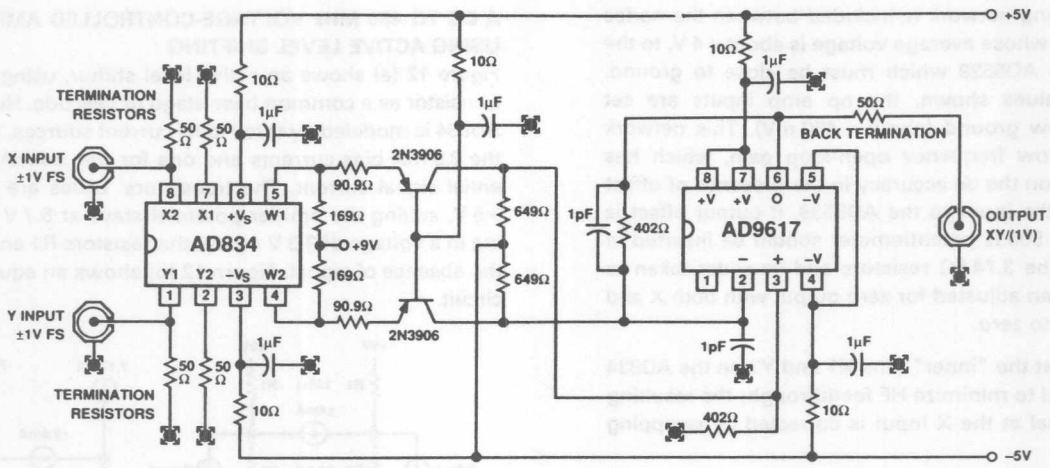


Figure 13. A DC to 480 MHz Voltage-Controlled Amplifier Using Active Level Shifting

Another potential pitfall when using the active PNP level shifter is oscillations at the cascode's emitter. The input impedance of a bipolar junction transistor's emitter is inductive at frequencies approaching its gain-bandwidth product (f_T), while the AD834's output is capacitive. Due to the high bandwidth of the system, these impedances can lead to oscillation.

To prevent such oscillations, the emitter in Figure 12 has been isolated from the AD834's output by R2. This prevents oscillations while providing signal attenuation (gain control) as related in Equation 4. The 2N3906s provide wideband level shifting without resonance or oscillation. Care must be taken when using alternative transistors.

The signal current at the cascodes' collectors is now fed to a wideband amplifier in a differential current to voltage converter configuration as shown in Figure 13. This configuration is similar to an op amp driven current-to-voltage converter which typically follows a current output multiplying digital-to-analog converter.

The AD9617 makes an excellent choice to drive the current to voltage converter. The AD9617 is a second-generation transimpedance amplifier (also known as a current feedback or TZ amplifier) with a fully complementary output stage (unlike the AD5539), and optimized for use with a 400 Ω feedback resistor.

The AD9617 inputs are tied directly to the collectors of the cascodes. The op amp creates a virtual short between the input nodes, forcing all the signal current to flow in the feedback paths. The differential transresistance of the convertor is 400 Ω. The desired scaling can be attained by means of the R1 and R2 attenuation network described above. The full-scale gain of the circuit (X = Y = 1 V) at the AD9617's output is calculated as:

$$2 \times 2.6\,mA \times 400\,\Omega = 2.08\,V \qquad (6)$$

or 1.04 V after the reverse termination resistor. The actual circuit shows a full-scale gain closer to unity.

Figure 14 shows the full-scale step response (−1 V to +1 V) applied to the X input and the Y input set to +1 V demonstrating the circuit's capabilities with a rise time of under 2 ns while exhibiting some overshoot, but no ringing. Note that the output slews at over 500 V/μs.

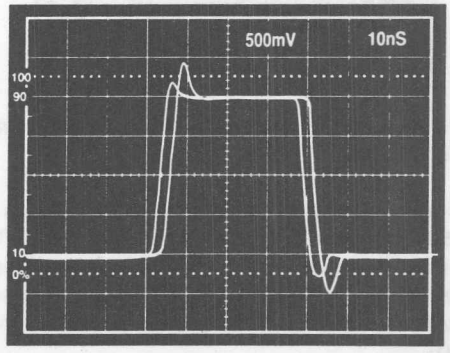


Figure 14. Step Response of the Wideband VCA

Figure 15 shows a set of frequency responses taken on the HP8753B network analyzer for Y inputs of +1 V, 316 mV, +100 mV, and 0 V. The Y input is actually adjusted to null the input offsets. Note that the circuit has a small-signal bandwidth of 500 MHz (at an input power level of 0 dBm). This bandwidth is possible with the two 1 pF capacitors at the inverting node. The high frequency feedthrough is less than −80 dB of full-scale ($f < 2$ MHz).

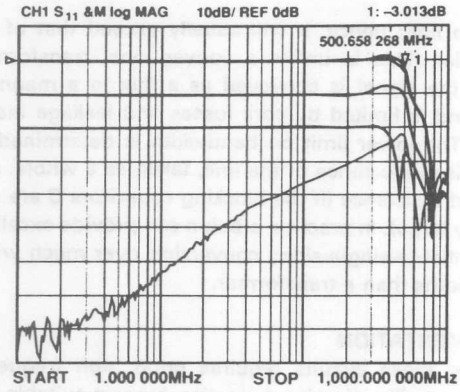


Figure 15. Frequency Response of the Wideband VCA

THE AD834 AS A VIDEO SWITCH

With 0 V or +1 V applied to the X channel as gate control and the video signal to the Y channel, the AD834 becomes a high-speed video switch. Figure 16 illustrates this idea with a high speed current switching circuit centered around an ECL switch. The current flows through either Q1 or Q2, depending on the input voltage. Current switching ensures fast and clean switching to determined levels (+1 V and ground), and allows the user to over- or under-drive the gate input.

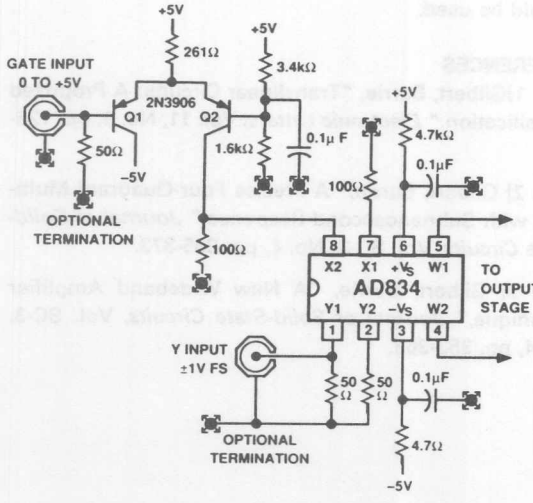


Figure 16. The AD834 as a High-Speed Video Switch

The AD834 switches on as the gate input rises from +1 V through +2 V at the gate circuit input. Below 1 V, Q1 absorbs almost all of the current from the 216 Ω resistor; the 2N3906 transistor is turned off. In this state, the 100 Ω resistor from the X2 input to ground accurately shuts the Y channel off, with Y channel feedthrough to the output measured at −50 dB. With the base of Q2 held at 1.6 V, the transistor's emitter potential is 2.35 V. A steady 10.2 mA (minus base current) from the 261 Ω resistor generates +1 V across the 100 Ω resistor at the X2 input independent of the exact high level of the gate input.

Figure 17 shows a scope photograph of a 1.5 ns rise-time pulse gating a 200 MHz signal. The resulting envelope rise time is 2.7 ns; it has a fall time of 3.0 ns. Although the switched signal may be much slower, the output stage from the AD834 should have a bandwidth greater than 100 MHz in order to maintain an envelope rise time of 3.5 ns.

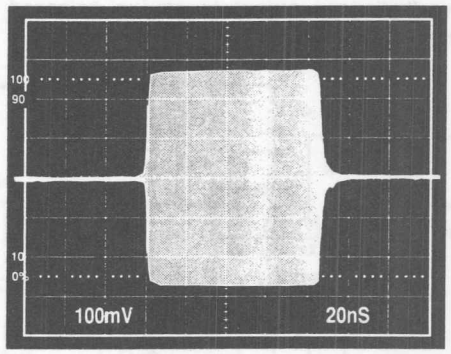


Figure 17. Rise Time of the Video Switch

AC OUTPUT-COUPLING METHODS

In many applications, the dc component at the output can be discarded. In such cases, a wideband buffer can easily ac couple to the AD834 output. The circuits below show the use of simple transformers and baluns for passive, ac coupled output circuits.

TRANSFORMER-COUPLED OUTPUT

Figure 18 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design will depend entirely on the application. Transformers may also be used at the inputs. Center-tapped transformers can reduce high frequency distortion and lower HF feedthrough by driving the inputs with balanced signals. Suitable center-tapped transformers include the Coilcraft WB2010PC, which the manufacturer specifies for 0.04 MHz to 250 MHz operation.

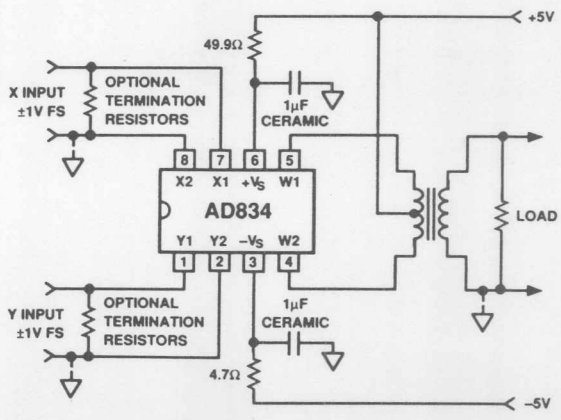


Figure 18. The AD834 with Transformer-Coupled Output

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BALUN-COUPLED OUTPUT

Figure 19 shows a circuit which uses blocking capacitors to eliminate the dc offset, and a balun, a particularly effective type of transformer, to convert the differential (or balanced) signal to a single-sided (or unbalanced) output. A balun consists of a short length of transmission line wound on to a toroidal ferrite core, which converts the 'bal'anced output to an 'un'-balanced one (hence the use of the term).

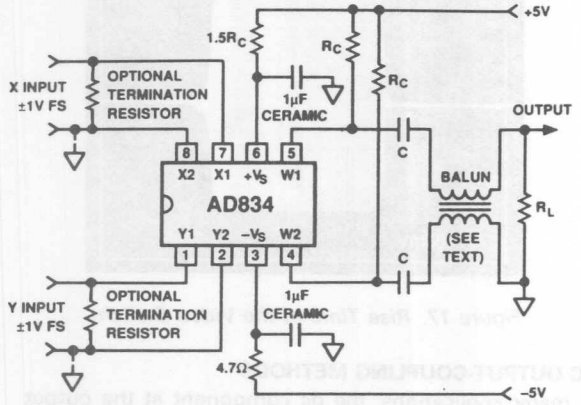


Figure 19. The AD834 with Balun-Coupled Output

Although the symbol used is identical to that for a transformer, the mode of operation is quite different. In the first place, the load should now be equal to the characteristic impedance of the line, although this will usually not be critical for short line lengths. The collector load resistors R_C may also be chosen to reverse-terminate the line, but again this will only be necessary when an electrically long line is used. In most cases, R_C will be made as large as the dc conditions allow, to minimize power loss to the load. The line may be a miniature coaxial cable or a twisted pair.

It is important to note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; hence, it will usually exceed that of the multiplier. This is unlike a conventional transformer, where the signal is conveyed as a flux in a magnetic core, and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the series inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors C are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

IMPLEMENTATION

Building these circuits requires good high frequency techniques. The circuit schematics suggest suitable layout. **Ground plane is essential for all of the circuits described in this applications brief.** It should cover as much of the component side of the PCB as possible, but not directly underneath the IC or encircling any individual pins. Sockets add to the pin capacitance and inductance, and should be avoided. If sockets are necessary, use individual pin sockets such as AMP p/n 6-330808-3. They contribute far less stray reactance than the molded socket assemblies. Each power trace should be decoupled at the IC with a 0.1 μF low inductance ceramic capacitor, in addition to the main decoupling capacitor. All lead lengths should be kept as short as possible. For lead lengths longer than an inch, stripline techniques should be used.

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[Ref. 3] Gilbert, Barrie, "A New Wideband Amplifier Technique," *Journal of Solid-State Circuits*, Vol. SC-3, No. 4, pp. 353-365.

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Video VCAs and Keyers Using the AD834 and AD811

by Eberhard Brunner, Bob Clarke, and Barrie Gilbert

INTRODUCTION

Voltage-controlled amplifiers (VCAs) built from analog multipliers take one of two forms. In the first, the multiplier acts as a voltage-controlled attenuator ahead of a fixed-gain amplifier. This type of VCA is used in applications where only a moderate maximum gain, but a fairly high maximum loss, are needed. In the second, the variable attenuation is placed in the feedback path around an op amp, which, in fact, implements an analog divider, more suitable for applications requiring high gains.

This application note describes practical circuits in which the wide bandwidth of the Analog Devices AD834 Four-Quadrant Multiplier and the AD811 Current-Feedback Op Amp are exploited to provide a video-quality VCA with a maximum gain of 12 dB (×4) or 20 dB (×10), based on the first of the above methods. A slightly modified form of this VCA, using two multipliers whose outputs are summed, provides the first of two video keyer designs; a second design uses global negative feedback around the multipliers to achieve improved accuracy and some simplification.

A VIDEO-QUALITY VCA

The VCA is shown in Figure 1. The AD834 multiplies the signal input by the control voltage. Its outputs are in the form of differential currents from a pair of open collectors, ensuring that the full bandwidth of the multiplier (which exceeds 500 MHz) is available for certain applications. In this case, more moderate bandwidth is obtained using current-to-voltage conversion, provided by the AD811 op amp, to realize a practical amplifier with a single-sided ground-referenced output. Using feedback resistors R8 and R9 of 511 Ω the overall gain ranges from −70 dB for V_G ~0 to +12 dB (a numerical gain of four) when V_G = +1 V.

The −3 dB bandwidth is 90 MHz (Figure 2) and is essentially independent of gain. The response can be maintained flat to within ±0.1 dB from dc to 40 MHz at full gain (Figure 3) with the addition of an optional capacitor of about 0.3 pF across the feedback resistor R8. The circuit produces a full-scale output of ±4 V for a ±1 V input, and can drive a reverse-terminated load of 50 Ω or 75 Ω to ±2 V. Figure 4 shows the typical pulse response.

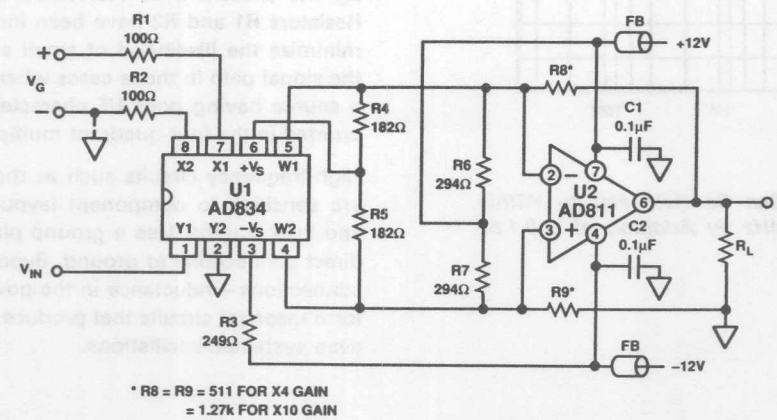


Figure 1. Complete VCA Provides Up to 20 dB of Gain (G = BW = 25 MHz) and a Bandwidth of Over 90 MHz (G = 12 dB)

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The gain can be increased to 20 dB (×10) by raising R8 and R9 to 1.27 kΩ, with a reduction of the −3 dB bandwidth to about 25 MHz (also shown in Figure 2) and a maximum output voltage of ±9 V using the ±12 V supplies. It is not necessary to alter R6 and R7 for the high gain version of the amplifier, although an optimized design would raise these slightly to restore the common-mode voltage at the input of the AD811 to +5 V.

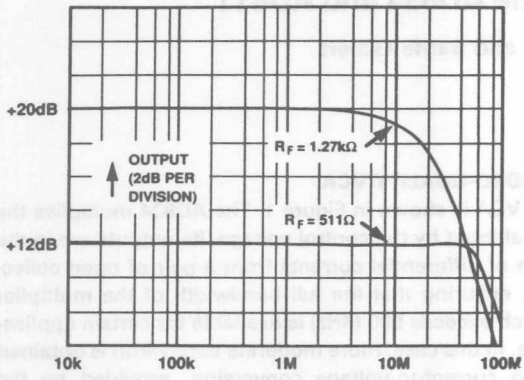


Figure 2. Small-Signal Response of the VCA Shows a −3 dB Bandwidth of 90 MHz for the 12 dB Version and 25 MHz for the 20 dB Version

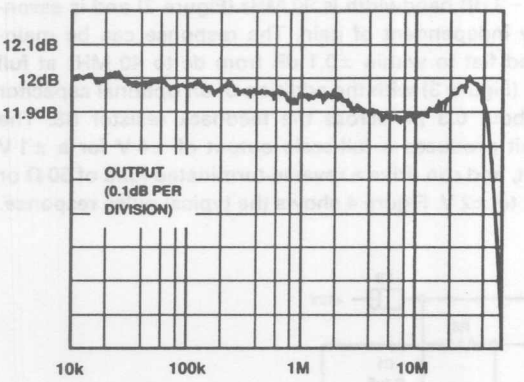


Figure 3. AC Response Can Be Held Flat to Within ±0.1 dB from DC to 40 MHz by Addition of a 0.1 pF Capacitor Across R8

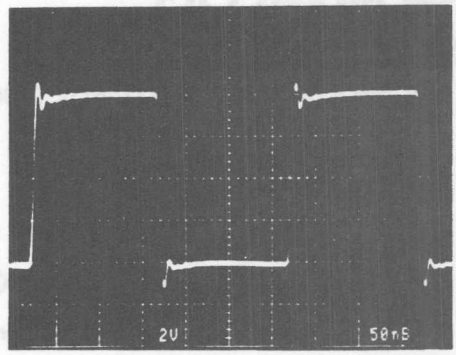


Figure 4. Full-Output Pulse Response for the 12 dB Amplifier

The gain-control input may be a positive or negative ground-referenced voltage, or fully differential, depending on the user's choice of connections at Pins 7 and 8. As shown, a positive value of V_G results in an overall noninverting response. Reversing the sign of V_G simply causes the sign of the overall response to invert. In fact, although we have called this a voltage-controlled amplifier, it can just as well be used as a general-purpose four-quadrant multiplier with good load-driving capabilities and fully symmetrical responses from X- and Y-inputs.

We have used the Y-input of the multiplier for the signal, since this port is slightly more linear than the X-input, and have shown X2 and Y2 grounded. These inputs each draw about 45 μA of bias current, so the grounded (unused) inputs should be terminated preferably in the same resistance as the source, in each case, to minimize offset voltages. The resistance of the signal source may in some cases be essentially zero (as in the case of a transformer-coupled input, or certain signal generators); note that a doubly terminated cable line of impedance Z_O will present a dc resistance of $Z_O/2$ at the input. Resistors R1 and R2 have been included in Figure 1 to minimize the likelihood of small aberrations arising in the signal path in those cases where V_G is derived from a source having poor HF characteristics; they may be omitted in the four-quadrant multiplier application.

High-frequency circuits such as those described herein are sensitive to component layout, stray capacitance, and lead lengths. Use a ground plane and make short, direct connections to ground. Bypass the power-supply connections—inductance in the power-supply leads can form resonant circuits that produce response peaking or even sustained oscillations.

Circuit Analysis

To understand the operation of the VCA, we need first to consider the scaling properties of the AD834, which is actually an accurate nonlinear (two-input) voltage-controlled current source. Figure 5 shows a simplified schematic of the whole VCA.

The exact transfer function for the AD834 would show that the differential voltage inputs at X1, X2 and Y1, Y2 are first multiplied together, divided by the scaling voltage of 1 V (determined by the on-chip bandgap reference) and the resulting voltage is then divided by an accurate 250 Ω resistor to generate the output current. A simplified form of this transfer function is

$$I_W = (X_1 - X_2)(Y_1 - Y_2) \times 4mA \qquad (1)$$

where I_W is the differential current output from W1 to W2 and it is understood that the inputs X_1, X_2, Y_1, and Y_2 are expressed in volts. Thus, when both differential inputs are 1 V, I_W is 4 mA; this current is laser-calibrated to close tolerance, which simplifies the use of the AD834 in many applications. Note carefully the direction of this current in determining the correct polarity of the output connections.

It is easy to show that the output of the AD811 is

$$V_{OUT} = 2 \times I_W \times R_F \qquad (2)$$

where R_F is the feedback resistor. For R_F = 500 Ω (499 Ω is the nearest standard resistor value), the overall transfer function of the VCA becomes

$$V_{OUT} = 4(X_1 - X_2)(Y_1 - Y_2) \qquad (3)$$

which reduces to $V_{OUT} = 4\,V_G\,V_{IN}$ using the labeling conventions shown in Figure 1. As noted, the phase of the output reverses when V_G is negative. A slightly higher value of R_F is used to compensate for the finite gain of the AD811.

Both the AD811 and the AD834 can operate individually from power-supply voltages of ±5 V. However, to ensure proper operation of the AD811's input stage, the common-mode voltage at W1 and W2 must be within the common-mode range of these inputs. There are several ways to do this. We can use separate supplies of ±5 V for the AD834 and ≥ ±9 V for the AD811. Here, we have chosen to show how the VCA can be biased from one dual supply of nominally ±12 V. Figure 5 also helps to understand the dc biasing design.

We begin by deciding to place the AD834's outputs at about +5 V (a little higher than they operate in the other published applications of this product). Under dc conditions, the high open-loop gain of the op amp forces W1 and W2 to assume the same potential. We calculate the values of R_A to introduce the required 7 V drop, by considering the components of the total current in each of these resistors for the zero-signal condition.

First, when V_{OUT} = 0, the current in resistors R_F must be 10 mA (5 V/ 500 Ω). Second, the standing current into W1 and W2, due to the AD834's internal biasing, is 8.5 mA per side. Third, in this application we provide the positive supply voltage for the AD834 (at Pin 6) via resistors R_B which each carry one-half of the total supply current of 11 mA. Thus, the total current in resistors R_A is 24 mA (10 + 8.5 + 5.5 mA) and a value of 294 Ω is chosen (the closest standard value to 7 V/24 mA) for these resistors. Finally, we choose R_B to set the voltage at Pin 6 to +4 V, which is high enough to ensure accurate operation of the AD834 over the full signal and temperature ranges; the nearest standard resistor value is 182 Ω (1 V/ 5.5 mA).

The presence of these resistors (whose parallel sum is 112 Ω on each side) at the input of the op amp causes it to operate at a "noise gain" of 4.45 (499 Ω/112 Ω), but this neither has any significant effect on the dc scaling of the system, nor does it lower the closed-loop bandwidth (as would be the case for a conventional voltage-feedback op amp).

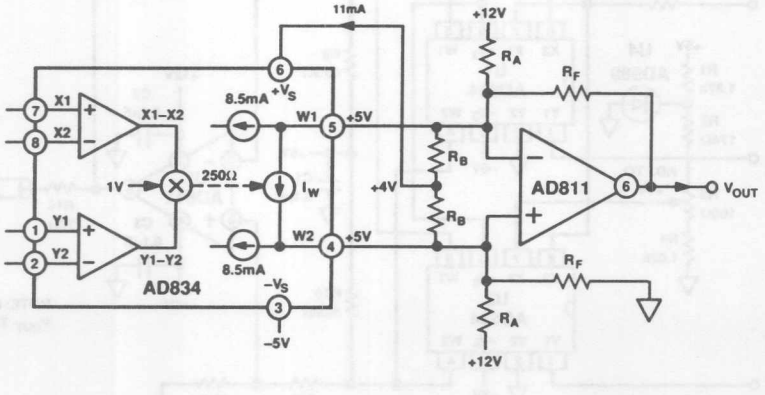


Figure 5. Simplified Schematic of the VCA for Analysis Purposes

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A VIDEO KEYER BASED ON THE VCA

Using two AD834s and adding a 1 V dc source, a special form of a two-input VCA called a video keyer (Figure 6) can be assembled. Keying is the term used in reference to blending two or more video sources under the control of a further signal or signals to create such special effects as dissolves and overlays. The circuit described here is a two-input keyer, with video inputs V_A and V_B, and a control input V_G. The output at the load is given by

$$V_{OUT} = GV_A + (1 - G)V_B \quad (4)$$

where G is a dimensionless variable (actually, just the gain of the "A" signal path) that ranges from 0 when $V_G = 0$, to 1 when $V_G = +1$ V. Thus, V_{OUT} varies continuously between V_A and V_B as G varies from 0 to 1.

The operation is straightforward. Consider first the signal path through U1, which handles video input V_A. Its gain is clearly zero when $V_G = 0$ and the scaling we have chosen ensures that it is unity when $V_G = +1$ V; this takes care of the first term in Equation 4. On the other hand, the V_G input to U2 is taken to the *inverting* input X2 while X1 is biased at an accurate +1 V. Thus, when $V_G = 0$, the response to video input V_B is already at its full-scale value of unity, whereas when $V_G = +1$ V, the differential input $X_1 - X_2$ is zero. This generates the second term in Equation 4.

To generate the 1 V dc needed for the "1–G" term, an AD589 reference supplies 1.225 V ±25 mV to a voltage divider consisting of resistors R2 through R4. Potentiometer R3 should be adjusted to provide exactly +1 V at the X1 input.

In this case, we have shown an alternative arrangement using dual supplies of ±5 V for the AD834 and ±12 V for the AD811. Also, the overall gain in this case is arranged to be unity *at the load*, when it is driven from a reverse-terminated 75 Ω line. This means that the "dual VCA" has to operate at a maximum gain of ×2, rather than ×4 as in Figure 1. However, this cannot be achieved by lowering the feedback resistor, since below a critical value (not much less that 500 Ω) the AD811 will become unstable. This is because the dominant pole in the closed-loop ac response of a current-feedback amplifier is controlled by this feedback resistor. It would be possible to operate at a gain of ×4 and then attenuate the signal at the output. Instead, we have chosen to attenuate the signals by 6 dB at the input to the AD811; this is the function of R8 through R11.

The −3dB bandwidth is about 85 MHz and the gain is flat within ±0.1 dB to 30 MHz (Figure 7). Output noise and signal isolation with either channel fully off and the other fully on is about −60 dB to 20 MHz. The feedthrough at 100 MHz is limited primarily by board layout.

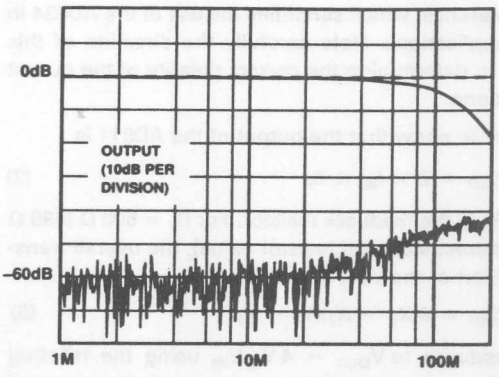


Figure 7. AC Response of the Video Keyer, at V_G = Zero and +1 V; Feedthrough Is About −60 dB

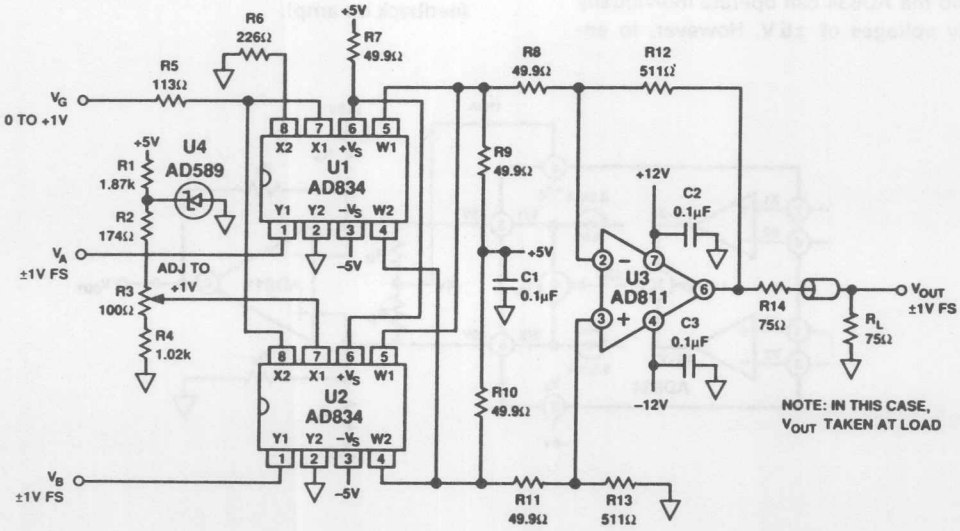


Figure 6. A Two-Input Video Keyer Based on the VCA

A FEEDBACK KEYER

The gain accuracy of the "VCA-based" keyer is dependent on the feedback resistor, R_F. Also, any nonlinearity in the multipliers will show up as a differential gain error. Using an alternative technique, in which the feedback is routed back to unused signal inputs on the AD834s, we can eliminate the feedback resistor and achieve higher accuracy. In the design shown here, we have also used a level-shifting network between the AD834 and the AD811 that eliminates the need for separate power supplies for the two ICs. (In fact, this technique can also be used in the VCAs.)

The basic idea is shown in Figure 8. Note first that V_{OUT} is returned to the inverting inputs Y2 of the multipliers and that their outputs are added. The sum is forced to zero by the assumed high open-loop gain of the op amp. Multiplier M1 produces an output $G(V_A–V_{OUT})$, while M2 produces an output $(1–G)(V_B–V_{OUT})$, where G is $V_G/(1\ V)$ and ranges from 0 to 1. Therefore, the complete system is described by the limiting condition

$$G(V_A–V_{OUT}) + (1–G)(V_B–V_{OUT}) \rightarrow 0 \qquad (5)$$

which requires that

$$V_{OUT} = GV_A + (1–G)V_B \qquad (6)$$

exactly as required for a two-input keyer. The summation of the differential current-mode outputs of the two AD834s is simply achieved by connecting together their respective W1 and W2 nodes. The resulting signal—essentially the loop error represented by the left-hand side of Equation 5—is forced to zero by the high gain of an AD811 op amp.

Figure 9 provides a practical embodiment of these ideas. The gain-control details to provide G and (1–G) terms

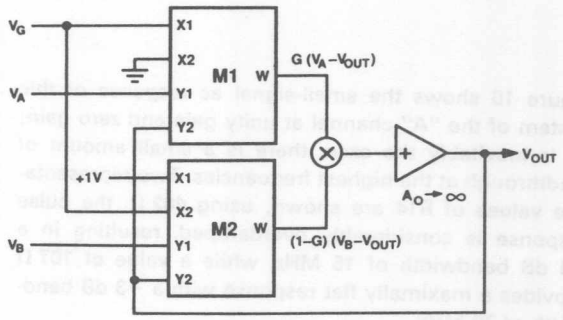


Figure 8. Elements of a Feedback Keyer

are identical to those used previously. The bias currents required at the output of the multipliers are provided by R8 and R9. A dc-level-shifting network comprising R10/R12 and R11/R13 ensures that the input nodes of the AD811 are positioned within an acceptable common-mode range for this IC. At high frequencies, C1 and C2 bypass R10 and R11, respectively.

R14 is included to lower the HF loop gain, and is needed because the voltage-to-current conversion in the AD834s, via the Y2 inputs, results in an effective value of the feedback resistance of 250 Ω (see Figure 5); this is only half the minimum value of 500 Ω required for HF stability of the AD811. (Note that this resistance is unaffected by G: when G = 1, all the feedback is via U1, while when G = 0 it is all via U2.) Resistor R14 reduces the fractional amount of output current from the multipliers into the current-summing inverting input of the AD811, by sharing it with R8. This resistor can be used to adjust the bandwidth and damping factor to best suit the application.

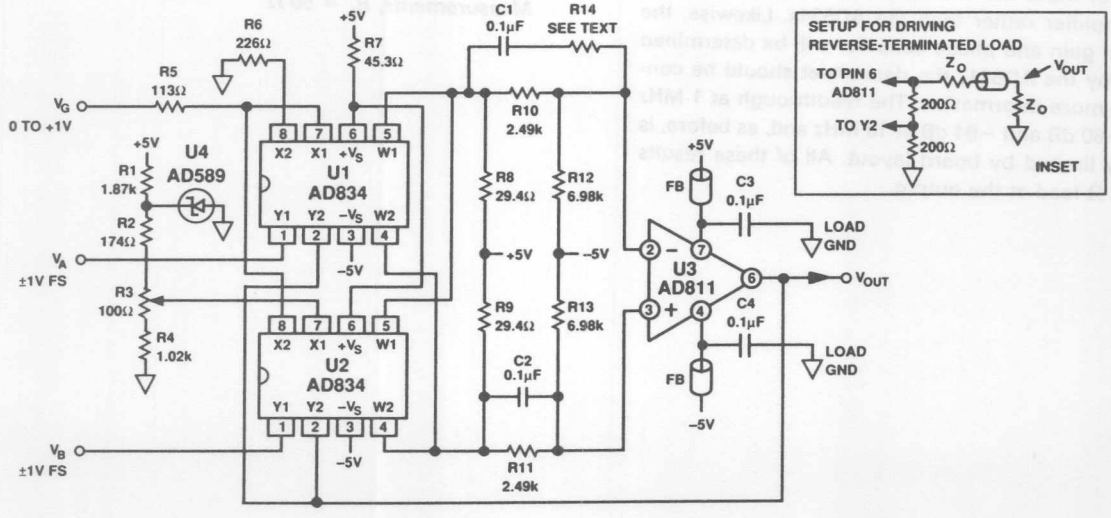


Figure 9. A Practical Embodiment of a Feedback Keyer. The Inset Shows the Feedback Configuration (Gain of ×2) for Driving a Reverse-Terminated Load.

Figure 10 shows the small-signal ac response of this system of the "A" channel at unity gain and zero gain; as is inevitably the case, there is a small amount of feedthrough at the highest frequencies. Two representative values of R14 are shown; using 402 Ω, the pulse response is considerably overdamped, resulting in a −3 dB bandwidth of 15 MHz, while a value of 107 Ω provides a maximally flat response with a −3 dB bandwidth of 70 MHz.

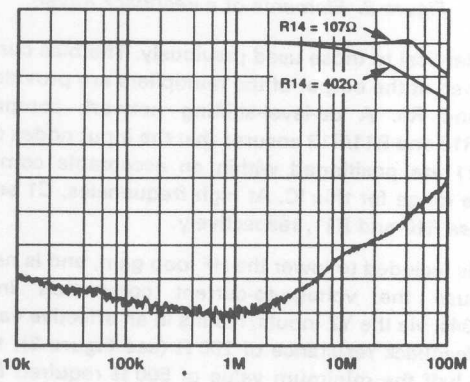
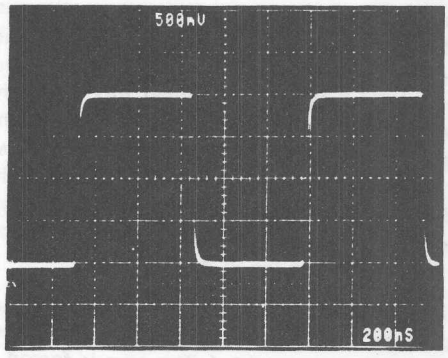
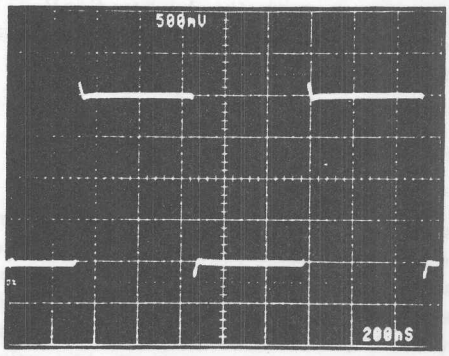


Figure 10. AC Response of the Feedback Keyer. For V_G = +1 V, the −3 dB Bandwidth Is 15 MHz Using R14 = 402 Ω and 70 MHz with R14 = 107 Ω. For These Measurements, R_L = 50 Ω

Figure 11 shows the pulse response at unity gain: in (a) R14 = 402 Ω, while in (b) R14 = 107 Ω. The frequency and pulse responses of the "B" channel, and of the gain-control input are the same, being limited by the output amplifier rather than the AD834s. Likewise, the differential gain and phase behavior will be determined primarily by the AD811; the data sheet should be consulted for more information. The feedthrough at 1 MHz is about −80 dB and −64 dB at 10 MHz and, as before, is eventually limited by board layout. All of these results used a 50 Ω load at the output.



a.



b.

Figure 11. Pulse Response of the Feedback Keyer. In (a), R14 = 402 Ω While in (b), R14 = 107 Ω. For These Measurements, R_L = 50 Ω

Unlike Figure 6's circuit, this keyer provides unity-gain operation. In applications where a reverse-terminated line (50+50 Ω or 75+75 Ω) is to be driven, the gain can be doubled by the inclusion of a resistive divider between V_{OUT} and the Y2 pins; equal resistors of 200 Ω can be used (see the inset in Figure 9). This halving of the feedback voltage also lowers the bandwidth, which can now be restored by reducing, or even eliminating, R14. Figures 12 and 13 show the modified circuit's performance when driving a 50 Ω reverse-terminated line.

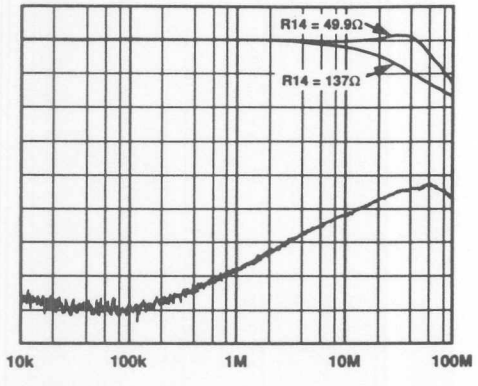
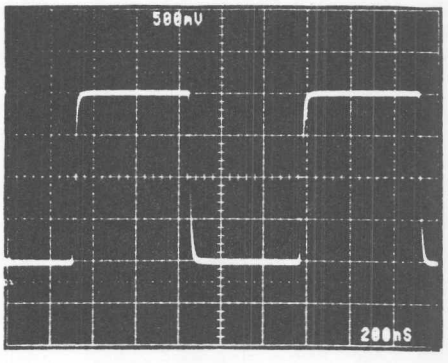
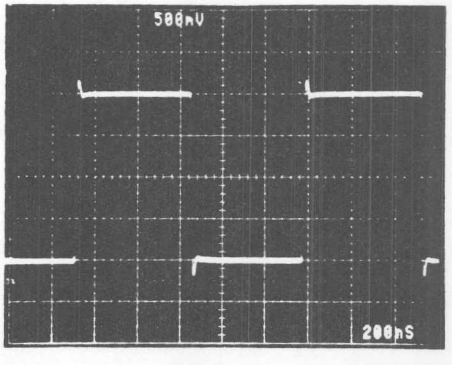


Figure 12. AC Response of the Feedback Keyer, Now Configured for a Gain of ×2. For V_G = + 1 V, the −3 dB Bandwidth Is 15 MHz Using R14 = 137 Ω and 70 MHz with R14 = 49.9 Ω. For These Measurements, R_L = 50 Ω



a.



b.

Figure 13. Pulse Response of the Feedback Keyer Now Configured for a Gain of ×2. In (a), R14 = 137 Ω While in (b), R14 = 49.9 Ω. For These Measurements, R_L = 50 Ω

SECTION X
UNUSUAL APPLICATIONS FOR OP AMPS

- Where do Op Amps Come From?
- What Really is An Op Amp?
- Basic Assumptions About Op Amps
- Novel Applications:
  Gain in the Feedback Loop, Composite Amplifiers, Abusing the Null Pins, Op Amps Without Feedback, Maltreatment of the Compensation Pins, Shunt-Mode Operation, Supply Sensing, Computer Simulation
- Op Amps Used as Comparators

SECTION X

UNUSUAL OP AMP APPLICATIONS

DEREK BOWERS, JAMES BRYANT

PERVERTING THE MONOLITHIC OP AMP

DEREK F. BOWERS

INTRODUCTION

The background behind this section started out fairly innocently. I have childhood memories of using small screwdrivers as brad awls and micrometers as glue clamps. I also remember converting the sledge (that had been carefully built by my father) in conjunction with some ladders and the garden shed into my first and only venture into roller coaster design.

By the time my career in electronics was underway, I had devised a veritable cornucopia of dubious practices. I showed my colleagues how to strip enamelled wire with a Bunsen burner and a jar of methanol, to purloin (somebody else's) nail-clippers for trimming coaxial braid, and employ an electric toaster as a test load for audio power amplifiers. Obviously, the designers of such artifacts had failed to elucidate the endless possibilities for their misuse.

Inevitably, I suppose, the operational amplifier was bound to fall victim to my natural predisposition to explore all possibilities, no matter how unconventional they might be. What surprises me, however, is how much material I have found from other sources. Apparently, I am by no means alone.

I think I can show that the op-amp, in being such a general element, is rarely used in the exact manner for which it was designed. I also firmly believe that regarding an op-amp in its purely conventional role is missing out on a lot of potential applications.

This section explores the unusual possibilities of present-day op-amps, while pointing out some of the pitfalls in designing with this universal component.

WHERE DO OP AMPS COME FROM?

I will not attempt to provide any form of history of negative feedback theory here, but suffice it to say that the first recognizable op-amp topologies seem to have evolved from work done by Lovell and Parkinson in the design of the Western Electric Nark-9 Gun Director during World War II. The actual term *operational amplifier* was not coined until 1947, however, in a paper by Ragazzini and colleagues [1].

Ragazzini described a vacuum-tube design producing a high gain amplifier capable of driving a feedback network to force a virtual earth. Such an amplifier is capable of realizing the 'classical' operations such as inversion, differentiation and integration; the major operations of an analog computer.

The next step in the evolution of the op-amp comes from the realization that the virtual earth can actually be an extra

(non-inverting) input, an advance generally attributed to Carl S. den Brinker. Now we start to see the basis of the familiar modern op-amp concept, though I pleasurably note that we are already starting to bend the rules.

WHAT REALLY IS AN OP AMP?

Using an op-amp is a little like buying a car. One specifies the color, seat material, make of sound equipment etc., but never that the vehicle must have four wheels and an engine. This is taken for granted.

Similarly, op-amps have pages of specifications such as offset voltage, gain, slew rate and so on, but it is almost always presumed to behave as a basically functional amplifier. Such an assumption is only guaranteed by the design (of course) but also by the test methodology involved.

Suffice it to say that the modern day op-amp should behave as a gain element presenting extremely high differential gain, very low common mode gain, and stability when some amount of feedback (often 100%) is applied from the output to the inverting gain terminal.

The validity of such a simplistic model is questionable, and given more space, I would explore this point further. However, for present purposes, I propose that the monolithic op-amp be regarded as an almost ideal voltage amplifier; a reasonable viewpoint in the light of all the possible permutations for its use; particularly those described in the following discourse.

BASIC ASSUMPTIONS ABOUT OP AMPS

The vast majority of monolithic op-amps are tested (and therefore specified) by a series of tests within an externally compensated test loop, which I believe originated at Tektronix, Incorporated. While making all the usual DC measurements possible, such a test loop in no way simulates the way an actual op-amp will be used. Many manufacturers (including Analog Devices) have implemented additional tests to measure noise, stability, slew rate et cetera, but the fact remains that without knowing the precise feedback circuitry around the device, the final performance can never be completely guaranteed. But experience shows that these tests are more-or-less adequate for the vast majority of applications. The "vast majority" of applications includes areas where the op-amp is used with some sort of passive feedback to form voltage amplification, inversion, or with reactive feedback to provide the function of active filters, integrators or differentiators. Most op-amp "cookbooks" also dabble in areas such as logarithmic amplifiers, where nonlinear gain is introduced inside the feedback loop. Alas, when an op-amp is employed in such a manner many of the manufacturer's tests (and data sheet curves) are rendered invalid.

But all this is fairly standard for analog components. Attempting to test a transistor, for example, to guarantee performance under every conceivable operating condition is clearly ludicrous. But good analog engineers understand transistors, and don't need a fifty page manual in order to use them. Similarly, a good understanding of op-amps is necessary for their successful inclusion in all but the simplest of systems. Proceeding one step further yields some circuits which are clearly beyond the boundaries of normal op-amp applications, but which perform highly useful functions with a minimum of complexity.

GAIN IN THE FEEDBACK LOOP

Perhaps the first departure from the classical op-amp usage is when some form of gain or nonlinearity is added into the feedback loop. Frequency compensation is a major issue here, partly because the feedback components introduce additional phase shift, but also because there is a possibility of the overall feedback becoming greater than 100%. This can cause problems for even the most "unity-gain stable" op-amp. Another caveat involves input voltage range; remember early op-amps such as the 709? This device had an output voltage swing greater than its input voltage range. Even worse, the device suffered phase reversal when this range was exceeded. The result was that it had a strong tendency to latch-up in unity gain applications. Most modern op-amps are designed to avoid this, but all bets are off if active devices in the feedback loop are used. Techniques to avoid this are similar to those needed when shunt-mode operation is employed, and will be dealt with in due course.

Dealing with the frequency compensation issue can be somewhat tricky also.

Figure 10.1 shows a fast logarithmic amplifier which I designed as an application for the MAT-02 ultra-matched NPN dual transistor. The circuit details are covered in the MAT-02 data sheet, but essentially revolves around non-linear (potentially high-gain) feedback for both of the op-amps. The basic trick for ensuring stability is to provide a capacitor from the output to the inverting input for both amplifiers (Cl & C2), assuming them to be unity-gain stable (which in this case they are). This capacitor bypasses the non-linear feedback at frequencies critical to the amplifier's stability. At the higher input currents, however, The dynamic emitter impedance of Ql appears in parallel with C2, reducing its effectiveness. The obvious solution of increasing C2 would lead to slow performance at lower currents. The addition of R4 circumvents this problem by swamping the dynamic resistance term, thus allowing a smaller value of C2. It is desirable that R4 be made as large as possible, but its upper limit is set by the output swing capability of Al.

COMPOSITE AMPLIFIERS

Another purpose of adding gain inside the feedback loop is to improve the op-amp's input characteristics. Figure 10.2 is an ultra-low noise op-amp, created by adding an additional gain stage to an OP-27 [2]. The three parallel MAT-02 transistor pairs, running at 1mA per transistor, yield a voltage noise spectral density of only $500pV/\sqrt{Hz}$. The 6mA tail current is generated by Q4, which is biased by a red LED. The LED has about one volt more forward voltage drop than the transistor, but about the same temperature coefficient, generating a stable voltage across R12 (yes, I know that LED's aren't designed to do this, but micrometers aren't intended to be glue clamps either). Resistors R1-R3 ensure equal splitting among the devices.

FAST LOG AMP CIRCUIT

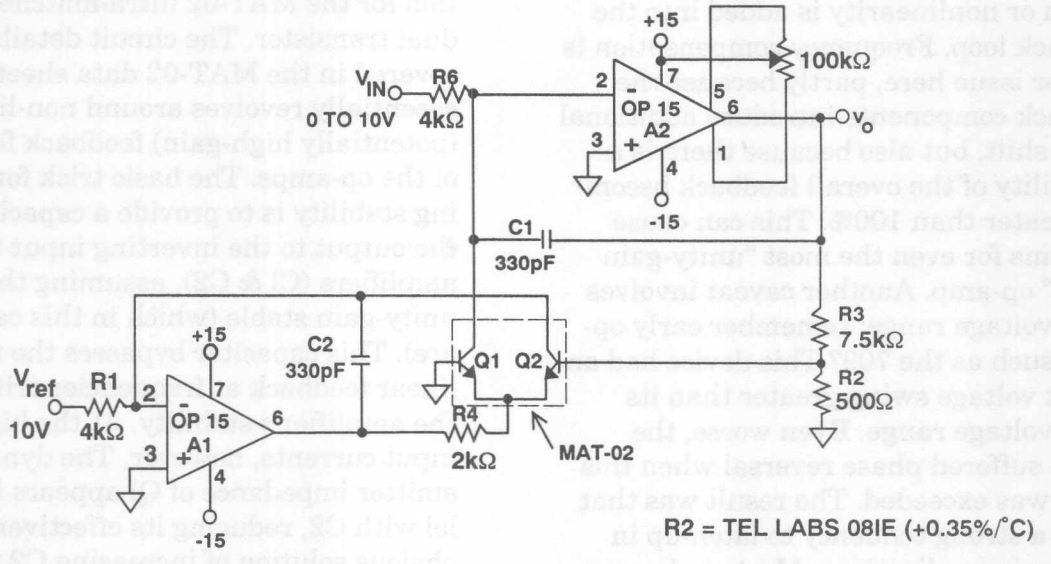


Figure 10.1

ULTRA LOW-NOISE COMPOSITE OP AMP USING ADDITIONAL GAIN STAGE

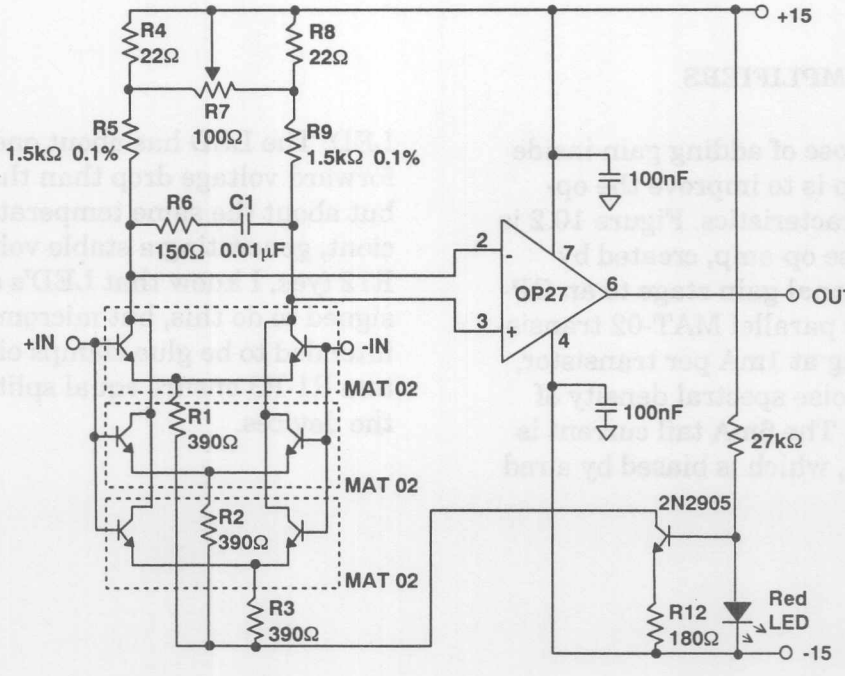


Figure 10.2

Frequency compensation is provided by R6 and Cl. The Idea here is to create a dominant pole with Cl and add a zero to accommodate the natural frequency compensation of the OP-27. The overall amplifier is compensated for gains of ten and above, since we couldn't really see why anybody would use such a low-noise amplifier at lower gains.

While such frequency compensation does work, it is difficult to optimize for a wide range of gains, and of course, yields amplifiers which are slower than those with less gain stages. Figure 10.3 shows a way around this [3].

The input stage of the SSM-2134 op-amp can be by-passed by feeding signals to its null pins. Furthermore, the internal input stage can be shut off by connecting pins 2 & 3 to the negative supply. Two drain resistors (Rd) parallel the internal SSM-2134 collector resistors, and the input stage (in this case a dual JFET) is biased by tail resistor Rs. Adding some extra components produces an extremely high performance JFET input op-amp as shown in Figure 10.4.

Here, a FET cascode pair reduces input bias current (<2pA), and a constant current source replaces the tail resistor for improved CMRR. For best circuit performance, the drain current is adjusted to produce a 2.5V drop across the drain load resistors. Next, the CMRR trim is adjusted to optimize this parameter. Finally, the input offset can be trimmed out. The overall amplifier has a $2nV/\sqrt{Hz}$ input noise voltage and a $50V/\mu s$ slew-rate without compensation. compensation capacitor Cc (on the order of a few tens of picofarads) can be added if capacitive loads need to be driven.

USING OFFSET NULL PINS TO CREATE JFET INPUT COMPOSITE

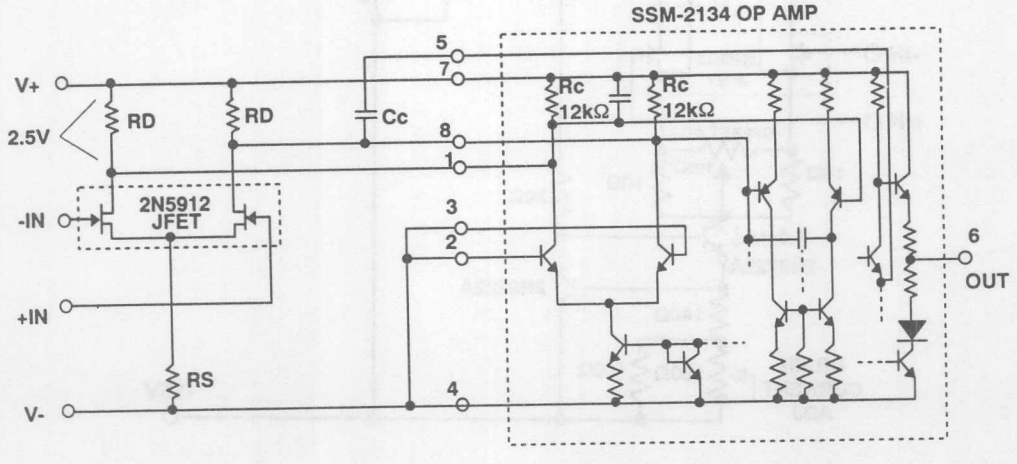


Figure 10.3

Another technique for producing composite amplifiers is shown in Figure 10.5. Here, a fast JFET input op-amp is corrected for DC errors by a slow but accurate superbeta input amplifier. The OP-97 continuously monitors the offset voltage of the OP-42 and forces it to near zero via the null pins of the latter amplifier. The external resistors are chosen to give realistic voltage swings at the output of the OP-97, and the factor of two difference yields an approximately symmetric correction range. Such amplifiers feature the full bandwidth and slew rate of the main amplifier, coupled with the DC precision of the correction amplifier. Settling time, however, is usually degraded because transient errors cannot be corrected quickly by the slower op-amp.

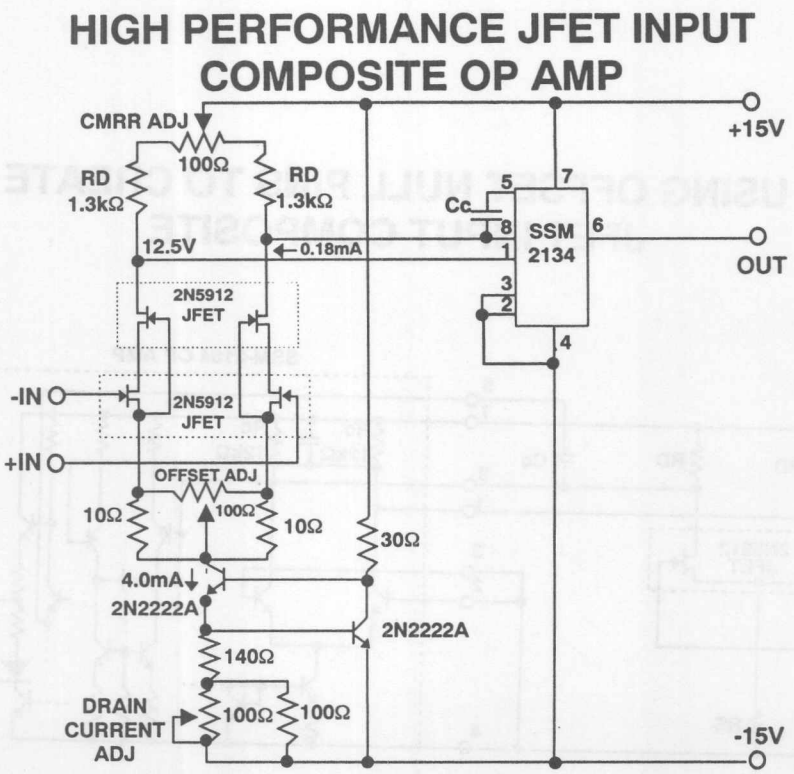


Figure 10.4

COMPOSITE AMPLIFIER USING FAST JFET INPUT OP AMP AND PRECISION SUPERBETA INPUT OP AMP

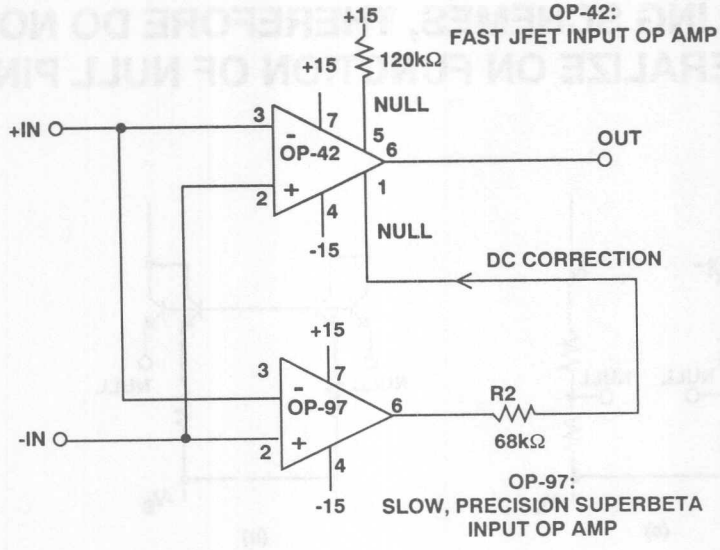


Figure 10.5

FURTHER ABUSES OF THE NULL PINS

The circuits of Figure 10.3 & Figure 10.4 rely on the fact that the null pins of an SSM-2134 give direct access to the internal load resistors. This is not generally true for op-amps, though these pins do provide a possible extra pair of inputs (or feedback points) for the op-amp (the popular 741 amplifier actually has higher gain at its null pins than at the inputs). There is a caveat here, however. Most op-amps have a nulling arrangement equivalent to that shown in Figure 10.6a, where nulling is intended to the negative supply. Some however, have the nulling at the positive supply. Usually, pins 1 & 5 are used for negative supply nulling, and pins 1 & 8 are used for positive supply nulling, but there are exceptions; the OP-160 and AD847 for example. Occasionally, a scheme such as that in Figure 10.6b is used, and in general op amps using such a topology are best avoided for applications such as that of Figure 10.5.

It is dangerous to generalize the function of null pins, but the 741-type of nulling scheme offers an inverting function at pin 5 and a non-inverting one at pin 1, level shifted (of course) down to the negative supply rail. This is the convention we tend to follow at the PMI division of Analog Devices. This, for example means that overcompensation of an op-amp can be achieved with a capacitor from the output to pin 5. Figure 10.7 is another way to use these pins [4], a rather unusual approach to a single-supply instrumentation amplifier, with an input and output range which includes ground.

DIFFERENT OP AMPS USE DIFFERENT NULLING SCHEMES, THEREFORE DO NOT GENERALIZE ON FUNCTION OF NULL PINS

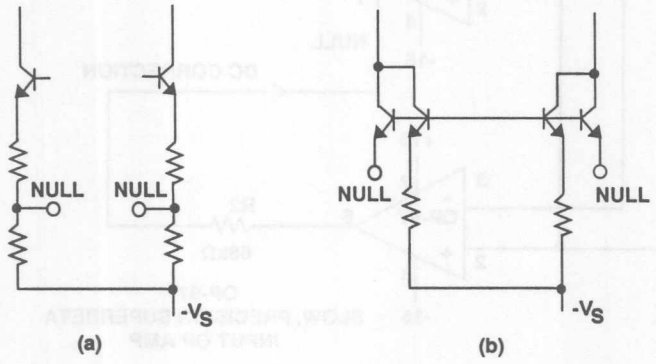


Figure 10.6

SINGLE-SUPPLY INSTRUMENTATION AMPLIFIER USING NULL PIN FOR FEEDBACK CONNECTION

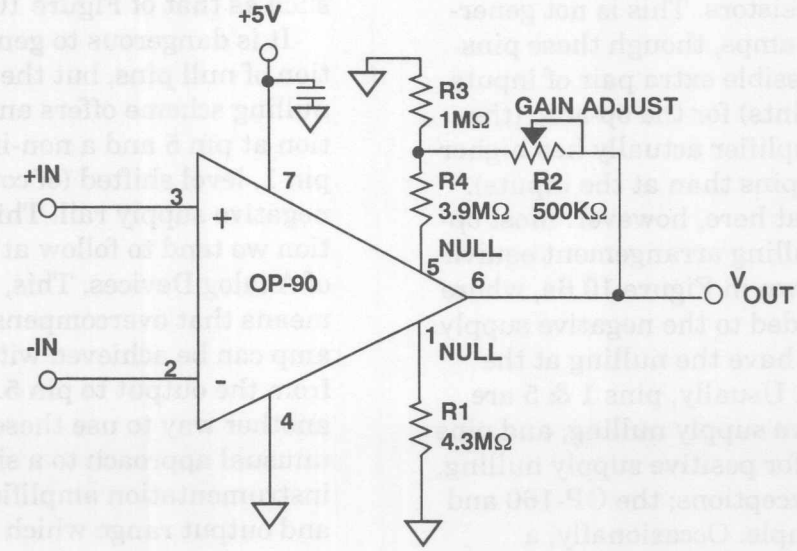


Figure 10.7

Feedback is provided via pin 5 of the OP-90, which frees up both the inputs for differential signal handling. Distortion is that of a differential pair; so this type of amplifier is only suitable for high gain applications. At a gain of 1000, linearity measures about 0.05% over a 2.5V output range. A gain trim is always necessary with this type of configuration because of internal tolerances associated with the internal nulling circuitry, but the values shown are designed for a gain of 1000. The OP-90, incidentally, has temperature compensated input stage transconductance, and in this application gain drift is only 50ppm/K.

The very low power bandgap reference of Figure 10.8 is another example of constructive abuse of the null pins (OP-90 data sheet for an official reference, but yet another of my strange creations). The overall circuit generates a low temperature coefficient 1.23 volt output with supplies from 2.5V to 36V, with only 17μA of supply current. When adjusted, the output drift is about 20ppm/K, but lower drift can be achieved by optimizing the output voltage; a 1% change produces a predictable 33ppm/K temperature drift. A significant problem with this type of circuit is ensuring reliable start-up. When no current is flowing through R1 & R2, the op-amp is beyond its positive input-range limit and has an undefined output state. To prevent this, one of the null pins (pin 5) is shorted to ground, forcing the output to a high state at power-up. This does introduce a few millivolts of offset at the amplifier's inputs, but this is not important in this application, since the offset is proportional to temperature, and therefore trims out when the output adjust is performed.

LOW-POWER BANDGAP VOLTAGE REFERENCE

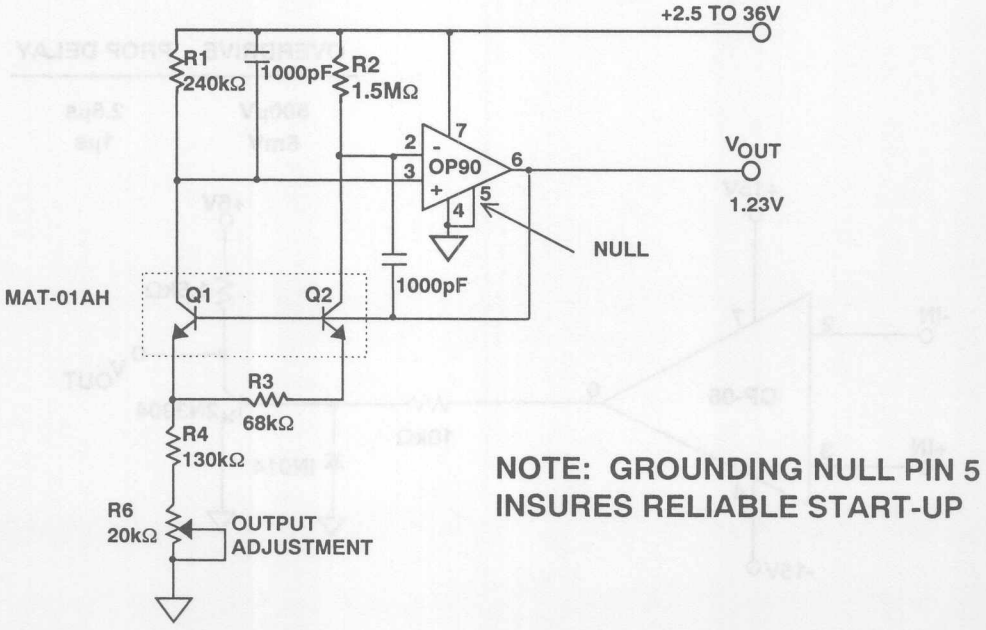


Figure 10.8

10

OP AMPS WITHOUT FEEDBACK

With the availability of the plethora of monolithic comparators available, at first glance it seems pointless to attempt to warp an op-amp into this function. But no available comparators have the precision performance of high-grade op-amps, and precision op-amps without internal compensation (such as the OP-06) can be surprisingly fast where low overdrive response is needed [5]. The circuit of Figure 10.9 delivers a TTL compatible output with a response time of about 1μs for 5mV overdrive, and 2.5μs for a 500μV overdrive.

Some op-amps feature a compensation pin which closely tracks the output voltage. This enables the output to be clamped at TTL levels with a zener diode (Figure 10.10), making comparator design quite painless.

COMPARATOR MADE FROM UN-COMPENSATED PRECISION OP AMP

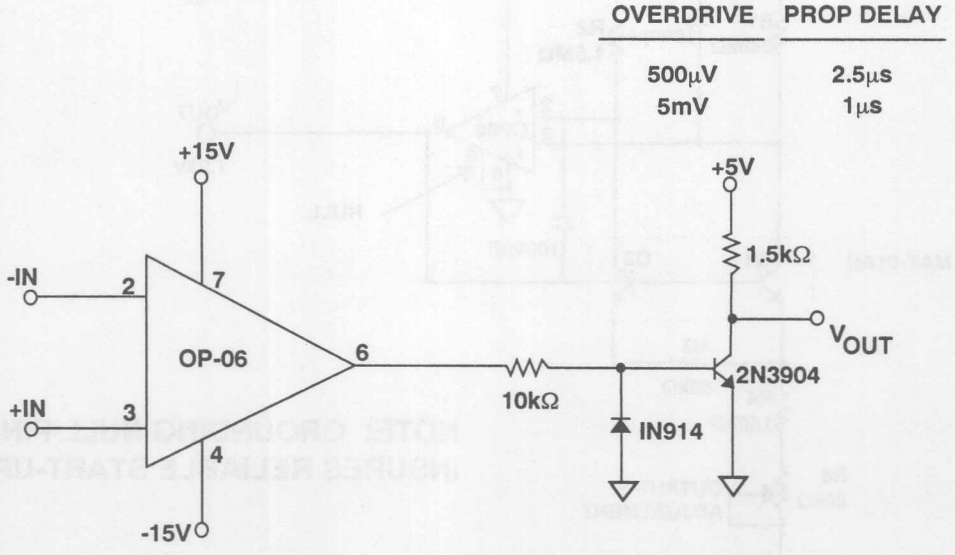


Figure 10.9

USING COMPENSATION PIN TO CLAMP OP AMP OUTPUT TO TTL LEVELS

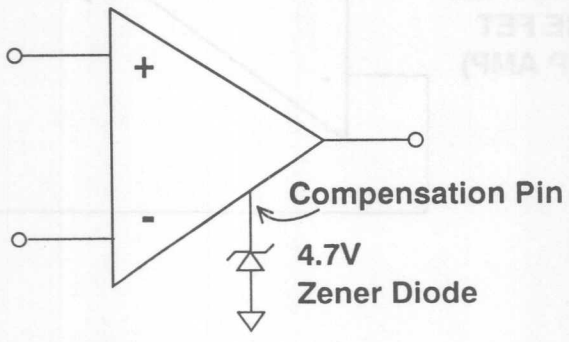


Figure 10.10

One possible problem when using op-amps without feedback is that large differential input voltage may be permanently present. Older NPN input op-amps could break down (with a subsequent degradation in input precision) under these conditions, but most are protected by clamp diodes these days. Even so, a substantial input current will flow when these are turned on, and this should be taken into consideration.

Even when feedback is employed, some circuits rely on correct operation when the feedback loop is broken. One example is the series-mode precision rectifier of Figure 10.11, which can also be used as a peak detector if R1 is replaced by a capacitor. This circuit requires a high input impedance under all conditions. Amplifiers with FET or lateral PNP inputs are good for this type of application.

SERIES-MODE PRECISION RECTIFIER

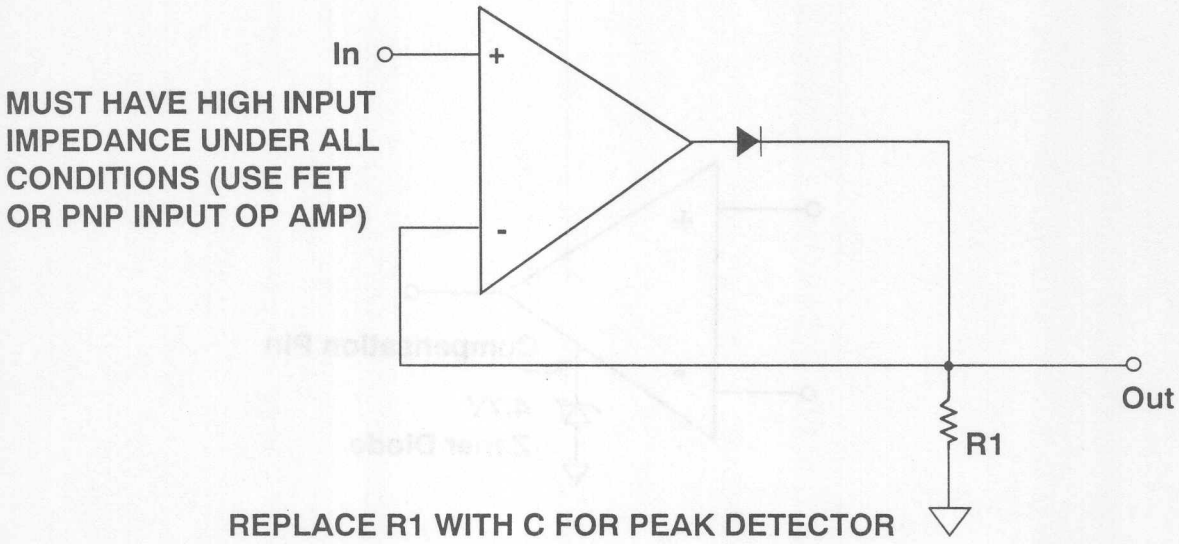


Figure 10.11

MORE MALTREATMENT OF THE COMPENSATION PINS

As mentioned earlier, some op-amps have a compensation pin which closely tracks the output. This can be used as a general purpose clipping function [6]. Referring to Figure 10.12, bias voltages for two back to back diode clamps are provided by a resistor string. Such a circuit is useful for preventing gross overdrive of analog switches, A/D converters etc.

There are also some quite ingenious ways of compensating op amps. Figure 10.13 is full-wave precision rectifier of the usual two op-amp type. Al is a type usually compensated by a capacitor from the output to pin 8. In this case however, two capacitors are used, connected to the output side of the feedback diodes [7]. This effectively disconnects the compensation when the diodes turn off, removing much of the usual 'dead-band' as the input swings through zero. I have done all sorts of other things with compensation pins, including using them to parallel op-amps. But these days even I have my limits.

USING OP AMP COMPENSATION PIN FOR CLIPPING

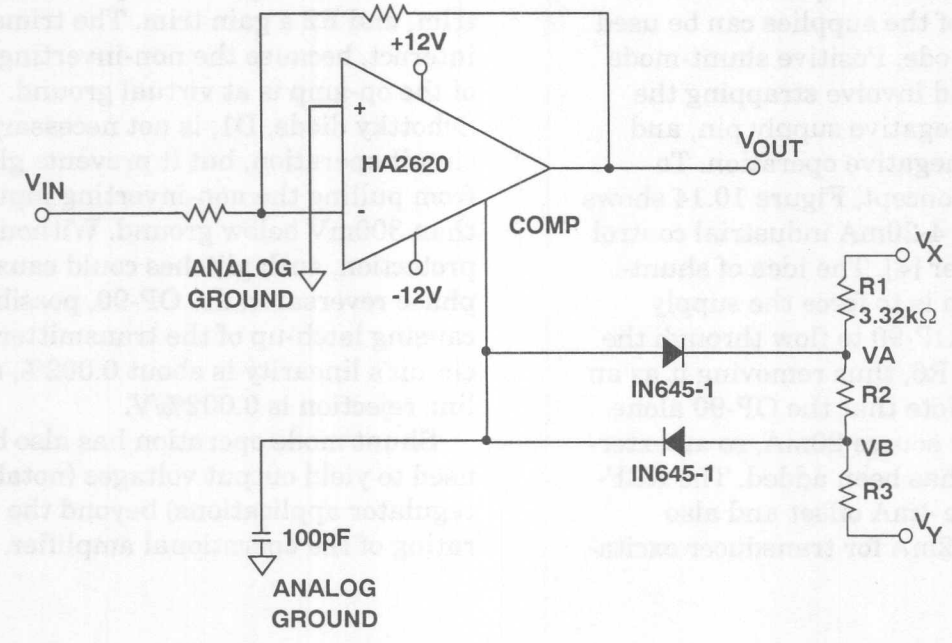


Figure 10.12

PRECISION FULL-WAVE RECTIFIER MINIMIZES ZERO-VOLT "DEADBAND"

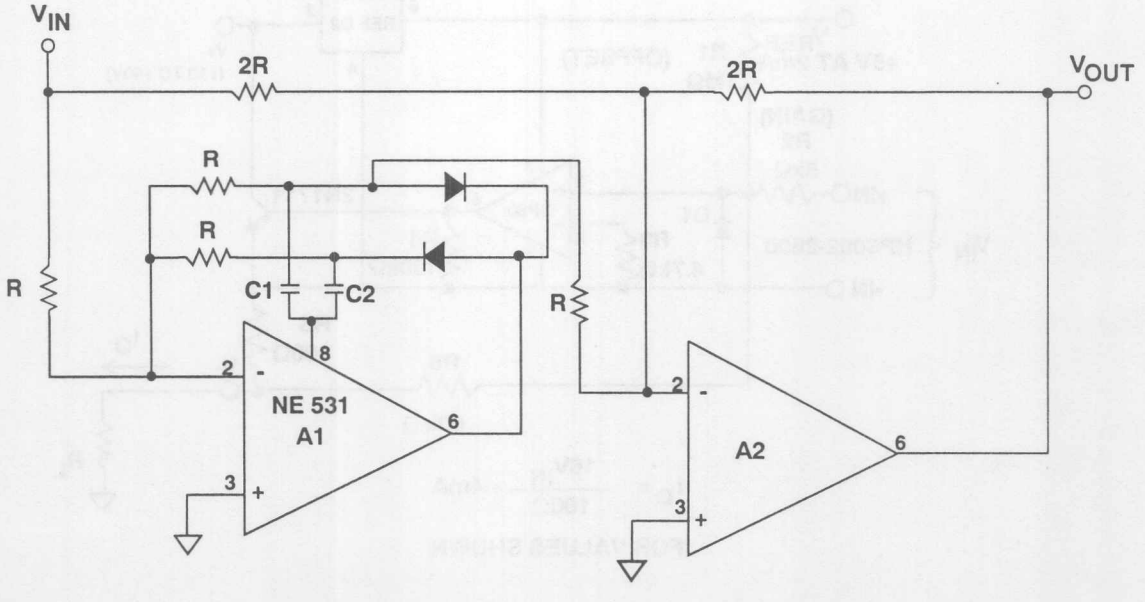


Figure 10.13

SHUNT-MODE OPERATION

Op-amps which can operate with the output at one of the supplies can be used in the shunt-mode. Positive shunt-mode operation would involve strapping the output to the negative supply pin, and vice versa for negative operation. To illustrate the concept, Figure 10.14 shows a fully floating 4-20mA industrial control loop transmitter [4]. The idea of shunt-mode operation is to force the supply current of the OP-90 to flow through the sense resistor, R6, thus removing it as an error source. Note that the OP-90 alone cannot directly source 20mA, so an external transistor has been added. The REF-02 provides the 4mA offset and also supplies up to 2mA for transducer excitation. If necessary, R1 can provide an offset trim, and R2 a gain trim. The trims do not interact, because the non-inverting input of the op-amp is at virtual ground. The Schottky diode, D1, is not necessary for circuit operation, but it prevents glitches from pulling the non-inverting input more than 300mV below ground. Without this protection, such glitches could cause phase reversal in the OP-90, possibly causing latch-up of the transmitter. The circuit's linearity is about 0.002%, and its line rejection is 0.002%/V.

Shunt mode operation has also been used to yield output voltages (notably in regulator applications) beyond the voltage rating of the operational amplifier.

FLOATING 4-TO-20mA TRANSMITTER ILLUSTRATES SHUNT-MODE OPERATION

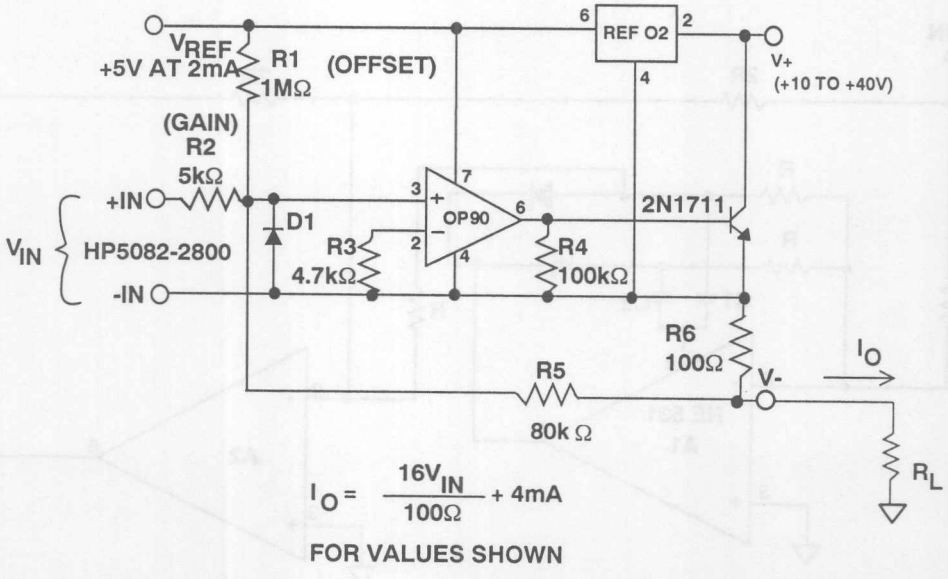


Figure 10.14

SUPPLY SENSING

Just as the inputs are not the only way to get signals into an op-amp, the output is not the only way to get them out either. Figure 10.15 is a voltage to current converter based on the idea of supply sensing [8].

The basic idea is to invert the supply currents of the amplifier with transistor current "mirrors" and subtract them at I_{out}. With no input, these currents will be symmetric (except for the input bias currents of the op amp), and result in no net output current. Any input voltage will be impressed across R1, unbalancing the supply currents by an amount exactly equal to the input voltage divided by R1. This imbalance appears at I_{out} as a high-impedance current output. Op-amp voltage swings can be minimized using this approach, and because there is no feedback from the output such circuits can be made very fast. The main design problem lies in designing accurate current mirrors.

These can be formed from monolithic duals (such as MAT-02 & MAT-03), or monolithic quad packages (Analog Devices manufacturers a quad NPN, the MAT-04, and PNP quads are available from other manufacturers). Emitter generation resistors in series with the upper and lower emitter pairs can also improve accuracy, remembering that without them a 250μV V_{be} mismatch will create 1% of error.

Figure 10.16 shows an instrumentation amplifier based on the supply sensing technique. Here, an extra op-amp is added to provide a differential high impedance drive to R1. Again the supply currents of Al are subtracted and fed to R2 (the

FAST VOLTAGE-TO-CURRENT CONVERTER USING POWER SUPPLY SENSING

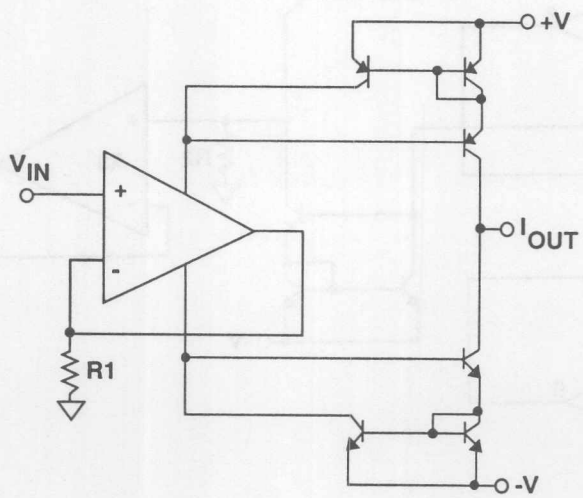


Figure 10.15

output buffer may not be necessary in some applications). The gain is simply set by the ratio of R2 to R1, and no trims are necessary to achieve high common-mode rejection. Note that the usual trick of using a dual op-amp for the input amplifiers is not practical here, because no dual of which I am aware brings out independent supplies for both amplifiers.

Figure 10.17 shows a (differential input) full-wave rectifier based on supply sensing. Here only the negative supply currents are used, and they are added instead of subtracted. Unfortunately, this leads to an output offset equal to both quiescent supply currents and this must be removed by adjustment of Rp. Figure 10.18 shows a comparison between this circuit (a)and the more conventional two op-amp configuration (b). Identical op-amps were used in both cases. For the record, the vertical scale is 1V/division, horizontal is 10μs/division and the op-amps were OP-41's, though faster amplifiers can be used of course.

It is possible to provide overall feedback around a supply sensing amplifier, and this actually results in a current feedback op-amp. This technique has been used to produce a very high performance audio amplifier [9].

INSTRUMENTATION AMPLIFIER USING POWER SUPPLY SENSING TECHNIQUE

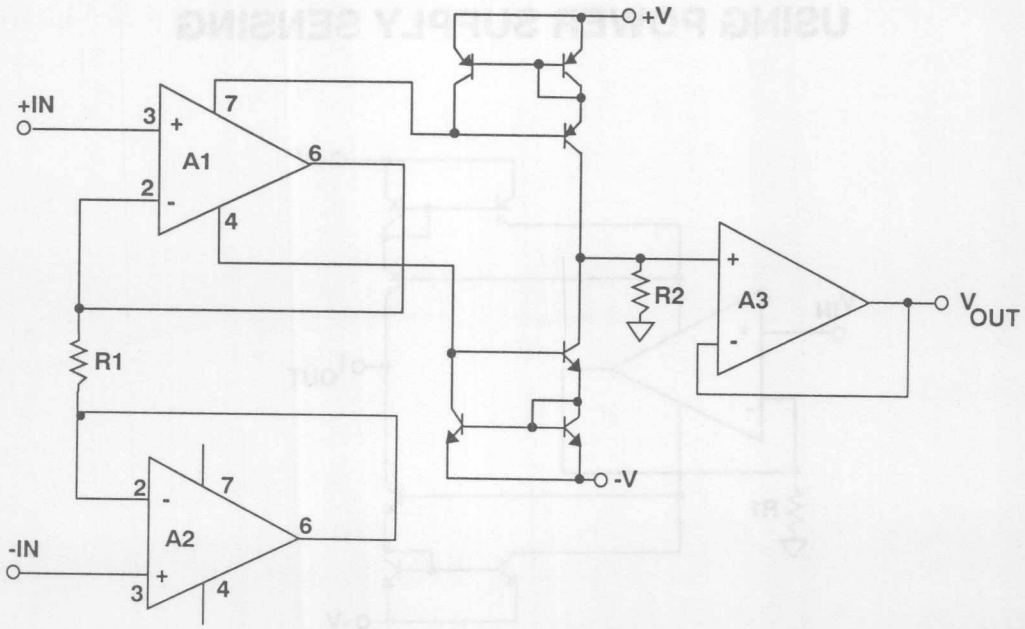


Figure 10.16

DIFFERENTIAL INPUT FULL-WAVE RECTIFIER USING POWER SUPPLY SENSING

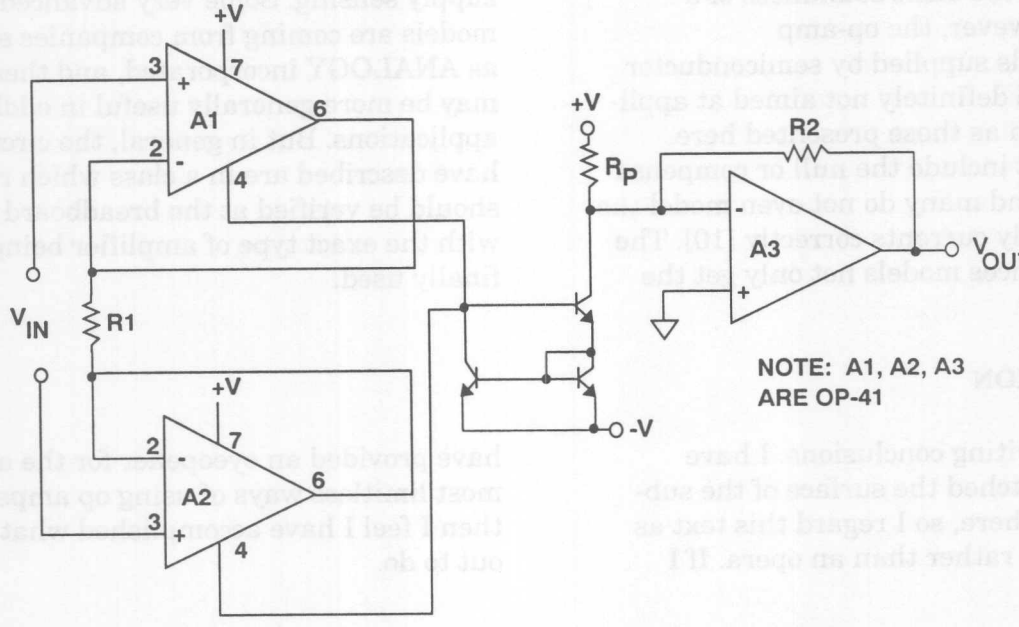
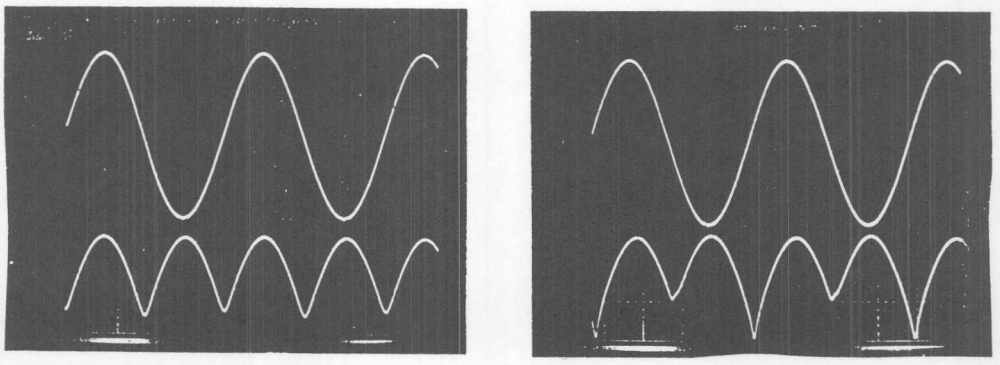


Figure 10.17

COMPARISON BETWEEN FULL-WAVE RECTIFIER USING POWER SUPPLY SENSING AND CONVENTIONAL 2 OP-AMP CIRCUIT

SUPPLY SENSING CIRCUIT

CONVENTIONAL
2 OP AMP CIRCUIT



VERTICAL SCALE: 1V/DIV.
HORIZONTAL SCALE: 10µs/DIV.

Figure 10.18

10

SOME NOTES ON COMPUTER SIMULATION

Many system designers are now using computer simulation techniques to at least verify the basic soundness of a design. However, the op-amp macromodels supplied by semiconductor vendors are definitely not aimed at applications such as those presented here. Most do not include the null or compensation pins, and many do not even model the power supply currents correctly [10]. The Analog Devices models not only get the supply currents right [11] but can also be used to simulate applications such as supply sensing. Some very advanced models are coming from companies such as ANALOGY incorporated, and these may be more generally useful in oddball applications. But in general, the circuits I have described are in a class which really should be verified at the breadboard level, with the exact type of amplifier being finally used.

CONCLUSION

I hate writing conclusions. I have merely scratched the surface of the subject matter here, so I regard this text as an overture rather than an opera. If I have provided an eyeopener for the almost limitless ways of using op amps, then I feel I have accomplished what I set out to do.

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[9) M. Alexander, *A Current Feedback Audio Power Amplifier*, **AES Preprint #2902**, presented at the 1990 AES conference in Montreaux, March 1990.

[10] G.R. Boyle et al , *Macromodeling of Integrated Circuit Operational Amplifiers*, **IEEE J. Solid-State Circuits**, vol. SC-9, Dec. 1974.

[11] M. Alexander & D. F. Bowers, *New Spice Compatible Op Amp Model Boosts ac Simulation Accuracy*, **EDN**, February 15, 1990 (and part 2, March 1 1990).

USING OP AMPS AS COMPARATORS

JAMES M. BRYANT

INTRODUCTION

A comparator is a device with two input terminals and a logic output which indicates which of the two inputs is at the higher potential. An operational amplifier is an amplifier with differential inputs, a single-ended output, and extremely high gain. Its output generally swings close to its supply rails. There is therefore a temptation to use op-amps as comparators. When faced with this temptation it is well to remember Mr. Punch's advice to those about to marry - DON'T!

Comparators are designed to work open-loop, they are designed to drive logic from their outputs, and they are designed to work at high speed with minimal instability. Op-amps are not designed for use as comparators, they may saturate if over-driven and recover comparatively slowly, many have input stages which behave in unexpected ways when used with large differential voltages, and their outputs are rarely compatible with logic.

COMPARATORS VERSUS OP AMPS

- **A COMPARATOR GIVES A LOGIC OUTPUT INDICATING THE RELATIVE POTENTIALS ON ITS TWO INPUTS**
- **AN OPERATIONAL AMPLIFIER AMPLIFIES THE DIFFERENTIAL VOLTAGE APPLIED TO ITS TWO INPUTS**

Figure 10.19

WHEN CONSIDERING USING OP-AMPS AS COMPARATORS

REMEMBER

MR. PUNCH'S ADVICE TO THOSE ABOUT TO MARRY

DON'T!

Figure 10.20

Nevertheless it is often tempting to use an op-amp as a comparator since comparators are, in general, designed for speed at the expense of some other parameters, and a suitable op-amp may have lower V_{OS}, I_b and price (especially if it is one op-amp of a chip containing four) than a comparable comparator. But it will also be much slower - an op-amp should never be used as a comparator if high speed is important to the application.

This section of the Seminar considers some of the issues to be considered when, for whatever reason, an op-amp is to be used as a comparator. Not all of them can be resolved by reference to the op-amp data sheet, since op-amps are not intended for use as comparators and are rarely specified for such an application.

The most common issues are speed (as we have already mentioned), the effects of input structures (protection diodes, phase inversion in FET amplifiers, and many others), output structures which are not intended to drive logic, hysteresis and stability, and common-mode effects.

HOWEVER

- OP-AMPS CAN HAVE LOWER:
  - OFFSET VOLTAGE
  - BIAS CURRENT
  - PRICE
- THEY WILL DEFINITELY HAVE LOWER SPEED!

Figure 10.21

ISSUES TO BE CONSIDERED WHEN USING OP-AMPS AS COMPARATORS

- *ALWAYS* SPEED
- OUTPUT LEVELS
- HYSTERESIS & STABILITY
- EFFECTS OF INPUT STRUCTURES
  - Protection Diodes
  - Phase-Inversion in BIFET Amplifiers
  - Common-Mode Range

Figure 10.22

SPEED

Most comparators are quite fast and some are very fast indeed - but so are some op-amps. Why must we expect low speed when using an op-amp as a comparator?

A comparator is designed to be used with large differential input voltages, whereas op-amps normally operate with their differential input voltage minimized by negative feedback. When an op-amp is over-driven, sometimes by only a few millivolts, some of its stages may saturate. If this occurs the device will take a comparatively long time to come out of saturation and will therefore be much slower than if it always remained unsaturated.

The desaturation time of an overdriven op-amp is likely to be considerably longer than the normal group delay of the amplifier, and will often depend on the amount of overdrive. Since few op-amps have their desaturation time specified for various amounts of overdrive it will generally be necessary to determine, by experiment, the behavior of the amplifier under the conditions of overdrive to be expected in a particular application.

WHY IS AN OP-AMP SLOWER THAN A COMPARATOR?

10

- **An Op-Amp Saturates when Over-driven Takes Time to Recover From Saturation (De-saturation Time)**

- **A Comparator is Designed NOT to Saturate**

Figure 10.23

SATURATION MAKES AN OP AMP USED AS A COMPARATOR SLOWER THAN THE SAME AMPLIFIER USED WITH NEGATIVE FEEDBACK

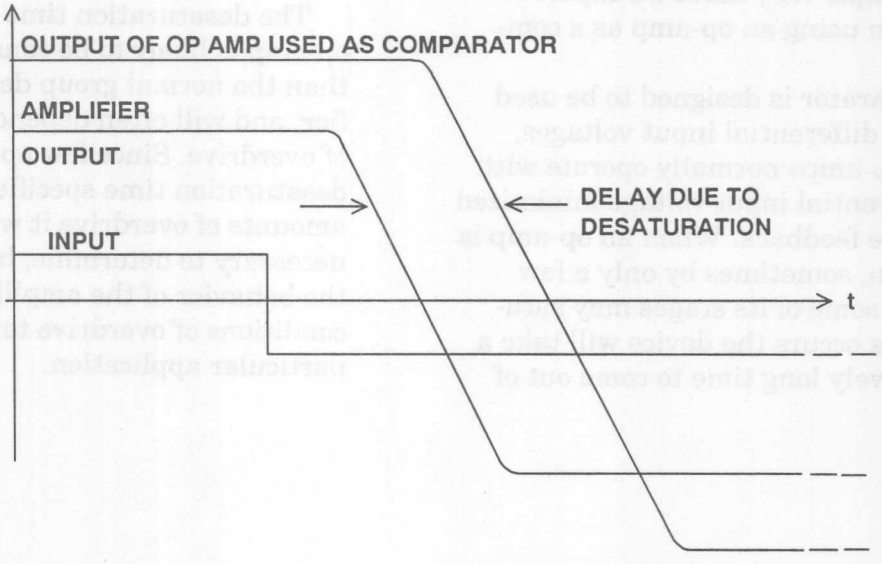


Figure 10.24

DESATURATION TIMES

- FOR VARIOUS LEVELS OF OVERDRIVE ARE RARELY SPECIFIED FOR OP-AMPS
- IT WILL BE NECESSARY TO DETERMINE THEM BY EXPERIMENT UNDER THE CONDITIONS OF THE PARTICULAR APPLICATION
- Remember that since this parameter is not specified or guaranteed it may vary quite widely from device. Test several devices from several batches and NEVER regard any set of results as typical.

Figure 10.25

The results of such experiments should be regarded with suspicion and the values of propagation delay through the op-amp comparator which is chosen for worst-case design calculations should be at least twice the worst value seen in any experiment.

OUTPUT CONSIDERATIONS

The output of a purpose-built comparator will be designed to drive a particular logic family or families, while the output of an op-amp is designed to swing from supply rail to supply rail. Frequently the logic being driven by the op-amp comparator will not share the op-amp's supplies and the op-amp rail to rail swing may go outside the logic supply rails - this will probably destroy the logic circuitry, and the resulting short-circuit may destroy the op-amp as well.

OP-AMP OUTPUTS AND LOGIC INPUTS

10

- **ARE GENERALLY INCOMPATIBLE (CMOS sharing the op-amp supply is an exception.)**
- **SOME INTERFACE CIRCUITRY IS USUALLY NECESSARY**

Figure 10.26

Of course some circuits will actually require rail-output swings from their comparator(s) and no addition interfacing is necessary. These include circuits which are not using IC logic but using the output of the comparator to switch discrete diodes and transistors, and circuits where the logic is CMOS powered from the same positive and negative supplies as the op-amp. (BEWARE: CMOS powered from the positive op-amp supply and the [center] ground rail is not included in this category - the op-amp output MUST be within the CMOS supply rails at all times.)

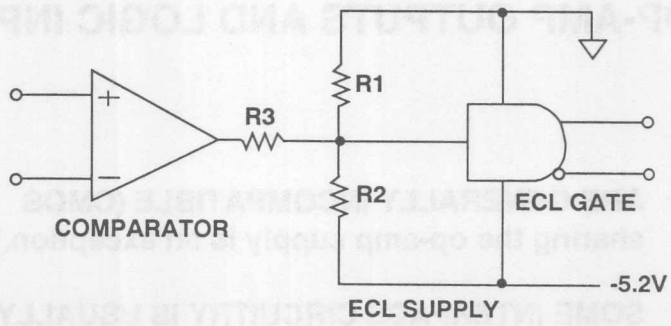
There are three types of logic which we must consider: ECL, TTL and CMOS.

ECL is a very fast current steering logic family. It is unlikely that an op-amp would be used as a comparator in applications where ECL's highest speed is involved, for reasons given above, so we shall usually be concerned only to drive ECL logic levels from an op-amp's signal swing and some additional loss of speed due to stray capacities will be unimportant. To do this we need only three resistors, as shown in Figure 10.27.

R1, R2 and R3 are chosen so that when the op-amp output is positive the level at the gate is -0.8V, and when it is low it is -1.6V. ECL is occasionally used with positive, rather than negative, supplies (i.e. the other rail is connected to ground), the same basic interface circuit may be used but the values must be recalculated.

Although CMOS and TTL input structures, logic levels, and current flows are quite different (although some CMOS is specified to work with TTL input levels) the same interface circuitry will work perfectly well with both types of logic, since they both work for logic 0 near to 0 V and logic 1 near to 5 V.

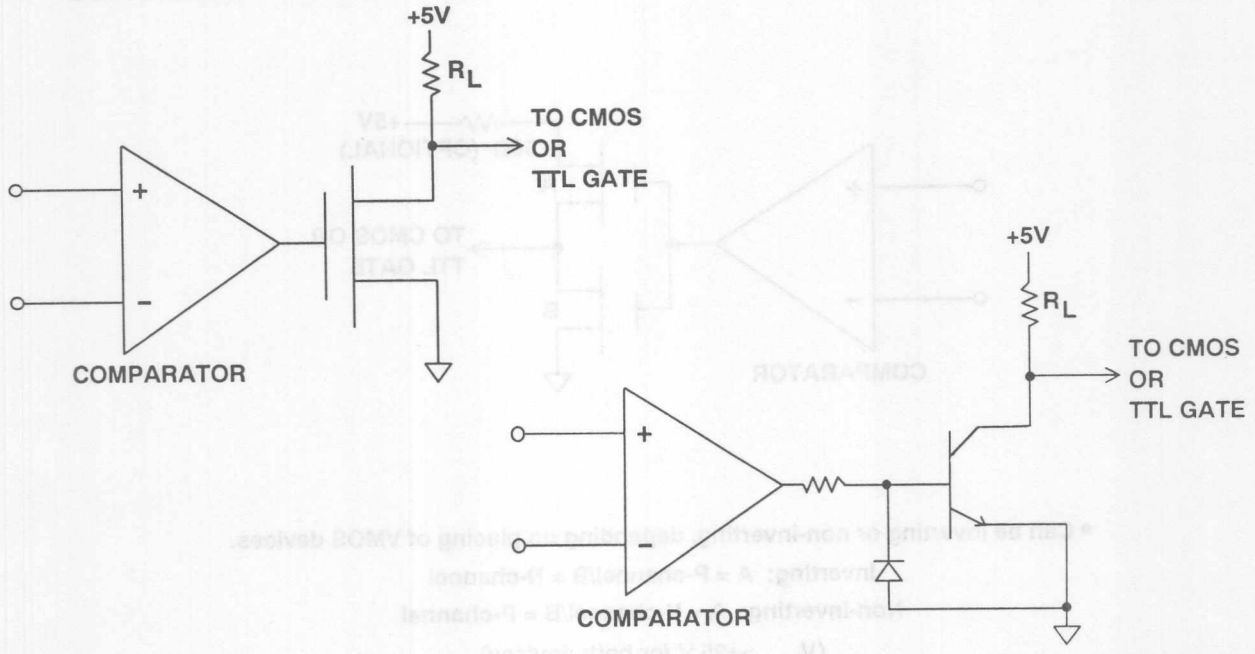
INTERFACE WITH ECL GATE



■ LOW RESISTOR VALUES WILL MINIMIZE THE EFFECT OF STRAY CAPACITANCE BUT INCREASE POWER CONSUMPTION

Figure 10.27

SIMPLE INTERFACES WITH CMOS AND TTL GATES



- Low resistor values will minimize the effects of stray capitance but increase power consumption

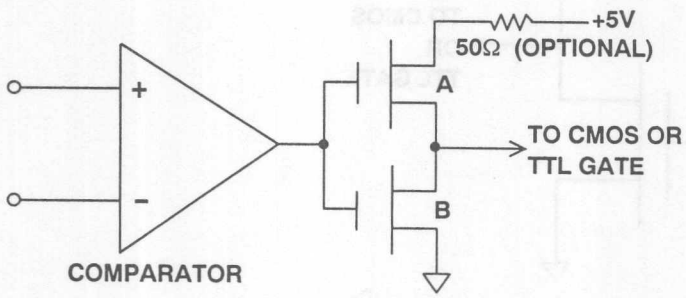
Figure 10.28

The simplest interface uses a single N-channel VMOS transistor and a pull-up resistor, R_L. A similar circuit may be made with an NPN transistor, R_L, and an additional transistor and diode. These circuits are simple, inexpensive and reliable, and may be connected with several transistors in parallel and a single R_L to give a "wired-or" function, but the speed of the 0-1 transition depends on the value of R_L and the stray capacity of the output node. The lower the value of R_L the faster, but the higher the power consumption.

By using two VMOS devices, one P-channel and one N-channel, it is possible to make a CMOS/TTL interface using only two components which has no quiescent power consumption in either state. Furthermore, it may be made inverting or non-inverting by simple positioning of components. It does, however, have a large current surge during switching, when both devices are on at once, and unless VMOS devices with high channel resistance are used a current limiting resistor may be necessary to reduce this effect. It is also important, in this application and the one in Figure 10.28, to use VMOS devices with gate-source breakdown voltages, V_{bgs}, greater than the output voltages of the comparator *in either direction*. A value of $V_{bgs} > \pm 25$ V is common in VMOS devices and is usually adequate, but some VMOS devices contain gate protection diodes which reduce the value - these should not be used.

Some op-amps have a terminal which may be used to clamp the output to within certain limits by connecting the terminal to reference voltages by diodes. Where such terminals exist they may be used to limit the op-amp output to values suitable for the logic being used but the circuitry is more complex than the simple interface circuitry given above and it is rarely worthwhile to do so.

LOW POWER INTERFACE WITH CMOS AND TTL GATES



- Can be inverting or non-inverting, depending on placing of VMOS devices.

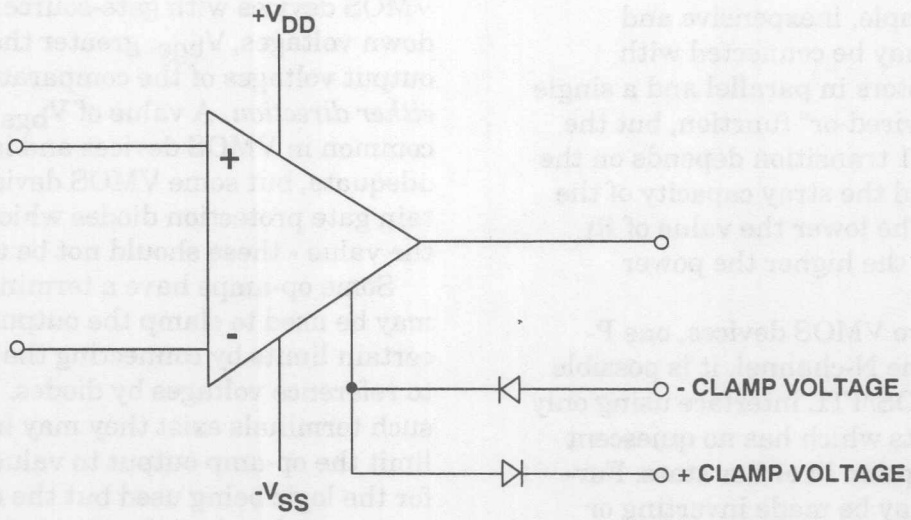
Inverting: A = P-channel/B = N-channel

Non-inverting: A = N-channel/B = P-channel

(V_{bgs} >±25 V for both devices)

Figure 10.29

OP AMPS WITH CLAMP CIRCUITRY MAY USE THIS TO LIMIT OUTPUT LEVELS TO LOGIC LEVELS



- But the circuitry shown in previous diagrams may be easier to use

Figure 10.30

INPUT CIRCUITRY

There are a number of effects which must be considered regarding the inputs of op-amps used as comparators. The first-level assumption engineers make about all op-amps and comparators is that they have infinite input impedance and can be regarded as open circuits - this is a reasonable starting position (except for current feedback (transimpedance) op-amps, which have a high impedance on their non-inverting input but a low impedance of a few tens of Ω on their inverting input, which is internally buffered to the same potential as the inverting input) but it must not be held indefinitely.

If an op-amp has a simple long-tailed pair as its input structure (whether using bipolar transistors or FETs) then its input impedance will remain high if a large differential voltage is applied to it. But many op-amps (especially bias-compensated ones such as the OP-07 and its many descendants) contain protective circuitry to prevent large voltages damaging input devices.

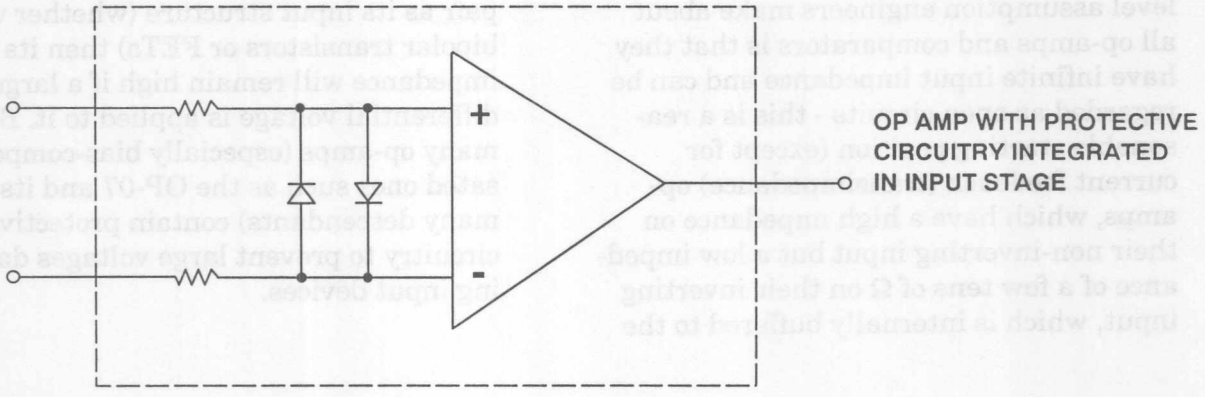
OP-AMP INPUT IMPEDANCE

10

- **INPUT IMPEDANCE IS NOT INFINITE (ESPECIALLY WHEN LARGE DIFFERENTIAL VOLTAGE IS APPLIED)**

Figure 10.31

MANY OP-AMPS HAVE CIRCUITRY TO PROTECT THEIR INPUT DEVICES



- This greatly reduces their input impedance when differential input voltages of more than ±700 mV are present

Figure 10.32

Others contain more complex input circuitry, which only has high impedance when the differential voltage applied to it is less than a few tens of mV, or which may actually be damaged by differential voltages of more than a few volts. It is therefore necessary, when using an op-amp as a comparator, to study the data sheet to determine how the input circuitry behaves when large differential voltages are applied to it. (It is always necessary to study the data sheet when using an integrated circuit to ensure that its non-ideal behavior (and every integrated circuit ever made has some non-ideal behavior) is compatible with the proposed application - it is just more important than usual in the present case.)

Of course some comparator applications never involve large differential voltages - or if they do the comparator input impedance when large differential voltages are present is comparatively unimportant. In such cases it may be appropriate to use as a comparator an op-amp whose input circuitry behaves non-linearly - but the issues involved must be considered, not just ignored.

As mentioned elsewhere in this seminar, nearly all BIFET op-amps exhibit anomalous behavior when their inputs are close to one of their supplies (usually the negative supply). Their inverting and non-inverting inputs may become interchanged. If this should occur when the op-amp is being used as a comparator the phase of the system involved will be inverted, which could well be inconvenient. The solution is, again, careful reading of the data sheet to determine just what common-mode range is acceptable.

READ THE DATA SHEET

- DETERMINE IF NON-LINEARITIES IN YOUR OP-AMP'S INPUT WILL AFFECT ITS OPERATION AS A COMPARATOR
- LOOK FOR:-

  Low values of Absolute Max Differential Input Voltage

  Graphs of Bias Current or Input Current vs Differential or Common-Mode Input Voltage

  Any other input specification which may indicate non-linearities

- WILL YOUR PROPOSED APPLICATION WORK WITH A COMPARATOR WHICH BEHAVES IN THIS WAY??

Figure 10.33

PHASE INVERSION

- BIFET AMPLIFIERS OFTEN SUFFER PHASE-INVERSION WHEN THEIR COMMON-MODE VOLTAGE IS CLOSE TO THEIR SUPPLIES
- Verify your common-mode range when using BIFET op-amps.

Figure 10.34

HYSTERESIS & STABILITY

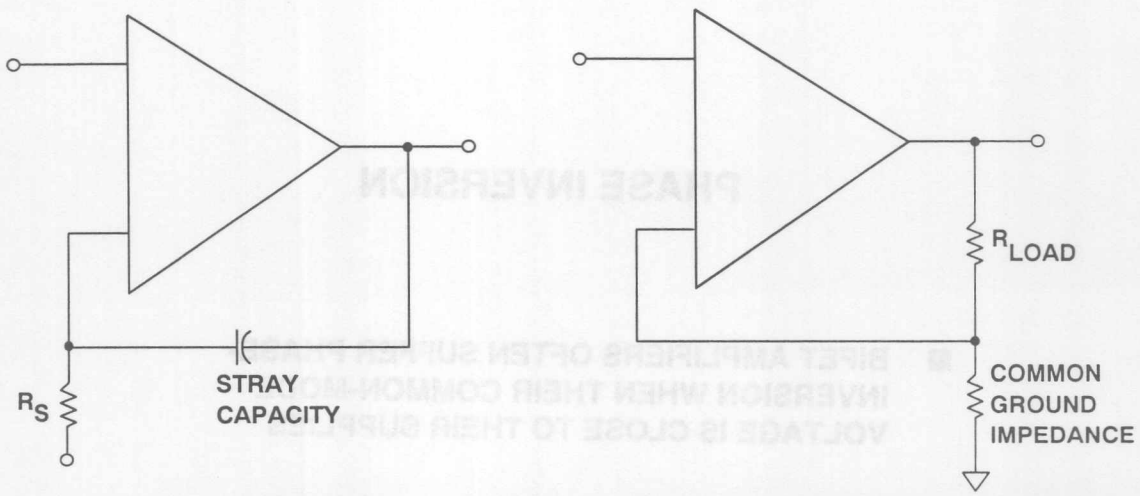
When an op-amp is functioning as a comparator there is no negative feedback present so, during transitions, its full open-loop gain is present and very small amounts of positive feedback can start oscillation.

This instability can result from capacitive feedback from the output to an input (usually the non-inverting input), or from coupling due to output currents flowing in ground impedances which are common to the input circuitry. The cure for the first is to minimize stray feedback capacity by proper layout, and to ensure that the impedance seen by the non-inverting input is as low as possible, ensuring that any remaining capacitively fed-back signal is attenuated to insignificance.

Ground current feedback is controlled by intelligent design of the ground circuit layout, as discussed in the relevant section of this Seminar.

Sometimes it is not possible to prevent instability by these measures. The only remaining possibility is to use positive feedback to introduce a small amount of hysteresis so that once a transition has started the input must undergo significant reversal before the reverse transition can occur.

OPEN-LOOP OP-AMPS USED AS COMPARATORS MAY SUFFER INSTABILITY OR LATCH-UP DUE TO FEEDBACK FROM STRAY CAPACITY OR COMMON GROUND IMPEDANCES.



- **The Problem may be eased by minimizing stray capacitance, source impedances, and common ground impedances.**

Figure 10.35

HYSTERESIS

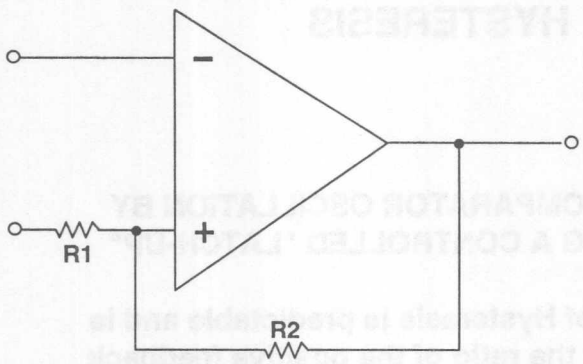
- **CAN CURE COMPARATOR OSCILLATION BY INTRODUCING A CONTROLLED "LATCH-UP"**
- **The amount of Hysteresis is predictable and is controlled by the ratio of the positive feedback resistors.**

Figure 10.36

This can be done with two resistors, and the amount of hysteresis is proportional to their ratio. The signal input to the comparator may be applied to either the inverting or the non-inverting input, but if it is applied to the inverting input its source impedance must be low enough to have insignificant effect on R1 (of course if the source impedance is sufficiently predictable it may be used as R1).

If the reference voltage is midway between the two comparator output voltages (as is the case with a symmetrical power supply and a ground reference) then the introduction of hysteresis will move the positive and negative thresholds equal distances from the reference, but if the reference is nearer to one output than to the other the thresholds will be asymmetrically placed about the reference voltage.

POSITIVE FEEDBACK ADDS HYSTERESIS TO A COMPARATOR



OUTPUT SWING: V_S

HYSTERESIS = $\frac{V_S (R1+R2)}{R1}$

- Input signal may be applied to either input but its source impedance must be low if it is applied to R1

Figure 10.37

CALCULATION OF THRESHOLDS WHEN THE REFERENCE IS NOT MIDWAY BETWEEN THE OUTPUTS

- Comparator output voltages are V_p & V_n
- Reference voltage is V_r
- Negative threshold is $\frac{(R1 + R2)V_r - R1V_p}{R2}$
- Positive threshold is $\frac{(R1 + R2)V_r - R1V_n}{R2}$

Figure 10.38

CONCLUSION

Operational amplifiers are not designed to be used as comparators, so this section has been, intentionally, a little discouraging. Nevertheless there are many applications where the use of an op-amp as a comparator is a correct engineering decision - what is important is to make it a *considered* decision, and ensure that the op-amp chosen will perform as expected. To do this it is necessary to read the data sheet carefully, to consider the effects of non-ideal op-amp performance, and to calculate the effects of op-amp parameters on the application. Since the op-amp is being used in a non-standard manner some experiment may also be necessary - since the amplifier used for the experiment will not necessarily be typical the results of experiments should always be interpreted somewhat pessimistically.

CONCLUSION

- **OP-AMPS MAY BE USED AS COMPARATORS BUT BE CAREFUL!**
- **Read the Data Sheet**
- **Calculate the effects of non-ideal parameters**
- **Experiment**
- **Always interpret your results a little pessimistically**

10

Figure 10.39

SECTION XI
OP AMP SUBTLETIES

- Op Amp Output Voltage Phase Reversal:
- Does Op Amp Open Loop Gain Non-Linearity Effect Accuracy?
- High Speed Op Amp Settling Time Measurements
- Op Amp Noise and How to Avoid it:
  Internal Circuit Noise, Circuit Noise from Components, External Noise, Photoelectric Effects, Noise from Switching Supplies, Noise Reduction, Measuring External Noise
- The IC Op Amp User's Guide to Grounding, Decoupling, and Making Things Go Right for a Change

SECTION XI

OP AMP SUBTLETIES

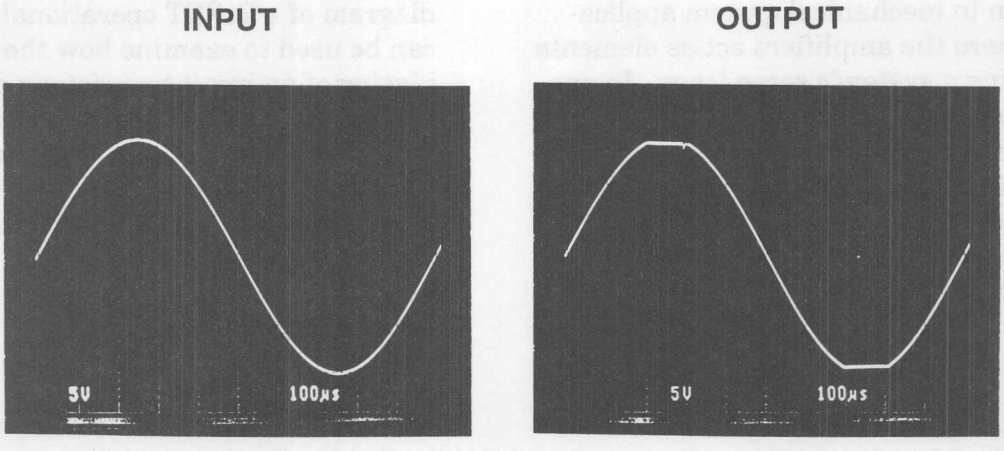
ADOLFO GARCIA, JAMES WONG, WALT KESTER, CHRIS HYDE, JAMES BRYANT, PAUL BROKAW

OPERATIONAL AMPLIFIER OUTPUT VOLTAGE PHASE REVERSAL

ADOLFO A. GARCIA

In vibration translation, process control, instrumentation, and servo system applications where sensitive sensors are used for recording and monitoring, oftentimes signals from these sensors can exceed an amplifier's common-mode voltage range during a fault condition or a power-up sequence. In the most extreme cases, fault conditions may generate input signals greater than the amplifier's supply voltages. Although not protected in the latter case, many, if not most all, operational amplifiers have protection built into them to safeguard the device from permanent damage should large differential signals appear at the device's input terminals. In many cases where input signals do exceed an amplifier's common-mode range, the amplifier behaves as a clipping circuit. Shown in Figure 11.1 is an example of the industry-standard OP-07 operational amplifier in a voltage follower configuration where the input voltage has exceeded the amplifier's common-mode range. Note how the amplifier clips the input signal without damage to the amplifier or the load.

BEHAVIOR OF OP-07 WHEN INPUT IS DRIVEN BEYOND LINEAR COMMON MODE RANGE



VERTICAL SCALE: 5V / div.
HORIZONTAL SCALE: 100µs / div.

Figure 11.1

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However, not all operational amplifiers behave as clipping circuits. Because of varied designs used in the input and gain stages, some operational amplifiers behave unusually when the input signal voltages exceed the amplifier's input common-mode range. For example, high input impedance amplifiers, such as the OP-42 and the AD711, use ion-implanted, p-channel JFETs in the input stage to reduce the bias currents to the picoamp range and, at the same time, to raise the input impedance levels above 10^9 Ω. As shown in Figure 11.2, the output of these amplifiers exhibit an output voltage phase inversion when the input signal exceeds the amplifier's linear, negative common-mode range.

Note that the output is suddenly driven to the positive output voltage limit and remains there until the input signal level returns within the common-mode range of the amplifier. This occurs most often with BiFET operational amplifiers configured as voltage followers in dual supply applications. Operational amplifiers designed for single supply applications also suffer from this malady and will be discussed elsewhere.

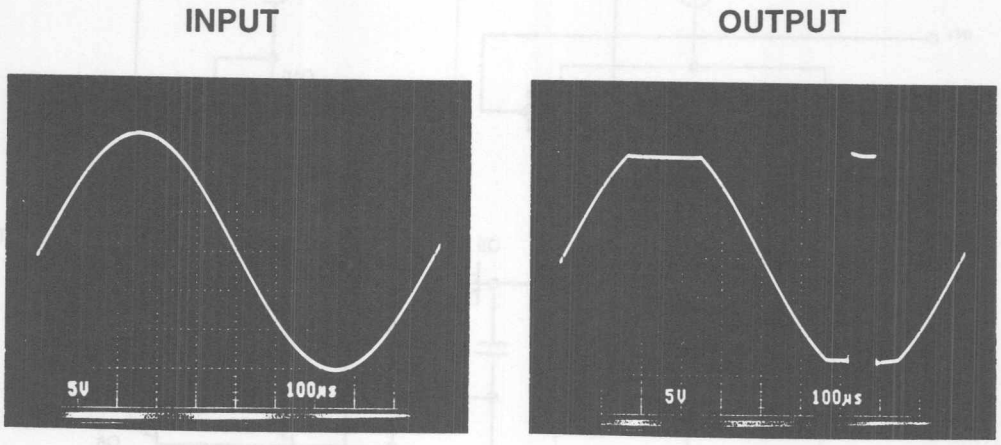
This effect in BiFET operational amplifiers can cause a very dangerous lock-up condition in mechanical system applications where the amplifiers act as elements controlling a system's servo loops. In one particular application, a customer who used BiFET amplifiers in the servo loops of a shaker table controller noted that he could consistently *launch* 100 lb. objects across his lab every time he induced a failure mode in his system. In one way, he was quite pleased that he had stumbled upon a new catapult system and wondered aloud if there would be a military application for it . On the other hand and not surprisingly, he was quite alarmed by the effect. Situations where a system failure could drive the input of the amplifier beyond its common-mode range occurs in roughly 2 to 3 % of all applications that use BiFET amplifiers. It is still important to understand what is happening and prevent the effect from occurring.

Shown in Figure 11.3 is the vertical cross section of an ion-implanted, p-channel JFET which is a good starting point for understanding the cause of amplifier output phase reversal.

In the equivalent circuit shown in Figure 11.3b, there are two parasistic pnp transistors directly under the source and drain diffusions. These parasitic devices typically exhibit very low current gains and contribute very little excess current flow during phase reversal. However, if the input exceeds the negative supply voltage (a condition that must always be avoided), these devices energize and can lead to destruction of the amplifier due to excessive current flow and power dissipation in the die.

At this point, a simplified schematic diagram of a BiFET operational amplifier can be used to examine how the forward-biasing of an input transistor's drain-gate diode leads to the phase reversal effect. Shown in Figure 11.4 is a schematic of one such BiFET amplifier, the OP-42. Note that a highlighted path illustrates the devices involved.

OP-42 OUTPUT PHASE REVERSAL WHEN INPUT DRIVEN WELL BEYOND LINEAR NEGATIVE COMMON MODE RANGE



VERTICAL SCALE: 5V / div.
HORIZONTAL SCALE: 100µs / div.

Figure 11.2

VERTICAL CROSS SECTION AND EQUIVALENT CIRCUIT FOR ION-IMPLANTED, P-CHANNEL JFET

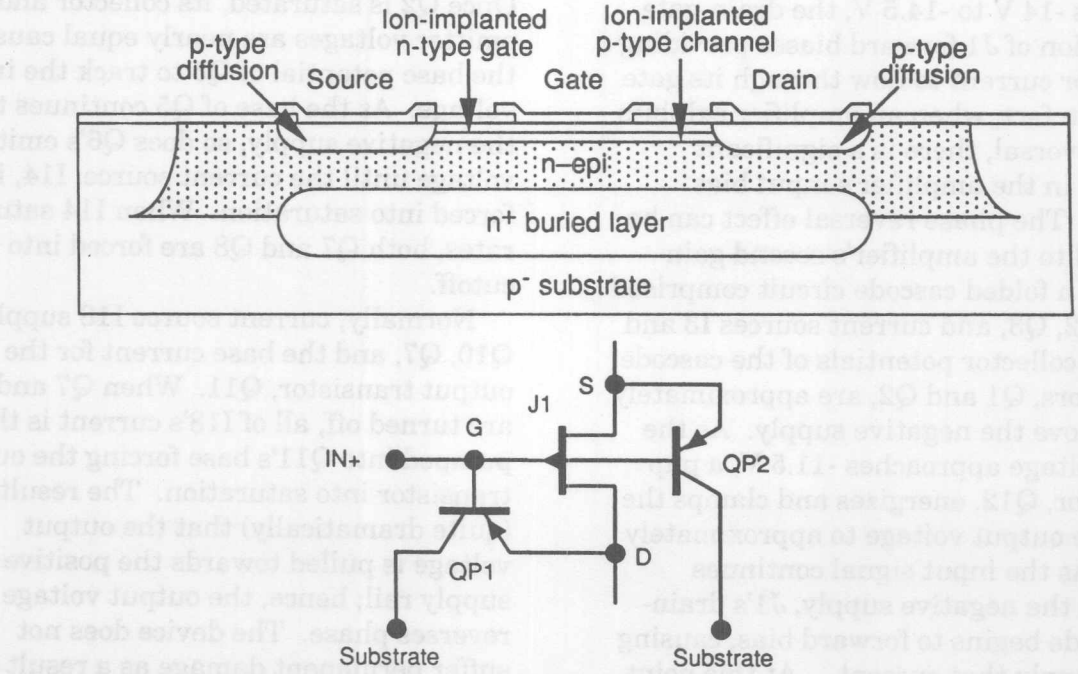


Figure 11.3

OP-42 SIMPLIFIED SCHEMATIC SHOWING DEVICES INVOLVED DURING OUTPUT PHASE REVERSAL

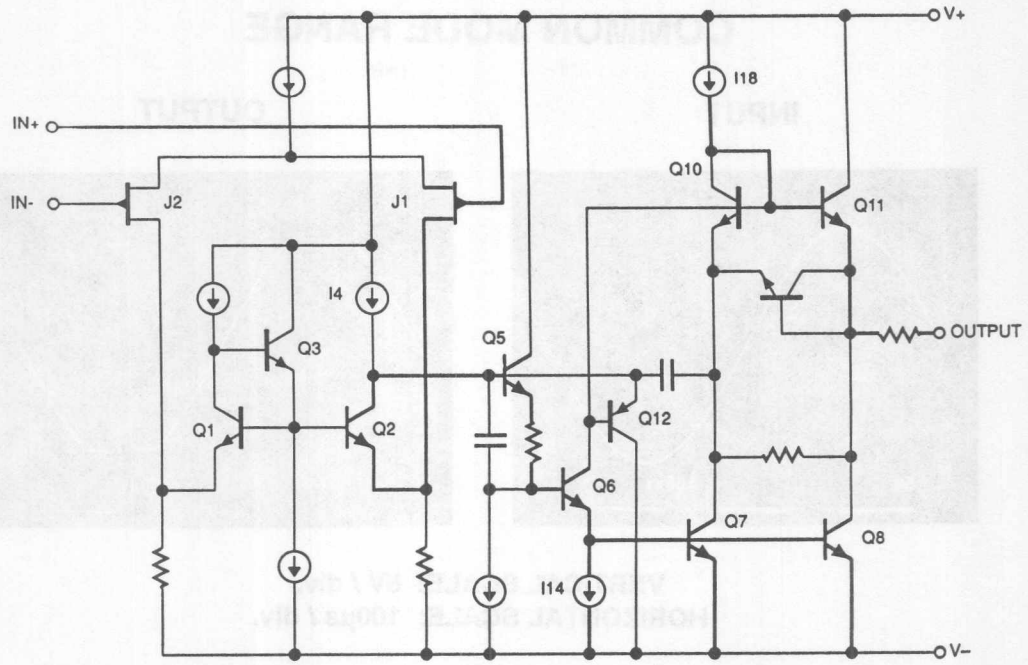


Figure 11.4

Under normal operating conditions in the OP-42, the drain voltages of J1 and J2 are typically 1 V above the negative supply rail. As the input voltage approaches -14 V to -14.5 V, the drain-gate pn junction of J1 forward biases providing a path for current to flow through its gate metal. In fact, when an amplifier exhibits phase reversal, there is a significant increase in the amplifier's input bias current. The phase reversal effect can be localized to the amplifier's second gain stage — a folded cascode circuit comprised of Q1, Q2, Q3, and current sources I3 and I4. The collector potentials of the cascode transistors, Q1 and Q2, are approximately 3.5 V above the negative supply. As the input voltage approaches -11.5 V, a pnp transistor, Q12, energizes and clamps the negative output voltage to approximately -12 V. As the input signal continues towards the negative supply, J1's drain-gate diode begins to forward bias, causing Q2 to supply that current. At this point, Q2's emitter ceases to control J1's drain voltage and begins to track the input voltage. Q2 continues to supply current for J1's forward-biased drain-gate diode until Q2 is forced into saturation because of the limited current available from I4. Once Q2 is saturated, its collector and emitter voltages are nearly equal causing the base potential of Q5 to track the input voltage. As the base of Q5 continues to the negative supply, so does Q6's emitter voltage until the current source, I14, is forced into saturation. When I14 saturates, both Q7 and Q8 are forced into cutoff.

Normally, current source I18 supplies Q10, Q7, and the base current for the output transistor, Q11. When Q7 and Q8 are turned off, all of I18's current is then pumped into Q11's base forcing the output transistor into saturation. The result is (quite dramatically) that the output voltage is pulled towards the positive supply rail; hence, the output voltage reverses phase. The device does not suffer permanent damage as a result of phase reversal provided the input is never allowed to exceed the negative supply rail.

THE FIX

Since the effect is caused by the saturation of Q2 due to the forward-biasing of J1's drain-gate pn junction, the solution to the phase reversal effect is preventing Q2 from being driven into saturation. Placing a resistor in series with the gate of J1 (the non-inverting terminal of the amplifier), as shown in Figure 11.5, limits the current flow through Q2. As illustrated in Figure 11.6, a 7.5 kΩ resistor effectively prevents the OP-42's output voltage from phase reversal over the full MIL-temperature range.

For other BiFET amplifiers, Figure 11.7 summarizes the series resistor values required to suppress output voltage phase reversal. Also shown for comparison in the table are the equivalent input voltage noise spectral densities of the amplifiers alone and with the an external series resistor. In using this technique, the increase in overall system noise and the new pole created with the stray input capacitance must be evaluated.

ELIMINATING OUTPUT VOLTAGE PHASE REVERSAL IN THE OP-42

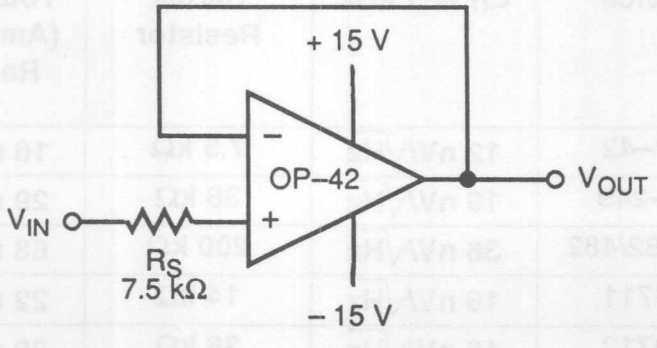
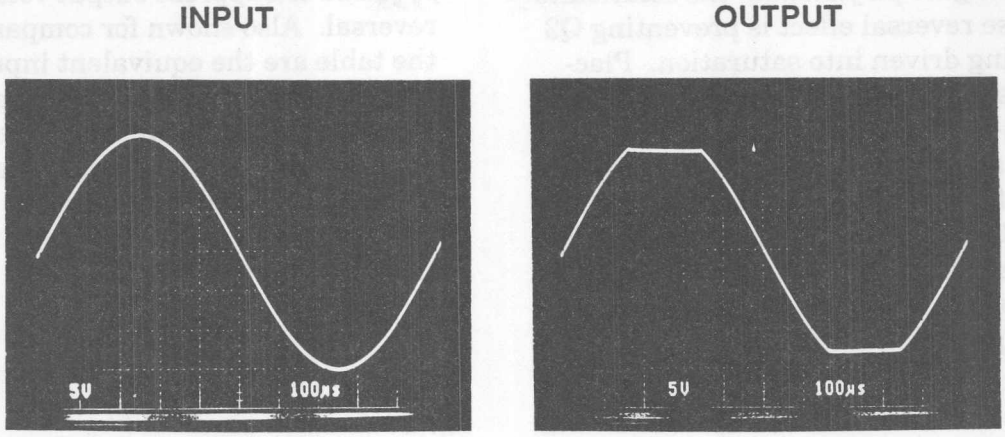


Figure 11.5

EFFECTIVENESS OF SERIES RESISTOR IN ELIMINATING PHASE REVERSAL IN THE OP-42



VERTICAL SCALE: 5V / div.
HORIZONTAL SCALE: 100µs / div.

Figure 11.6

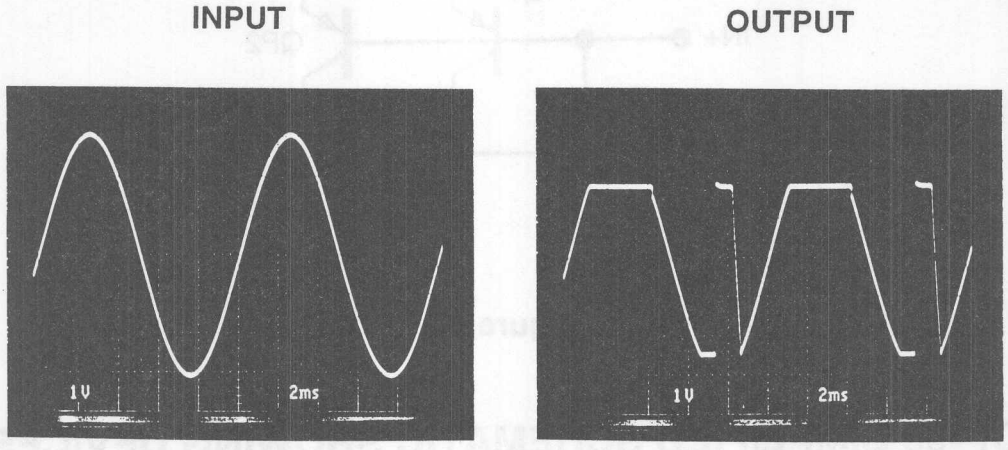
SERIES RESISTANCE VALUES FOR BIFET AMPLIFIERS TO PREVENT PHASE REVERSAL

Device	E_n @ 1 kHz	Series Resistor	Total Noise (Amplifier + Resistor)
OP–42	12 nV/$\sqrt{Hz}$	7.5 kΩ	16 nV/$\sqrt{Hz}$
OP-249	16 nV/$\sqrt{Hz}$	36 kΩ	29 nV/$\sqrt{Hz}$
OP-282/482	36 nV/$\sqrt{Hz}$	200 kΩ	68 nV/$\sqrt{Hz}$
AD711	16 nV/$\sqrt{Hz}$	14 kΩ	22 nV/$\sqrt{Hz}$
AD712	16 nV/$\sqrt{Hz}$	36 kΩ	29 nV/$\sqrt{Hz}$

Figure 11.7

As previously mentioned, BiFET amplifiers are not the only devices susceptible to output phase reversal. The effect also manifests itself in operational amplifiers designed for single-supply operation. In these cases, these amplifiers exhibit a phase reversal when the input signal drops below the negative supply rail. For example, Figure 11.8 illustrates an OP-90 configured as a voltage follower that uses a single + 5V supply. When the input exceeds the negative supply – in this case, ground – by about 0.6V, the OP-90's output voltage goes into phase reversal.

PHASE REVERSAL IN THE OP-90 SINGLE SUPPLY OP AMP



VERTICAL SCALE: 1V / div.
HORIZONTAL SCALE: 2ms / div.

Figure 11.8

In order for the input common-mode range to include the negative supply in these amplifiers, the input stages use pnp transistors, usually lateral devices. The input stages are intentionally designed to have slightly forward-biased collector-base junctions when the inputs are at zero volts. These junctions could have as much as 80 mV to 120 mV of forward bias across the collector-base junction. There are other active devices to consider in addition to the input transistors under this condition. Consider the vertical cross section of a typical lateral pnp transistors Figure 11.9, there are two parasitic vertical pnp transistors to the substrate: one under the collector diffusion and one under the emitter diffusion.

VERTICAL CROSS SECTION AND EQUIVALENT CIRCUIT FOR LATERAL PNP TRANSISTOR

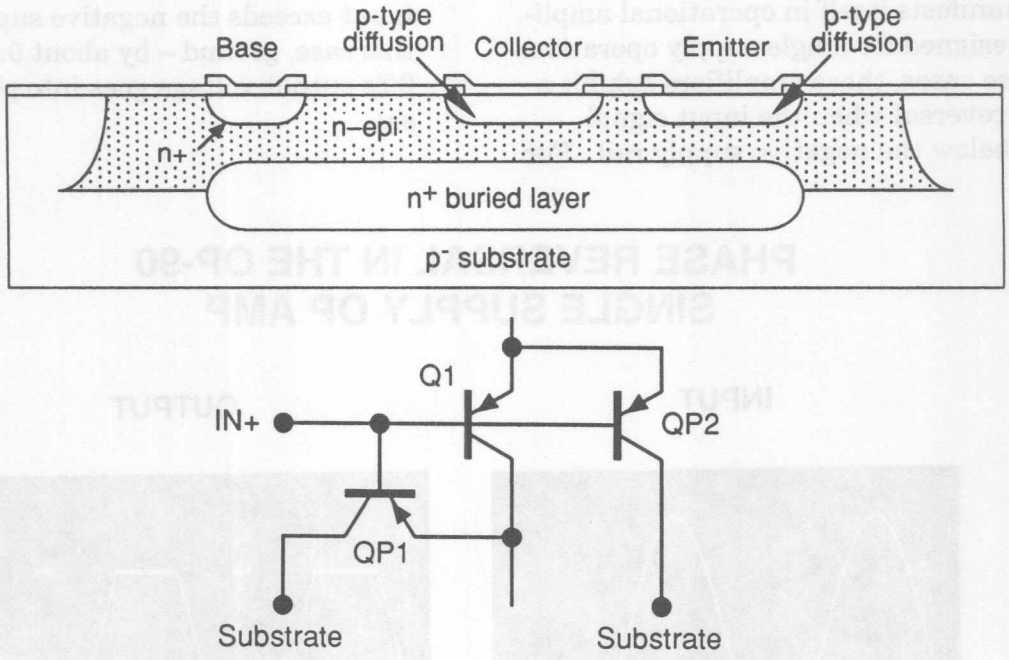


Figure 11.9

OP-90 SIMPLIFIED SCHEMATIC SHOWING DEVICES INVOLVED DURING OUTPUT PHASE REVERSAL

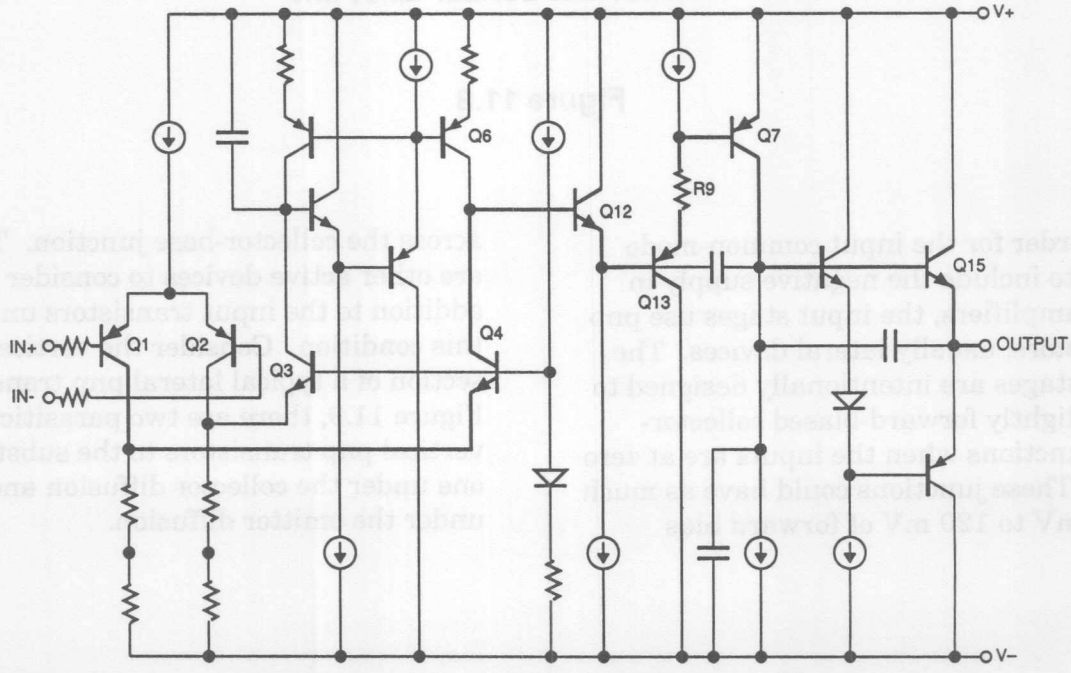


Figure 11.10

Since the collector junction of Q1 is biased slightly above the negative supply, the base-emitter junction of QP1 also begins to conduct current. As the input of the amplifier goes below ground by approximately 0.6 V, both QP1 and QP2 are forced into saturation. Even though three pn junctions are turned on, any increase in input bias current during phase reversal is slight because the highly resistive epitaxial layer limits current flow through the base junctions.

Using the same approach as for the BiFET amplifiers, a simplified schematic of the OP-90 can be used to discover the cause of phase reversal in single-supply amplifiers. Its simplified schematic is shown in Figure 11.10. The devices involved in phase reversal are highlighted.

When Q1's input drops below the negative supply, its collector junction tracks the input causing a transistor, Q4, in the folded cascode gain stage to saturate because of the limited amount of current in the stage provided by Q6. With Q4 in saturation, the base voltage of the complementary darlington pair, Q12 and Q13, also tracks the input voltage. This causes a larger voltage drop across R9 and, in turn, causes larger base currents to flow in Q7. In the design of the OP-90, Q7 is a large lateral pnp transistor whose function is to provide the base drive for the output drive transistor, Q15. As Q7's collector current increases in the absence of a load at the output of the amplifier, Q15 is driven into saturation. The output voltage is then pulled up to the amplifier's positive output voltage limit.

THE FIX FOR THE OP-90

Since there is no marked increase in the input bias current of the OP-90 at the point of phase reversal, the best method for preventing this effect is to clamp the input voltage to ground using a schottky diode, as shown in Figure 11.11. This technique is best used when the amplifier is configured as a voltage follower. Figure 11.12, shows that this technique is quite effective in preventing output phase reversal.

A schottky diode typically exhibits a turn-on voltage of 0.3 V to 0.4 V which is below the voltage required to forward bias Q1's collector-base junction. A 1 kΩ resistor in series with the input of the OP-90 is optional; however, using it is a good idea because it serves to limit the current flow in the schottky diode should the input voltage become significantly larger than the forward voltage drop of the schottky diode. In single-supply + 12 V or + 15 V applications, be mindful of schottky diodes' low breakdown voltages and comparatively high reverse leakage. Large reverse-bias leakage currents may flow through the diode and might appear as input bias current errors in the amplifier circuit.

ELIMINATING OUTPUT PHASE REVERSAL IN THE OP-90

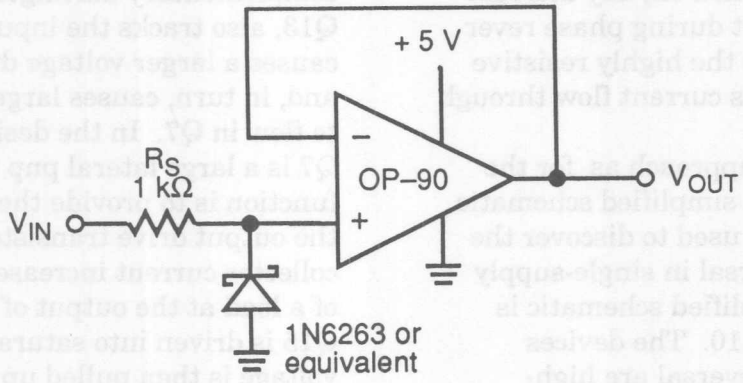
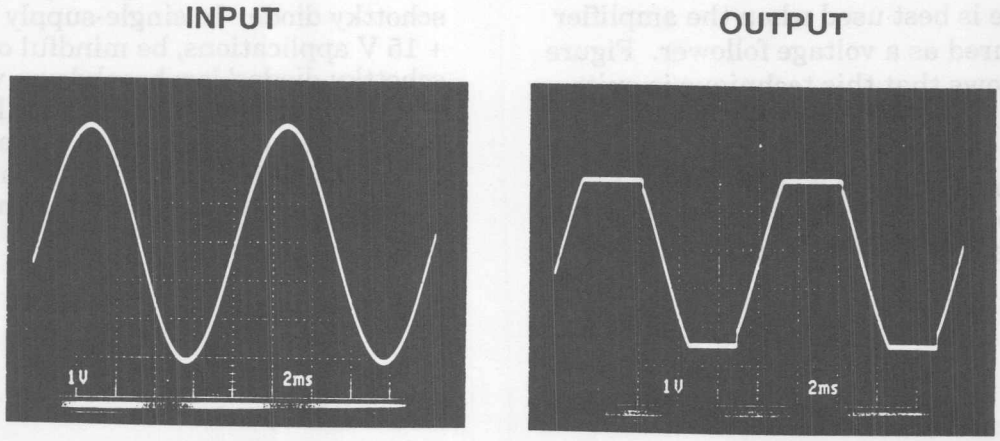


Figure 11.11

EFFECTIVENESS OF SCHOTTKY DIODE IN PREVENTING PHASE REVERSAL IN SINGLE-SUPPLY OP-90



VERTICAL SCALE: 1V / div.
HORIZONTAL SCALE: 2ms / div.

Figure 11.12

DOES OP AMP OPEN-LOOP GAIN NON-LINEARITY EFFECT ACCURACY?

JAMES WONG

This question has a two-part answer. In the case of a high gain circuit, the answer is YES, and gain nonlinearity can be a significant source of error. On the other hand, its nonlinear effect is much diminished at lower gains. Unlike input offset voltage and common-mode errors which are generally specified and can be measured at a fixed input voltage or an input voltage range, open-loop gain nonlinearity is a subtle error produced by output swings. Generally this error source is neither specified nor quantified. Yet it may be a real part of an op amp's error source. If present, it degrades the accuracy of a circuit without being noticed.

WHAT IS OPEN-LOOP GAIN NONLINEARITY?

Nonlinearity exists if an op amp experiences a change in its open-loop gain as the output swings through its linear voltage range. Because gain is the ratio of output to input, any nonlinearity is referred to the input and shows up as a change in input offset. Thus in an amplifier circuit, this translates to a deviation of the output voltage from the expected output because of the offset change. This occurs even though the input common-mode voltage remains relatively constant. Clearly, this can have appreciable effect on the accuracy of an amplifier. The error is especially pronounced if the amplifier is operating at high closed-loop gains.

To be sure, this input offset error change is indistinguishable from any input offset voltage change due to other factors such as self-heating, or bias shifts. Nonetheless, in an actual application, the error is real and directly affects the output accuracy of an amplifier.

Figure 11.13 shows a useful test circuit that can be used to measure the gain linearity behavior of an op amp. The nonlinear behavior can take many different shapes such as bowing, double bowing, or S-curved. Every device type is different.

The linear ramp input causes the output to swing through a +/-10V range. This voltage is measured against the pseudo summing node V_Y which represents the input voltage of the op amp magnified by a gain-factor (that is determined by $R_G/10\ \Omega$). The open-loop gain is the inverse of the slope of the curve, dV_X / dV_Y, multiplied by the gain-factor. If the open-loop gain is linear, V_Y will be linearly proportional to V_X. Thus a straight line will be plotted. Otherwise a nonlinear line will be drawn. An offset adjustment may be necessary to center the curve on the plotter.

Component values shown in the figure are for use with open loop gains from 1 million to 10 million. The value of R_G may be reduced for gains less than 1 million to increase measurement resolution.

Figure 11.14 shows an example of the measured behavior of an industry-standard precision op amp. Of course, every op amp has its own unique characteristic. One should measure this parameter to assure the right op amp is chosen for the application.

OPEN-LOOP GAIN NON-LINEARITY TEST CIRCUIT

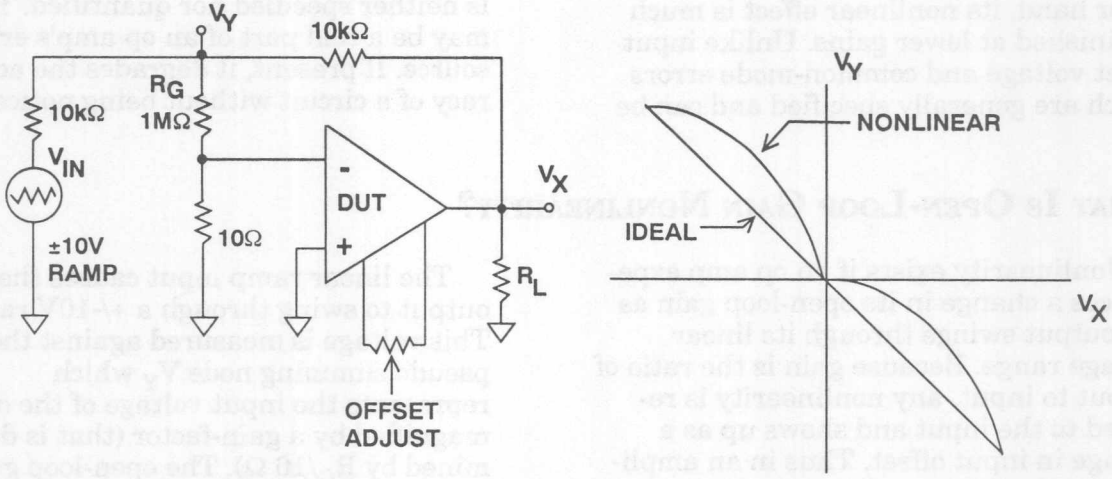


Figure 11.13

MEASURED OPEN-LOOP GAIN BEHAVIOR AS A FUNCTION OF OUTPUT VOLTAGE

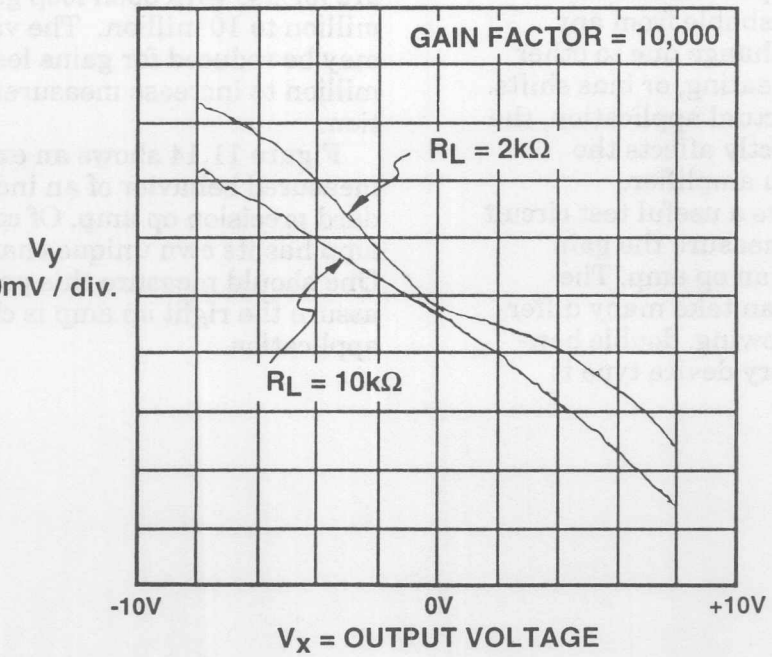


Figure 11.14

WHAT CAUSES GAIN NONLINEARITY ?

The severity of the nonlinearity varies widely from device type to device type, and may be dependent on the load it is driving. Although many precision op amps do exhibit some amount of nonlinearity, it is important for the designer to know up-front whether they have high enough open-loop gain to minimize its impact on accuracy. Only a few exhibit no error at all. These are the most desirable and produce the best accuracy.

Gain nonlinearity can come from many sources, depending on the design and layout of the chip. One possible source is thermal feedback. As the output swings, the amount of output current also changes, causing the power dissipation of the output device to change. Should the resulting temperature shift cause the gain stage to drift, a nonlinear gain will result. Similarly, if this temperature shift migrates to the input stage's differential pair in an unbalanced way, an additional offset error will result, which produces an apparent gain shift.

If temperature shift is the sole cause of the nonlinearity error, it can be postulated that minimizing the output loading will help. To verify this, measure the linearity behavior under a light load (>10 kΩ) and compare with the case of a heavy load (<2 kΩ). If nonlinearity is detected with the heavy load and not with the light load, then the solution is to reduce the loading. An example of this is the OP-97 low-power precision op amp, whose open-loop gain curves under different loads are shown in Figure 11.15 below.

GAIN NONLINEARITY INCREASES AS LOAD RESISTANCE DECREASES, SHOWN FOR OP-97 PRECISION OP AMP

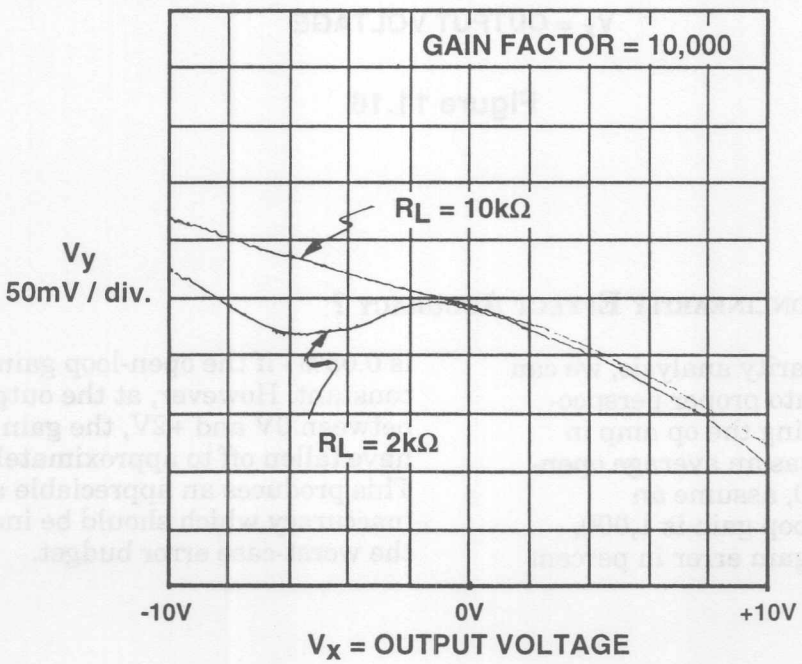


Figure 11.15

With this knowledge, one should operate the OP-97 with no less than 10 kΩ load, which in most applications is not a problem. However, not all op amps' gain nonlinearity can be cured this way, as some are inherently nonlinear regardless of load. For these devices, there must be other second-order effects inherent of the design that cause the nonlinear behavior. For example, a sample of the LT1077 op amp exhibited rather poor linearity as evidenced in the measured behavior in Figure 11.16. Reducing the load did not help eliminate the problem.

SOME OP AMPS EXHIBIT POOR GAIN LINEARITY REGARDLESS OF LOAD CONDITIONS

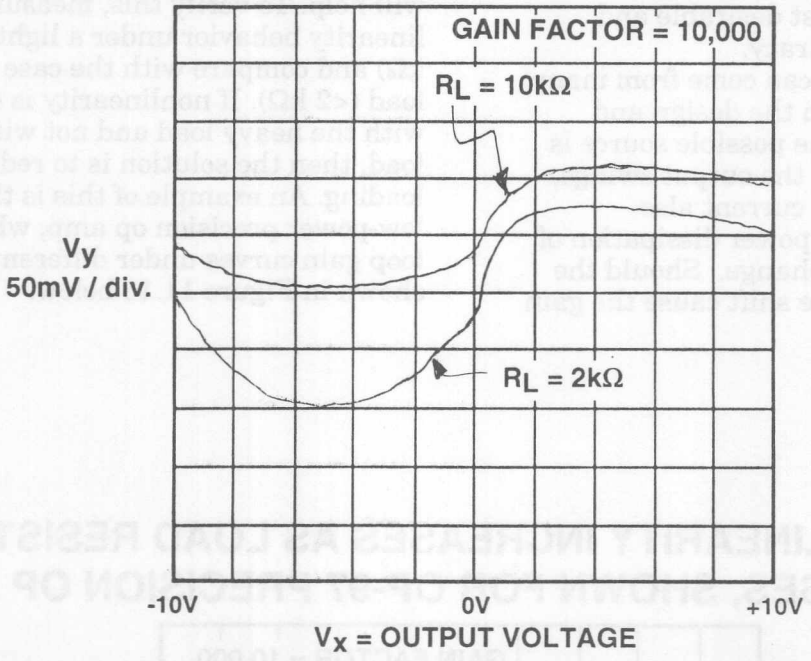


Figure 11.16

HOW DOES GAIN-NONLINEARITY EFFECT ACCURACY ?

From this nonlinearity analysis, we can put this error term into proper perspective. For example, using the op amp in Figure 11.16 which has an average open-loop gain of 2,000,000, assume an application's closed-loop gain is 1,000, then the closed-loop gain error in percent is 0.05% - if the open-loop gain remains constant. However, at the output voltage between 0V and +2V, the gain appears to have fallen off to approximately 300,000. This produces an appreciable amount of inaccuracy which should be included in the worst-case error budget.

GAIN NONLINEARITY EFFECT ON GAIN ERROR

- Assumptions: $A_{VOL} = 2{,}000{,}000$

  $A_{VCL} = 1{,}000$

- Gain Error (closed-loop) $= \frac{A_{VCL}}{A_{VOL}} = \frac{1000}{2000000} \times 100\%$

  $= 0.05\ \%$

- If A_{VOL} Drops To 300,000 Due To Gain Nonlinearity,

- Gain Error (closed-loop) $= \frac{1000}{300000} \times 100\%$

  $= 0.33\%$

Figure 11.17

From this analysis, clearly gain nonlinearity cannot be ignored if absolute precision is to be attained. There are two ways to solve the problem from a system designer's perspective. One is to simply choose an op amp that does not exhibit this nonlinear behavior. Examples of a linear op amp are the OP-177 and the AD707, which are among the industry's highest precision op amps. Their open-loop gain linearities are shown in Figure 11.18 and Figure 11.19, respectively. The OP-177 open loop gain is approximately 8 million, while that of the AD707 is approximately 25 million.

The best way to minimize the nonlinear impact is to make sure the amplifier open loop gain is sufficiently high such that in spite of its presence, there is ample loop-gain to correct for any gain variations.

THE OP-177 IS DESIGNED FOR LINEAR GAIN TO INSURE PRECISION PERFORMANCE

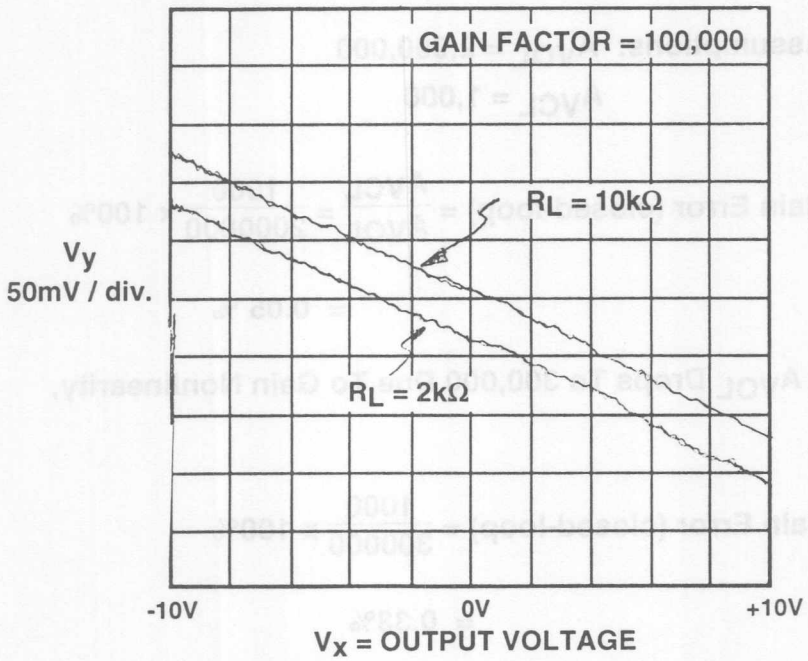


Figure 11.18

THE AD707 EXHIBITS LINEAR GAIN TO INSURE CIRCUIT ACCURACY

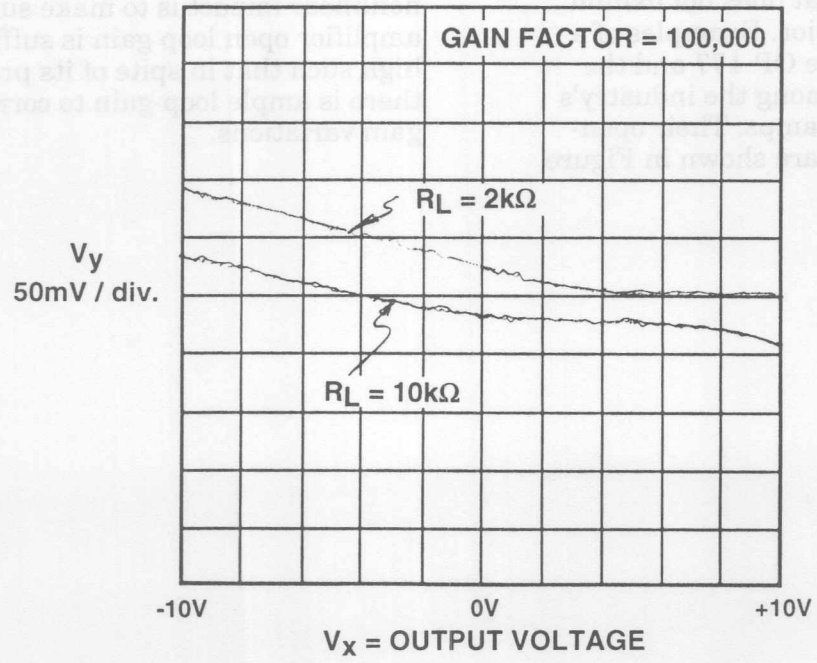


Figure 11.19

HIGH SPEED OP AMP SETTLING TIME MEASUREMENTS

WALT KESTER

Settling time of an op amp is defined as the interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band. This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing and (4) linear settling to within the error band.

The measurement of settling times of high speed amplifiers is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

Measuring settling times of inverting op amps may be accomplished by creating a false summing junction with a resistive divider connected between the amplifier output and the input as shown in Figure 11.20. Care should be taken to insure that the time constant at the false summing junction created by the scope capacitance is less than that of the amplifier being tested. The back-to-back diodes help prevent oscilloscope overdrive.

The circuit shown in Figure 11.21. may be used if extra gain is required between the summing junction and the scope. This circuit is useful for measuring settling times of over 80ns to 12-bit accuracy (0.01%). The diagram shows the test setup for the AD843 high speed FET input op amp which settles to 0.01% in less than 135ns. The settling time characteristics are shown in Figure 11.22.

MEASUREMENT OF INVERTING MODE SETTLING TIME USING A FALSE SUMMING JUNCTION

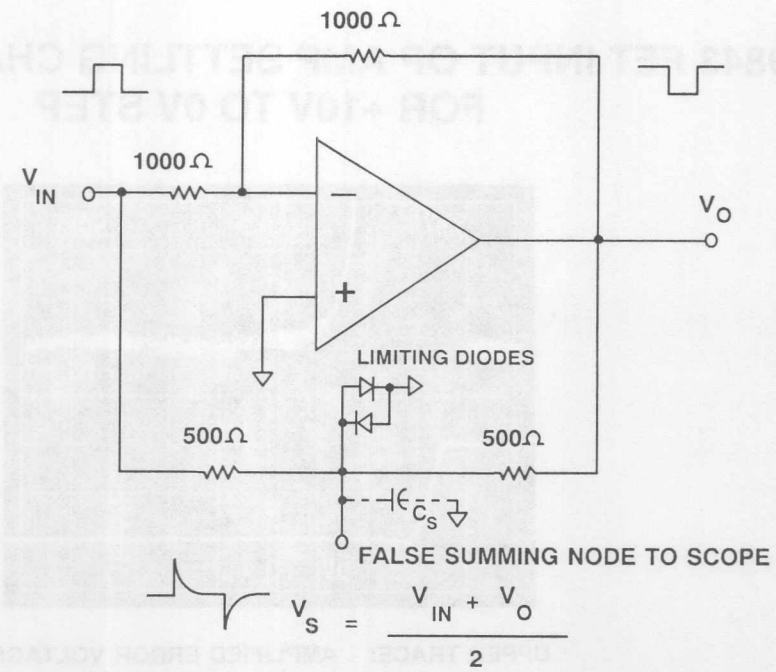


Figure 11.20

GREATER THAN 80ns SETTLING TIME CIRCUIT WITH SUMMING JUNCTION GAIN

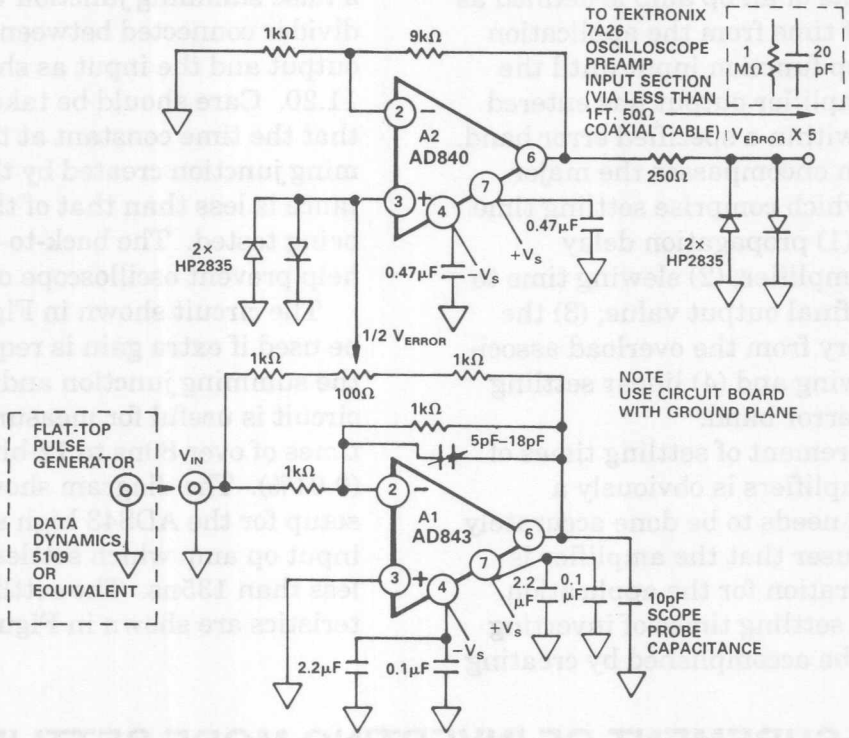
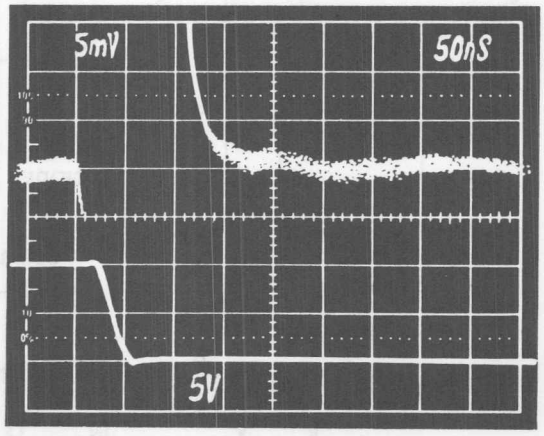


Figure 11.21

AD843 FET INPUT OP AMP SETTLING CHARACTERISTIC FOR +10V TO 0V STEP



UPPER TRACE: AMPLIFIED ERROR VOLTAGE (0.01%/DIV)

LOWER TRACE: OUTPUT OF AD843 (5V/DIV)

Figure 11.22

The false summing junction technique described above will not work with a non-inverting amplifier for obvious reasons. Most oscilloscopes will not allow direct observation of the output waveforms true settling time because they will be severely overdriven when operating at the required resolution. The technique shown in Figure 11.23 uses a diode network on the amplifier output to limit the swing of the 5V output step to 0.75V. This step can be observed directly by the scope with approximately 25mV/division vertical sensitivity without overdriving the scope input. Actual measurements on an amplifier are shown in Figure 11.24. The Schottky diode network on the input of the amplifier is used to generate a flat pulse. This network must be placed less than 0.5 inches from the amplifier input in order to minimize parasitic effects.

When making settling time measurements to 0.02% to less than 15ns, especially in the non-inverting mode, there are problems with all of the above techniques. At these speeds, it is best to use a high-speed sampling plug-in, such as the Data Precision Model 640 (using Data Precision 6100 Waveform Digitizer). This plug-in uses a 16-bit successive approximation ADC with the comparator actually an integral part of the probe tip. Using this architecture, the scope input is not sensitive to overdrive, and the settling time measurement can be made directly as shown in Figure 11.25. for the AD9620 unity-gain buffer. The output pulse is 2V, and the vertical resolution of the digitized output is 0.4mV, or 0.02%/division.

SETTLING TIME TEST CIRCUIT LIMITS OSCILLOSCOPE OVERDRIVE

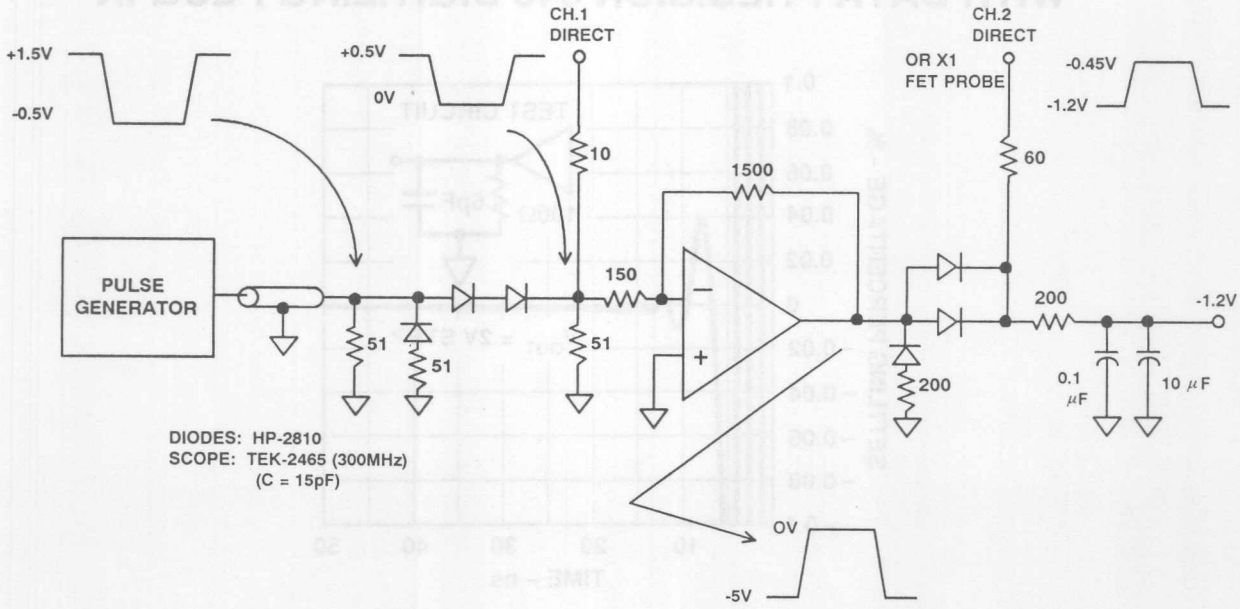
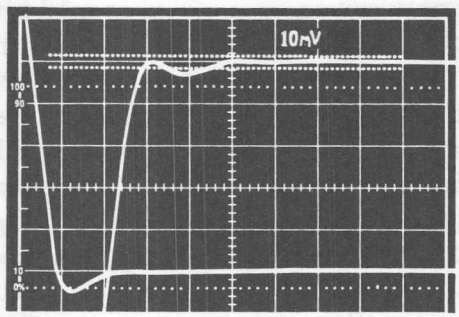


Figure 11.23

SETTLING TIME MEASUREMENT USING OVERDRIVE-LIMITING TEST CIRCUIT



GAIN = – 10; 5V OUTPUT; ERROR WINDOW (±5mV) = 0.1%; 5ns/DIV

Figure 11.24

AD9620 BUFFER SETTLING TIME MEASURED DIRECTLY WITH DATA PRECISION 640 DIGITIZING PLUG-IN

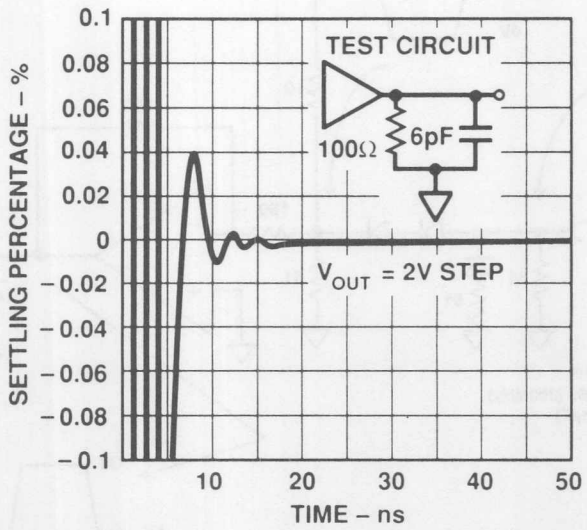


Figure 11.25

In order to duplicate test results such as those described above, excellent high speed layout techniques must be observed! Large-area ground plane, compact layout, appropriate decoupling is mandatory. Molded plastic socket assemblies are absolutely forbidden! If sockets must be used, individual pin sockets on each IC pin may be acceptable, provided the IC is mounted flush on the PCB. There must be no excess lead length between the tops of the pin sockets and the bottom of the IC.

OP AMP NOISE AND HOW TO AVOID IT

JAMES M. BRYANT

INTRODUCTION

This section of the seminar considers the two categories of noise found in op-amp circuitry and discusses how they can be minimized in practical applications.

These two categories of noise are the internal noise of the circuits, that is the op-amp itself and the components of its immediate circuitry, and external noise from elsewhere in the system. We shall consider DC error sources in this section as well, since it is quite reasonable to treat DC errors as noise.

TYPES OF NOISE

11

- **NOISE GENERATED WITHIN A CIRCUIT**
- **EXTERNAL NOISE (Which is a signal which is wanted, in a place where it isn't.)**

Figure 11.26

UNCORRELATED NOISE VOLTAGES ADD AS THE ROOT OF THE SUM OF THE SQUARES

- **For N uncorrelated noise voltages V_1, V_2,....V_N the total noise voltage Vn is given by**

$$V_n = \sqrt{V_1^2 + V_2^2 + ...V_N^2}$$

- **If any noise voltage is more than 3-5 times another we may generally ignore the smaller.**

Figure 11. 27

The general principle of noise calculation is that uncorrelated noise sources add in a root sum of squares manner, which means that if a noise source has a contribution to the output noise of a system which is less than 20% of the amplitude of the noise from some other noise source in the system then its contribution to the total system noise will be less than 2% of the total and that noise source can almost invariably be ignored - in many cases noise sources smaller than 33% of the largest can be ignored. Remember, though, that design changes can change the relative amplitudes of noise sources so that a previously unimportant noise source becomes dominant. This means that all noise sources must be re-evaluated when a design is changed.

INTERNAL CIRCUIT NOISE

The three noise sources in an op-amp circuit are the voltage noise of the op-amp, the current noise of the op-amp (there are two uncorrelated sources, one in each input), and the Johnson noise of the resistances in the circuit.

THERE ARE THREE SOURCES OF NOISE WITHIN A CIRCUIT

- Voltage Noise of the Op-Amp
- Current Noise of the Op-Amp
- Johnson Noise of the Resistors in the Circuit

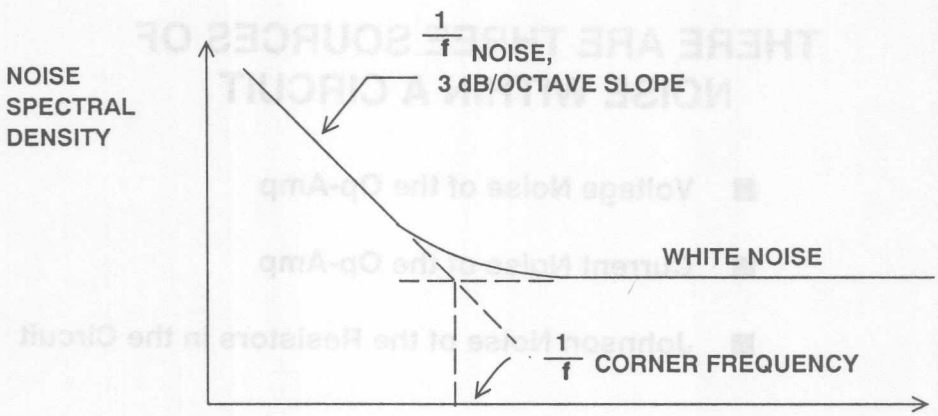
Figure 11.28

Operational amplifier noise has two components - white noise at medium frequencies and low frequency noise whose spectral density is inversely proportional to the square root of the frequency. It should be noted that, though both the voltage and the current noise may have the same characteristic behavior, in a particular amplifier the 1/f corner frequency is not necessarily the same for voltage and current noise (it is usually specified for voltage noise).

The low-frequency noise is generally known as 1/f noise (the noise *power* obeys a 1/f law - the noise voltage or noise current is proportional to $1/\sqrt{f}$). The frequency at which the 1/f noise spectral density equals the white noise is known as the "1/f Corner Frequency" and is a figure of merit for the op-amp, with low values indicating better performance. Values of 1/f corner frequency vary from a few Hz for the most modern low noise low frequency amplifiers to several hundreds, or even thousands, of Hz for some high speed op-amps where process compromises favor high speed rather than low frequency noise.

Voltage noise, which appears in series with the two input terminals of the op-amp, can have spectral densities of under in the best low noise op-amps.

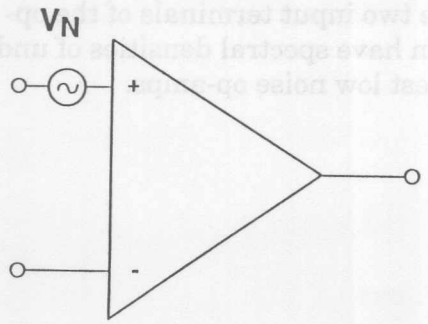
OP AMP NOISE CHARACTERISTICS



■ Voltage & Current Noise have the same characteristics but the 1/f Corner Frequencies for Voltage and Current Noise in the same Amplifier are not necessarily the same.

Figure 11.29

VOLTAGE NOISE IN OP AMPS



- The best low-noise Op-Amps have voltage noise

$$<1nV/\sqrt{Hz}$$

- 1/f Corner Frequencies can be as low as 2.7 Hz (OP-27) or as high as 1-2 KHz in high speed op-amps where low 1/f noise is sacrificed for better HF performance.

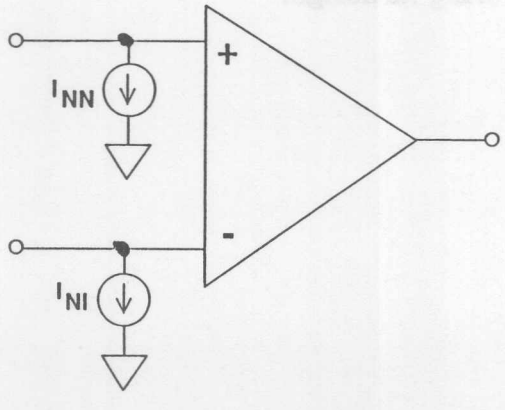
Figure 11.30

Current noise appears at each of the input terminals of an op-amp. In conventional (voltage feedback) op-amps the noise currents in each input are approximately equal in amplitude, though not strongly correlated (but they may be weakly correlated to the voltage noise). The noise currents in the inverting and non-inverting inputs of current feedback (transimpedance) op-amps are not matched in any way - they are neither equal nor correlated. Current noise varies very widely from type to type of amplifier, by at least 10^4:1. from under 0.1 fA/$\sqrt{Hz}$ in the lowest bias current BIFET op-amps to several pA/$\sqrt{Hz}$ in bias-compensated bipolar op-amps and in high speed op-amps.

Current noise is often inadequately specified. In op-amps where the input stage is a simple long-tailed pair of bipolar or field-effect transistors the whole of the bias current flows in the input junction and the current noise floor is equal to the Schottky noise (or "shot noise") of the bias current which can be calculated from the bias current. But in bias compensated amplifiers and current feedback amplifiers there are several currents flowing internally through each input node and it is not possible to predict the noise current from the external bias current and if the noise current is not specified it cannot be calculated. It is therefore important to be aware of the structure of an op-amp if its noise current is likely to be of importance.

The noise current of an op-amp is important if it flows in an impedance to produce a voltage, which the op-amp then amplifies. Consequently the impedance (Z) seen by each input of an op-amp produces a noise voltage of I_nZ, where I_n is the noise current at that input.

CURRENT NOISE IN OP AMPS

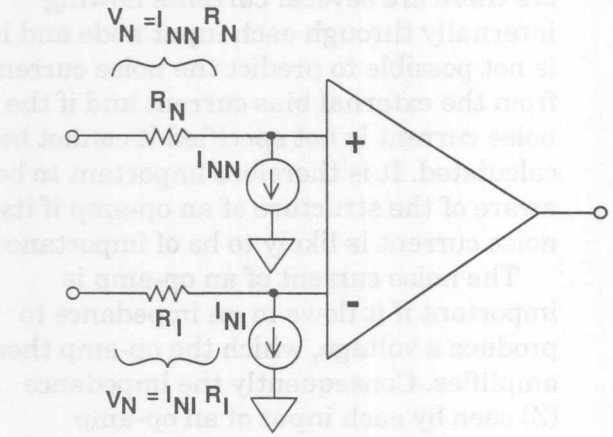


- In conventional (voltage feedback) op-amps the current noise in the inverting and non-inverting inputs are equal, but are not correlated.
- In current feedback (transimpedance) op-amps the current noise in the inverting and non-inverting inputs may be totally different (and is certainly uncorrelated).

11

Figure 11.31

INPUT NOISE CURRENT



- **Conventional (Voltage Feedback) Op-Amps without bias-compensated input structures have white noise approximately equal to the Schottky Noise (or Shot Noise) of their Bias Current.**

$$I_n = \sqrt{2IqB}$$

(I is the bias current, q is the electron charge and B is bandwidth)

- **Current Feedback (Transimpedance) and Bias-Compensated Op-Amps do not.**

- **Current Noise flows in Op-Amp Input Source Impedances to produce noise voltages.**

Figure 11.32

JOHNSON NOISE

The impedance is resistive there is a second noise voltage to be reckoned with. All resistors have a noise voltage, known as thermal, or Johnson, noise, of $\sqrt{4kTBR}$, where k is Boltzmann's constant (1.38×10^{-23} J/K), T is the absolute temperature, B is the bandwidth, and R is the resistance.[1] Every resistance in a circuit contributes noise to it. Although the noise contributions from most resistors are insignificant the noise contribution of each resistor in a noise-critical circuit should be checked at some point during its design.

JOHNSON NOISE

- ALL RESISTANCES (BUT *NOT* REACTIVE IMPEDANCES) HAVE THERMAL NOISE OF

  $\sqrt{4kTBR}$

- WHERE k IS BOLTZMANN'S CONSTANT (1.38×10^{-23} J/K)
- T IS THE ABSOLUTE TEMPERATURE
- B IS THE BANDWIDTH & R IS THE RESISTANCE
- EVERY RESISTANCE IN A CIRCUIT WILL CONTRIBUTE TO ITS NOISE
- A 1000 Ω RESISTOR GENERATES 4nV/$\sqrt{Hz}$ @ 25°C

Figure 11.33

DOMINANT NOISE SOURCES

We have already pointed out that any noise source which produces less than one fifth of the noise of some other source can usually be ignored. (Both noise voltages must be referred to the same point in the circuit.) To analyze the noise performance of an op-amp circuit we must assess the noise contributions of each part of the circuit and determine which are significant. To simplify the following calculations we shall work with noise spectral densities rather than actual voltages to leave bandwidth out of the expressions (the noise spectral density, which is generally expressed in nV/$\sqrt{Hz}$, is equivalent to the noise in a 1 Hz bandwidth).

If we consider the circuit in Figure 11.34, which is an amplifier consisting of an op-amp and three resistors (R_1 represents the source resistance at node A), we can find six separate noise sources: the Johnson noise of the three resistors, the op-amp voltage noise, and the current noise in each input of the op-amp. Each has its own contribution to the noise at the amplifier output. (Noise is generally specified r.t.i., or referred to the input, but it is often simpler to calculate the noise at the output and then divide it by the *signal* gain (not the *noise* gain) of the amplifier to obtain the r.t.i. noise).

A signal applied to input A (B being grounded) sees a gain of

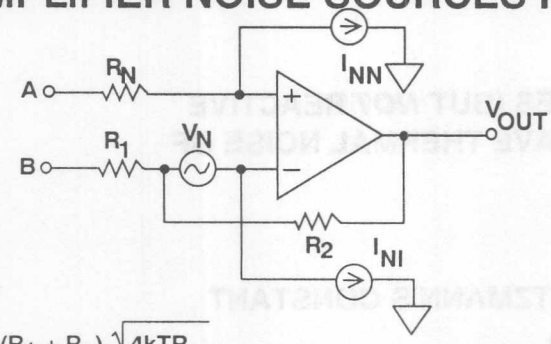
$$\frac{R_1 + R_2}{R_1} \quad \text{or} \quad 1 + \frac{R_2}{R_1} \quad [1]$$

Whereas a signal applied to B (A being grounded) sees a gain of

$$\frac{-R_2}{R_1} \quad [2]$$

These are the non-inverting and inverting gains, respectively, of the amplifier.

AMPLIFIER NOISE SOURCES REFERRED TO OUTPUT



GAIN TO OUTPUT

A: $\frac{R_1+R_2}{R_1} = 1 + \frac{R_2}{R_1}$ [1]

B: $\frac{-R_2}{R_1}$ [2]

$\frac{(R_1 + R_2)\sqrt{4kTR_N}}{R_1}$ [A] JOHNSON NOISE IN R_N (AMPLIFIED BY [1])

$\frac{I_{NN}R_N(R_1 + R_2)}{R_1}$ [B] CURRENT NOISE (NON-INVERTING INPUT, FLOWING IN R_N, AMPLIFIED BY [1])

$\frac{V_N(R_1 + R_2)}{R_1}$ [C] AMPLIFIER VOLTAGE NOISE (AMPLIFIED BY [1])

$\frac{R_2\sqrt{4kTR_1}}{R_1}$ [D] JOHNSON NOISE R_1 (AMPLIFIED BY [2])

$\sqrt{4kTR_2}$ [E] JOHNSON NOISE R_2

$I_{NI}R_2$ [F] CURRENT NOISE (NON-INVERTING INPUT, FLOWING IN R_2)

Figure 11. 34

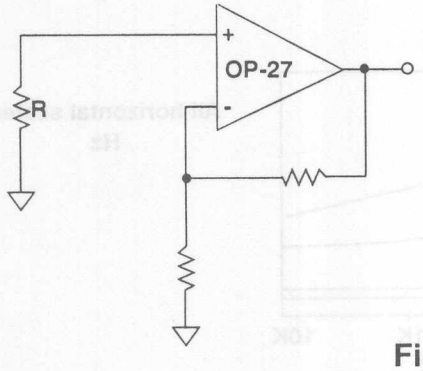
The current noise of the non-inverting input, I_{NN}, flows in R_N and gives rise to a noise voltage of $I_{NN}R_N$, which is amplified by [1], as are the op-amp noise voltage, V_N, and the Johnson noise of R_N, which is $\sqrt{4kTR_N}$. The Johnson noise of R_1 is amplified by [2], and the Johnson noise of R_2 is not amplified at all but is buffered directly to the output. The current noise of the non-inverting input, I_{NI}, does not flow in R_1, as might be expected - negative feedback around the amplifier works to keep the potential at the inverting input unchanged, so that a current flowing from that pin is forced, by negative feedback, to flow in R_2 only, resulting in a voltage at the amplifier output of $I_{NI}R_2$ (we could equally well consider the voltage caused by I_{NI} flowing in the parallel combination of R_1 & R_2 and then amplified by the noise gain of the amplifier (see below) but the results are identical - only the calculations are more involved).

If we consider these six noise contributions we see that if R_N and R_2 are low then the effect of current noise and Johnson noise will be minimized and the dominant noise will be the op-amp's voltage noise. As we increase resistance both Johnson noise and the voltage noise produced by noise currents will rise. If noise currents are low then Johnson noise will take over from voltage noise as the dominant contributor. Johnson noise, however, rises with the square root of the resistance, while the current noise voltage rises linearly with resistance, so ultimately, as the resistance continues to rise, the voltage due to noise currents will become dominant. An example is shown in Figure 11.35.

These noise contributions we have analyzed are not affected by whether the input is connected to node A or node B (the other being grounded or connected to some other low-impedance voltage source), which is why the non-inverting gain $(1 + R_2/R_1)$, which is seen by the voltage noise of the op-amp, V_N, is some-

EFFECT OF SOURCE RESISTANCE ON NOISE

Example: OP-27
Voltage Noise = 3nV/$\sqrt{Hz}$
Current Noise = 1pA/ $\sqrt{Hz}$
(T = 25°C)



CONTRIBUTION FROM	VALUES OF R		
	0	3kΩ	300kΩ
AMPLIFIER VOLTAGE NOISE	3	3	3
AMPLIFIER CURRENT NOISE FLOWING IN R	0	3	300
JOHNSON NOISE OF R	0	7	70

RTI NOISE (nV/ $\sqrt{Hz}$)

Dominant Noise is Highlighted

Figure 11.35

times known as the "noise gain" of the amplifier. The difference between the noise gain and the inverting gain to signals applied to node B can be important at low gains - if we program a gain of -1 by making R_1 = R_2 then the amplifier noise will see a gain of 2 and the signal/noise ratio will be worsened by a factor of 2, if the gain is smaller than this the degradation will be even worse. This can be important in the design of low-pass filters, and also in determining the stability of op-amps without full frequency compensation (see below).

We thus see that choice of an op-amp for low noise depends greatly on the impedances involved in the circuit. For low impedance circuitry amplifiers with low voltage noise, such as the OP-27, will be the obvious choice, since they are inexpensive and their comparatively large current noise will not affect the application. At medium resistances, unless we use an absurdly noisy amplifier, we will find that the Johnson noise of our resistors is dominant, while at very high resistances we must choose an op-amp with the smallest possible current noise, such as the AD549 or AD645.

Until recently BIFET amplifiers tended to have comparatively high voltage noise, though very low current noise, and were thus more suitable for low noise applications in high impedance circuitry than at low impedance. Recently the AD645 and AD743/AD745 have become available, which have very low values of both voltage and current noise. The AD645 specifications at 10kHz are 10nV/$\sqrt{Hz}$ and 0.6fA/$\sqrt{Hz}$, and the AD743/AD745 specifications at 10 kHz are 2.9nV/$\sqrt{Hz}$ and 6.9fA/$\sqrt{Hz}$. These make possible the design of low-noise amplifiers which have low noise over a wide range of source impedances.

DIFFERENT AMPLIFIERS ARE BEST AT DIFFERENT IMPEDANCE LEVELS

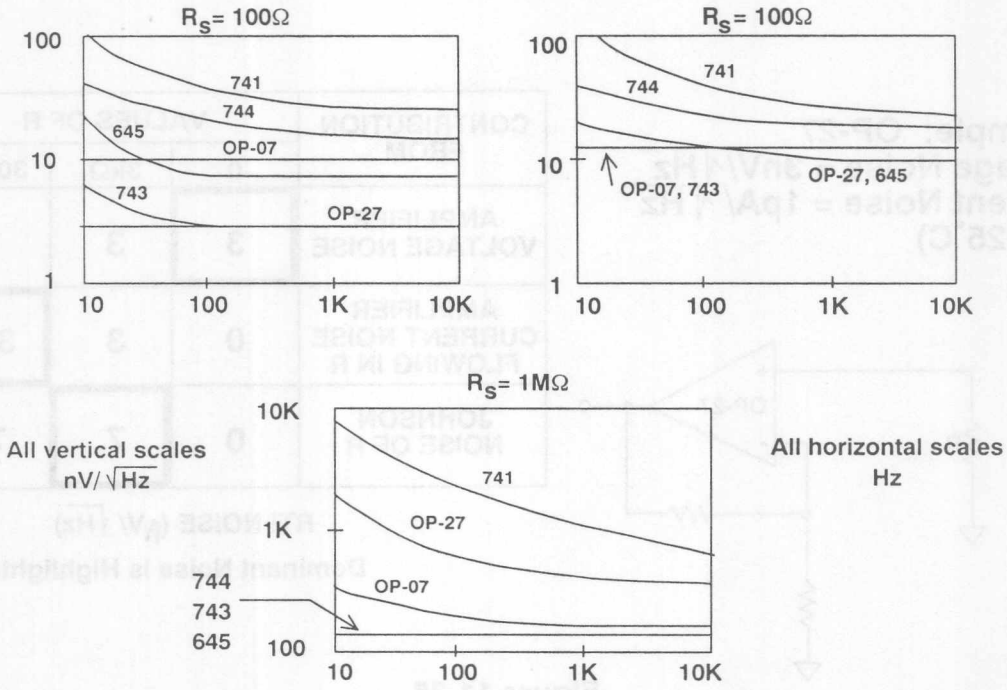


Figure 11.36

NOISE FIGURE

The "noise figure" of an amplifier is defined at a particular source resistance. It is the ratio, expressed in dB, of the noise of the amplifier when driven by a perfect resistance of the particular value to the noise of a perfect (noise-free) amplifier operated under the same conditions. Noise figure is a useful parameter for RF amplifiers, which are generally operated with resistive termination of 50 Ω or 7 5 Ω, but since operational amplifiers are operated over a very wide range of conditions and termination impedances noise figure is not a useful op-amp parameter and it is never specified. (Whatever resistance is chosen would be wrong, and the lack of correlation of voltage and current noise in an op-amp make it impossible to calculate the noise figure at one resistance from its value at another - if it is needed it may be calculated from the voltage and current noise figures.)

INSTABILITY & ITS CURES

A common cause of unexpectedly large noise in op-amp circuitry is high frequency oscillation. Integrated circuit chips contain transistors with f_t of hundreds or thousands of MHz and if they are inadequately decoupled they may oscillate at VHF or UHF. Such oscillation may not prevent low frequency operation of the circuit, but it will certainly prevent the achievement of low noise and high DC accuracy. It can also be hard to detect, since few oscilloscopes have sufficient bandwidth to detect a signal of a few hundred MHz - and, indeed, the capacity of the oscilloscope probe may be sufficient to stop the oscillation, so the circuit works properly when an oscilloscope is attached to it!

The best way to detect such VHF oscillation is to use a broadband spectrum analyzer (to at least 1 GHz) since the probe need not actually contact the circuit to detect an oscillation. It is best to search

NOISE FIGURE

- IS *ALWAYS* SPECIFIED AT A PARTICULAR SOURCE RESISTANCE
- IT IS THE RATIO OF THE NOISE OF AN AMPLIFIER OPERATED AT THAT SOURCE RESISTANCE TOTHE NOISE OF A PERFECT AMPLIFIER OPERATED AT THE SAME SOURCE RESISTANCE
- IT IS GENERALLY GIVEN IN dB
- IT IS NOT A PRACTICAL SPECIFICATION FOR OP-AMPS AND IS RARELY SPECIFIED FOR THEM

Figure 11.37

PARASITIC OSCILLATION

- I.C. OP-AMPS CONTAIN TRANSISTORS WITH f_t OF HUNDREDS OF MHz
- THEY CAN OSCILLATE AT HUNDREDS OF MHz

Figure 11.38

DETECTING PARASITIC OSCILLATION

- **THE CAPACITANCE OF AN OSCILLOSCOPE PROBE MAY BE SUFFICIENT TO STOP PARASITIC OSCILLATION**
- **DETECT IT WITH A BROADBAND SPECTRUM ANALYZER WITH ITS PROBE CLOSE TO, BUT NOT TOUCHING,THE NODE BEING ANALYZED**
- **DRIVE THE INPUT WITH A FULL-SCALE L.F SIGNAL DURING THIS TEST BECAUSE SOME PARASITICS OCCUR ONLY AT CERTAIN INPUT LEVELS**

Figure 11.39

for parasitic oscillations with a full-scale input signal to the circuit being tested since sometimes parasitic oscillation only occurs at a particular input level and not over the whole range.

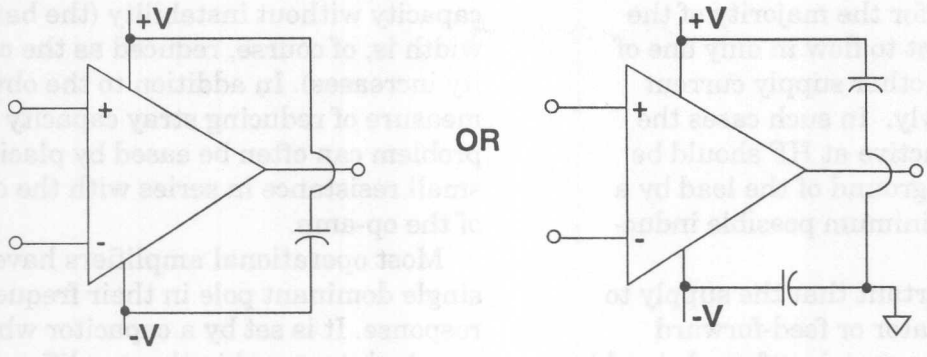
The commonest cause of HF instability is inadequate HF supply decoupling. Internal HF currents within the supplies of an op-amp should be short-circuited by decoupling the supplies with a capacitor having very low HF impedance - this means that the capacitor itself must have low inductance, and that its leads and the PC tracks to them must also have low inductance. (A common layout mistake is to decouple the supply of an IC in one row to the ground bus of the ICs in an adjacent row - the inductance from the supply to the grounding point on the bus may well be low - but the inductance of the length of ground bus from the capacitor grounding point to the ground pin of the IC being grounded may be intolerable.)

Paper, foil, electrolytic and plastic film capacitors all tend to be inductive. The best HF decoupling capacitors are low ESR and ESL monolithic ceramic types, preferably surface mounted, but otherwise with leads of less than 1.5 mm.

Not only is it important to ensure that the internal device currents are properly decoupled at HF, it is also important to ensure that HF load currents have the lowest possible impedance of return path.

Many IC processes make NPN transistors which are much faster than their PNP transistors (or vice versa), although this is not the case with Analog Devices' "CB" process, which makes complimentary bipolar transistors of roughly equal speed.

AMPLIFIER DECOUPLING



- TO PREVENT PARASITIC OSCILLATION DECOUPLING CAPACITORS MUST HAVE LOW INDUCTANCE TO PROVIDE A MINIMUM IMPEDANCE PATH TO H.F. CURRENTS IN THE I.C.
- This means low inductance capacitors (monolithic ceramic and NOT foil or electrolytic types).
- It also means low inductance leads and PC tracks (surface mount or lead lengths <1.5 mm, PC tracks as wide as possible and no longer than a few mm)

Figure 11.40

SOME OP AMPS HAVE ONE SUPPLY WHOSE DECOUPLING IS MORE CRITICAL THAN THE OTHER. EXTRA CARE SHOULD BE TAKEN TO DECOUPLE THE "ACTIVE SUPPLY"

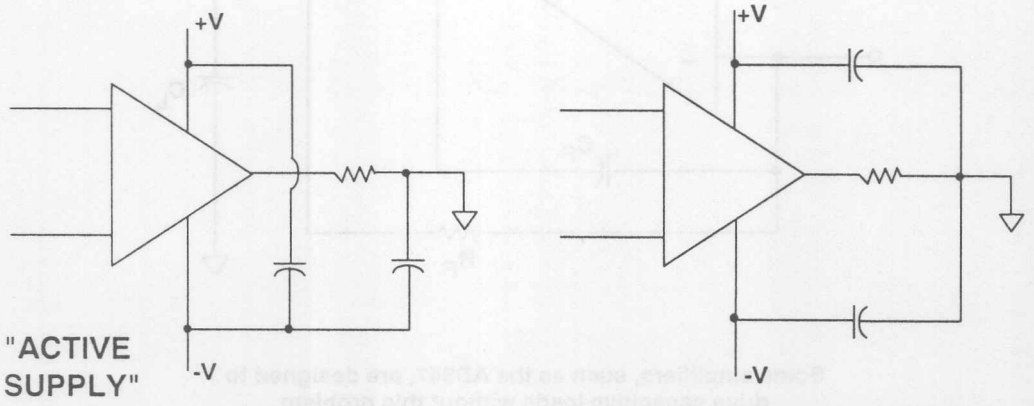


Figure 11.41

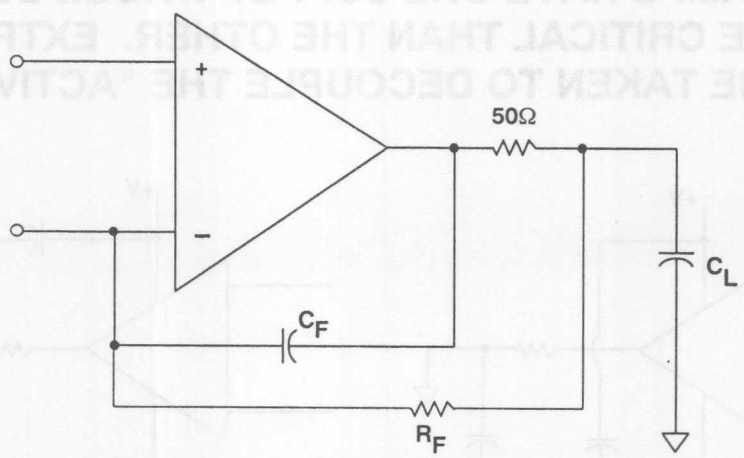
Where transistor speeds are unequal it is quite common for the majority of the HF output current to flow in only one of the supplies, the other supply current varying only slowly. In such cases the supply which is active at HF should be decoupled to the ground of the load by a capacitor with minimum possible inductance.

It is also important that the supply to which any integrator or feed-forward capacitor in the op amp is referred should be decoupled to the load ground in the same way. The critical supply of many op amps is listed in the application note at the end of this section.[2]

Two other sources of instability are reactive loads and insufficient frequency compensation. Many operational amplifiers oscillate if required to drive capacitances of more than a few picofarads, although some (such as the AD847) are specially designed to drive any value of capacity without instability (the bandwidth is, of course, reduced as the capacity increases). In addition to the obvious measure of reducing stray capacity the problem can often be eased by placing a small resistance in series with the output of the op-amp.

Most operational amplifiers have a single dominant pole in their frequency response. It is set by a capacitor which may be integrated in the amplifier or connected externally. If the 6 dB/octave low-pass frequency response caused by this pole continues down to gains of 1 or less the amplifier is said to be fully compensated and may be used in closed loop applications at any gain. If the frequency of the pole is set higher one of the other poles in the amplifier response will take effect at a gain of G, before the gain has dropped to unity, and the gain then rolls

CAPACITIVE LOADS CAUSE INSTABILITY: ISOLATE THEM WITH A SMALL SERIES RESISTOR



Some amplifiers, such as the AD847, are designed to drive capacitive loads without this problem

Figure 11.42

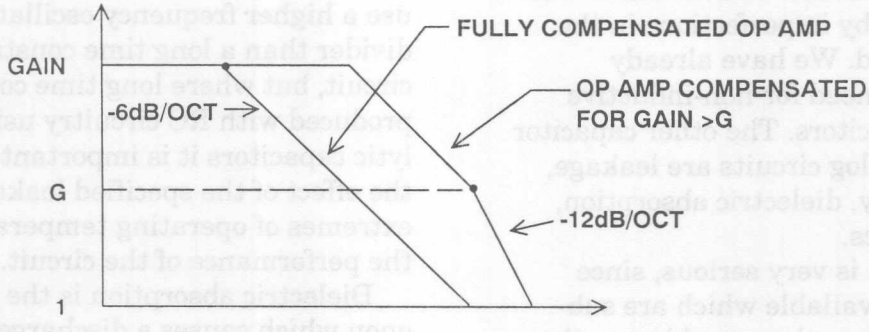
off at 12 dB/octave. In this case the amplifier has a higher gain/bandwidth product but is not stable at closed-loop gains of much less than G because the additional phase shift in the negative feedback makes it positive feedback.

If this incomplete compensation is internal the op-amp data sheet will specify "Stable at gains ≥ X" with some value of X (usually between 2 and 25). It is quite common to find families of amplifiers which are identical except for the value of the internal compensation capacitor (an example is the family of the AD847, AD848 and AD849). If an amplifier which has two pole roll-off is used at too low a closed-loop gain it will oscillate. This effect is easily overlooked during design and the resulting problems are quite commonly referred to Analog Devices' Applications Department for solution.

The simplest solution is to use an op-amp which is stable at the gain required and has sufficient bandwidth. However, if, for whatever reason, a particular op-amp must be used at a lower gain than is stable, there is a solution which is practical (but has the disadvantage of worsened noise performance).

Consider Figure 11.44. If R_1 is omitted the amplifier has a gain of 1 to a signal and a noise gain of 2 (see the formulas [1] and [2] earlier in this section) and if it uses an op-amp which is stable only at gains ≥5 it will probably oscillate. If R_1 is present, however, the signal gain is unaffected but the noise gain is increased to 12 and the circuit becomes stable. *But* the signal to noise ratio becomes six times worse (if the dominant noise is the op-amp voltage noise) since the noise gain has increased by a factor of 6. In many applications this is unimportant, so the technique is a useful one.

FULLY AND PARTIALLY COMPENSATED OP AMPS



■ A fully compensated op amp has a roll-off of 6 dB/octave to unity gain

■ A partially compensated amplifier has a larger gain/bandwidth product (for the same basic amplifier) but the roll-off increases to 12 dB/octave above a certain frequency (when the gain is less than G). As a consequence, such amplifiers are not stable in closed-loop applications with gains < G.

Figure 11.43

11

AMPLIFIERS WHICH ARE NOT UNITY GAIN STABLE MAY BE USED AT UNITY GAIN IF THEIR NOISE GAIN IS INCREASED BY THE USE OF R_1.

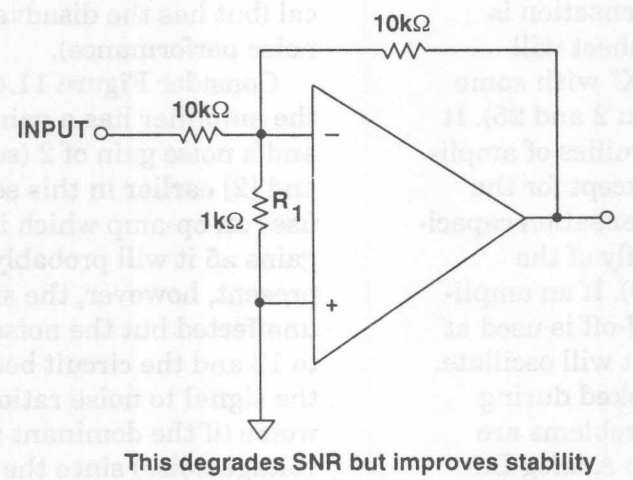


Figure 11.44

CIRCUIT NOISE FROM COMPONENTS - CAPACITORS

Noise and error can be introduced into op-amp circuits by imperfections in the components used. We have already pointed out the need for non-inductive decoupling capacitors. The other capacitor problems in analog circuits are leakage, thermal stability, dielectric absorption, and microphonics.

None of them is very serious, since capacitors are available which are substantially free from these problems - the important consideration for the circuit designer is to ensure that he considers the effects of the errors on his circuit and chooses a component whose performance is adequate to its task.

The only modern capacitors with appreciable leakage are electrolytic ones (aluminium and tantalum), and the only common application where leakage presents a severe performance problem is long delay timers. Since CMOS dividers are now so cheap it is probably better to use a higher frequency oscillator and a divider than a long time constant RC circuit, but where long time constants are produced with RC circuitry using electrolytic capacitors it is important to calculate the effect of the specified leakage (at the extremes of operating temperature) on the performance of the circuit.

Dielectric absorption is the phenomenon which causes a discharged capacitor to recover a small amount of charge if it open-circuited - the amount depends on the previous state of charge. The normal application where dielectric absorption must be avoided is in the design of sample and hold circuitry, since dielectric absorption causes the hold state of a SHA to depend not only on the voltage present at the time of the sample/hold transition but also on the previous charge history of the

THE PRINCIPLE PROBLEMS WITH CAPACITORS

- **INDUCTANCE**
- **LEAKAGE**
- **TEMPERATURE COEFFICIENT**
- **DIELECTRIC ABSORPTION**
- **With modern capacitors none of them is very serious but they must be considered when designing circuits.**

Figure 11.45

capacitor. Today most SHAs contain integral capacitors and the designer need not specify a hold capacitor. However, on the occasion when a SHA is built with a discrete hold capacitor it is critically important that a capacitor is chosen with *guaranteed* dielectric absorption. This ensures that the manufacturer has tested this particular parameter. The problem is that dielectric absorption can vary quite widely from batch to batch, even with types of capacitor which are normally good. If the dielectric absorption is not tested parts from a batch with bad dielectric absorption will be found from time to time among parts of a type which is normally quite good. A guaranteed and tested part eliminates this risk.

Certain analog designs are affected by small variations of capacitance with temperature. In particular, high-K ceramic and electrolytic capacitors should not be used in accurate filter circuits since their TCs can be as high as 1000 ppm/°C. For the timing capacitors in VFC and other precision oscillators mica, ceramic and polyester parts with guaranteed TCs of a few ppm/°C are available - but use *guaranteed* parts, not generic ones or, still worse, anonymous objects from that old parts box on the workbench.

FEATURES OF COMMON CAPACITORS

TYPE	TYPICAL DIELECTRIC ABSORPTION	ADVANTAGES	DISADVANTAGES
NPO Ceramic	0.1%	Small Case Size Inexpensive Good Stability Wide Range of Values Many Vendors Low Inductance	DA too High for More than 8-Bit Applications
Polystyrene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values Good Stability	Destroyed by Temperature > +85°C Large Case Size High Inductance
Polypropylene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values	Destroyed by Temperature > +105°C Large Case Size High Inductance
Teflon	0.003% to 0.02%	Low DA Available Good Stability Operational Above +125°C Wide Range of Values	Relatively Expensive Large High Inductance
MOS	0.01%	Good DA Small Operational Above +125°C Low Inductance	Limited Availability Available only in Small Capacitance Values
Polycarbonate	0.1%	Good Stability Low Cost Wide Temperature Range	Large DA Limits to 8-Bit Applications High Inductance
Polysulfone	0.1%	Good Stability Low Cost Wide Temperature Range	Large DA Limits to 8-Bit Applications High Inductance
Monolithic Ceramic	>0.2%	Low Inductance Wide Range of Values	Poor Stability Poor DA
Mica	>0.003%	Low Loss at HF Low Inductance Very Stable Available in 1% Values or Better	Quite Large Low Values (<10nF) Expensive
Aluminium Electrolytic	High	Large Values High Currents High Voltages Small Size	High Leakage Usually Polarized Poor Stability Poor Accuracy Inductive
Tantalum Electrolytic	High	Small Size Large Values Medium Inductance Reliable	Quite High Leakage Usually Polarized Expensive Poor Stability Poor Accuracy

Figure 11.46

CIRCUIT NOISE FROM COMPONENTS - RESISTORS

In the past many resistors were noisy. Today better resistor materials and structures are available and most resistors have noise which is quite close to the Johnson noise of an ideal resistor of the same value. (This excess noise is related to the current flowing in the resistor.) Solid carbon composition resistors and ultra-high value resistors are exceptions. In general it is best to avoid cheap carbon composition resistors (but *not* carbon film resistors, which use a completely different technology).

Unfortunately it is sometimes impracticable to avoid the use of very high value resistors, although it is good practice to avoid resistors above 10 MΩ where possible. Where their use is inevitable study the data on available types and ensure that the performance of the type you choose does not compromise the performance of your system. You should also note that many types of very high value resistor have rather poor linearity (i.e. they do not (quite) obey Ohm's Law). This, again, should be checked before choosing a component.

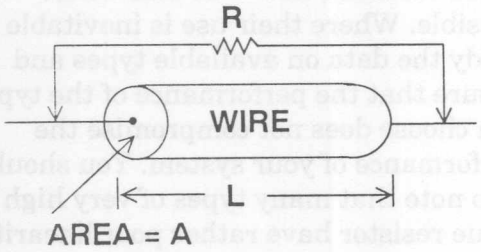
In addition to noise there are other resistor characteristics which affect the accuracy which may be achieved by amplifier circuits. We shall consider them in turn, with the lowest level effects first.

RESISTOR NOISE

- **IN GENERAL MODERN RESISTORS HAVE NOISE WHICH IS NOT MUCH GREATER THAN THEIR JOHNSON NOISE**
- **Carbon composition resistors are an exception and should be avoided where noise matters.**
- **Ultra-high resistors (>10 MΩ) can be noisy, too. They may also have other nasty habits, like non-linearity. Avoid them if you can and if you can't, read the data sheet VERY CAREFULLY.**

Figure 11.47

RESISTANCE OF CONDUCTORS

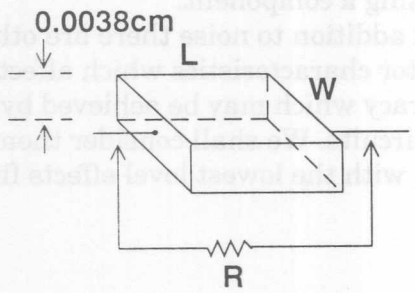


$R = \frac{\rho L}{A}$, WHERE

ρ = BULK RESISTIVITY
= 1.724×10^{-6} Ωcm FOR COPPER

A = AREA (cm^2)

L = LENGTH



THICKNESS OF STANDARD PC FOIL - O.0038cm

FOR A SQUARE OF FOIL, L = W

$\therefore R = \frac{\rho}{0.0038} \approx 0.45m\Omega$

$\therefore$ SHEET RESISTIVITY OF PC FOIL $\approx \frac{0.45m\Omega}{SQUARE}$

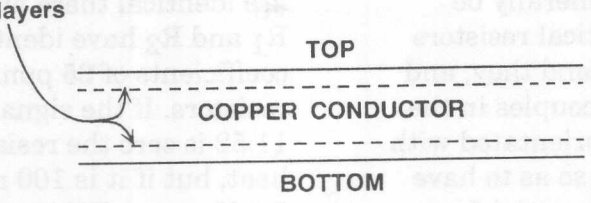
Figure 11.48

Every conductor in a circuit, including wires and PC tracks, has some resistance. Voltage drops in this resistance, though generally small, can be large enough to affect system accuracy and if there is the slightest reason to suspect that this effect will be significant it should certainly be calculated. At high frequencies the resistance of conductors rises due to "skin effect" - and this, too, should be considered.

Wherever there is a junction between two different conductors we have a voltage. If two junctions are present in a circuit we have a thermocouple, and if those two junctions are at different temperatures there will be a net voltage in the circuit. This effect is used to measure temperature, but is a potential source of inaccuracy in low level circuits, since wherever two different conductors meet we have a thermocouple (whether we think "This is a thermocouple." or not). This will cause errors if the various junctions are at different temperatures. The effect is hard to avoid since, even if we use copper conductors everywhere, every resistor contains two thermocouples. Therefore, if there is a temperature difference between the ends of a resistor (or between any other two junctions in a circuit) there will be a potential difference. Values for typical wirewound resistors are of the order of 40 μV/°C.

SKIN EFFECT

- HF Current flows only in thin surface layers



- Skin Depth: $6.61/\sqrt{f}$ cm, f in Hz
- Skin Resistance: $2.6 \times 10^{-7} \sqrt{f}$ ohms per square, f in Hz
- Since skin currents flow in both sides of a PC track, the value of skin resistance in PCBs must take account of this

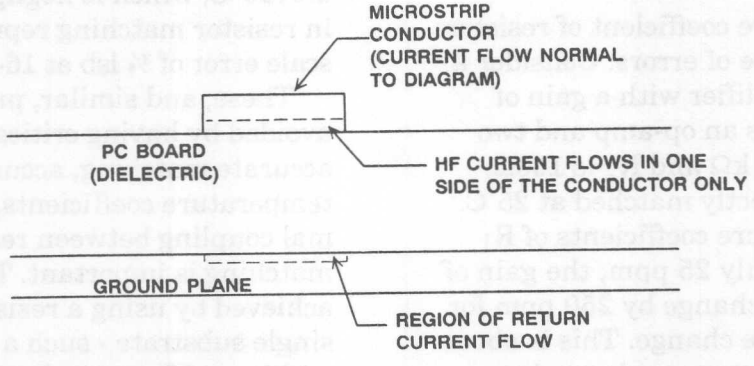
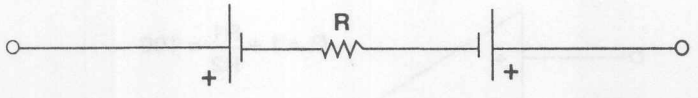


Figure 11.49

RESISTORS CONTAIN THERMOCOUPLES



- If their ends are at different temperatures they may introduce significant errors into low-level DC circuits. (A typical value for wirewound resistors is 40μV/°C temperature difference.)
- The same effect occurs wherever dissimilar conductors meet in a circuit.
- Minimize the problem by planning to minimize temperature differences at critical junctions by careful layout and avoiding heat sources.

Figure 11.50

The effect is minimized by careful design. The problem will generally be kept under control if all critical resistors have leads of equal length, and they, and any other potential thermocouples in the circuit, are positioned and orientated with respect to any heat sources so as to have minimum temperature differential from end to end. It is possible to buy resistors which are made of materials with very low thermoelectric e.m.f. These ease the problem still further but are somewhat expensive.

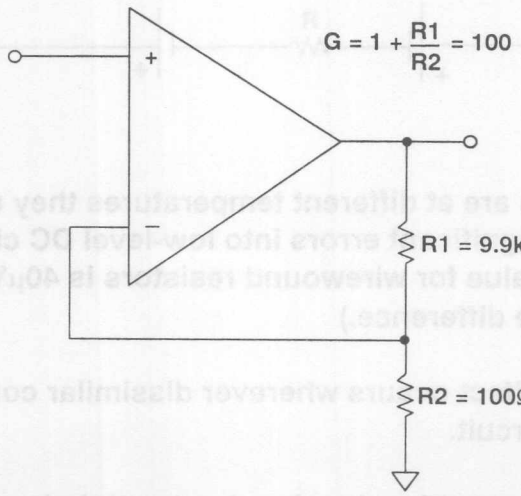
The temperature coefficient of resistors can also be a source of errors. Consider a non-inverting amplifier with a gain of exactly 100. It uses an op-amp and two resistors, R_1 is 9.9 kΩ and R_2 is 100Ω, and they are perfectly matched at 25°C.

If the temperature coefficients of R_1 and R_2 differ by only 25 ppm, the gain of the amplifier will change by 250 ppm for a 10°C temperature change. This is about 1 lsb in a 12-bit system, and a major disaster in a 16-bit system.

Even if the temperature coefficients are identical there are problems. Suppose R_1 and R_2 have identical temperature coefficients of 25 ppm and are both ¼ W resistors. If the signal input in Figure 11.52 is zero the resistors will dissipate no heat, but if it is 100 mV there will be 9.9 V across R1, it will dissipate 9.9 mW and experience a temperature rise of 1.24°C, which will change its resistance and the gain by 31 ppm. R2, with only 100 mV across it, is only heated 0.0125°C, which is negligible. This change in resistor matching represents a full-scale error of ¾ lsb at 16-bits.[3]

These, and similar, problems are avoided by having critical resistors with accurate matching, accurately matched temperature coefficients, and tight thermal coupling between resistors whose matching is important. This is best achieved by using a resistor network on a single substrate - such a network may be within an IC or may be a separately packaged thin-film resistor network.

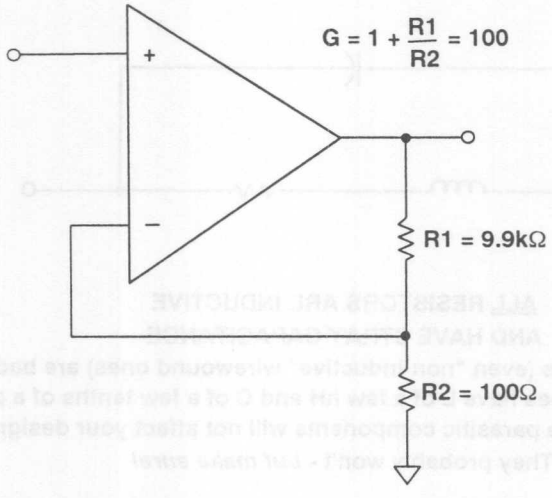
RESISTOR TEMPERATURE COEFFICIENT MISMATCHES CAUSE GAIN VARIATION WITH TEMPERATURE



If the TCs of R_1 & R_2 differ by only 25 ppm/°C a temperature change of 10°C will cause of gain change of 250 ppm - this is 1 lsb in a 12-bit system and a major disaster in a 16-bit system.

Figure 11.51

RESISTOR SELF-HEATING, EVEN IN RESISTORS WHOSE TCs ARE PERFECTLY MATCHED, CAN CAUSE GAIN VARIATION WITH INPUT LEVEL.



If R1 & R2 are ¼ W resistors with a resistance TC of 25 ppm/°C, an input of 100 mV will heat R1 by 1.24°C and R2 by a negligible amount. This will alter the gain by 31 ppm, or ¾ lsb at 16-bits.

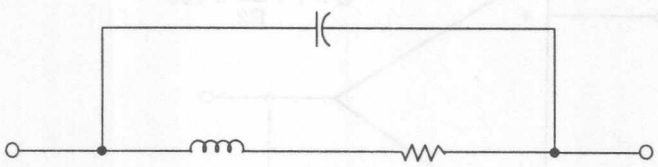
Figure 11.52

RESISTOR MATCHING

- MOST RESISTOR MATCHING PROBLEMS CAN BE ELIMINATED BY MAKING ALL RESISTORS WHOSE MATCHING IS CRITICAL ON A SINGLE THIN-FILM SUBSTRATE.
- THE NETWORK HAS TIGHT THERMAL COUPLING AND EXCELLENT MATCHING OF CHARACTERISTICS.
- This substrate may be an IC chip or a glass substrate depending on circumstances.
- This does not remove the necessity of care with layout

Figure 11.53

RESISTOR MODEL



ALL RESISTORS ARE INDUCTIVE
AND HAVE STRAY CAPACITANCE
Wirewound ones (even "non-inductive" wirewound ones) are bad, but even cermet types have L of a few nH and C of a few tenths of a pF. Verify that these parasitic components will not affect your design. They probably won't - *but make sure!*

Figure 11.54

A final consideration with resistors is their stray reactances. Wirewound resistors, even the so-called "non-inductive" types which have half their turns wound clockwise and half anticlockwise to minimize their inductance, have quite considerable inductance and capacitance (several μH and pF or even more) and must be treated with respect even at medium frequencies.

But even cermet resistors have inductance of a few nanohenries and stray capacitance of a few tenths of a pF. These stray reactances may need to be considered in higher frequency designs, as should the stray reactances of the tracks of the PCB.[4] While such issues are rarely important in high accuracy LF designs it is important that engineers are aware that resistors have such characteristics and that they may affect the performance of their circuits, since, as we have mentioned before, even low frequency ICs may contain transistors with very high frequency performance.

RESISTOR COMPARISON CHART

	TYPE	ADVANTAGES	DISADVANTAGES
DISCRETE	Carbon Composition	Lowest Cost High Power/Small Case Size	Poor Tolerance (5%) Poor Temperature Coefficient (1500ppm/°C)
	Wire-Wound	Excellent Tolerance (0.01%) Excellent TC (1ppm/°C) High Power	Reactance May be a Problem Large Case Size Most Expensive
	Metal Film	Good Tolerance (0.1%) Good TC (<1 to 100ppm/°C) Moderate Cost	Must be Stabilized with Burn-In Low Power
	Bulk Metal or Metal Foil	Excellent Tolerance (to 0.005%) Excellent TC (to <1ppm/°C) Low Reactance	Low Power Very Expensive
	High Megohm	Very High Values (10^8 - $10^{14}\Omega$) Only Choice for Some Circuits	High Voltage Coefficient (200ppm/V) Fragile Glass Case Expensive
NETWORKS	Thick Film	Low Cost High Power Laser-Trimmable Readily Available	Fair Matching (0.1%) Poor TC (>100ppm/°C) Poor Tracking TC (10ppm/°C)
	Thin Film on Glass	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance	Delicate Often Large Geometry Low Power
	Thin Film on Ceramic	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance Suitable for Hybrid IC Substrate	Often Large Geometry
NETWORKS	Thin Film on Silicon	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Suitable for Monolithic IC Construction	Some Capacitance to Substrate Low Power
	Thin Film on Sapphire	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Laser-Trimmable Low Capacitance	Higher Cost Low Power

Figure 11.55

EXTERNAL NOISE

A good definition of this type of noise is a wanted signal in a place where it is not wanted. This section considers ways in which unwanted signals can invade small-signal circuitry and damage its performance. There are four basic mechanisms: conduction, electrostatic coupling, magnetic coupling and electromagnetic coupling. If we understand the coupling mechanism responsible for a particular problem we are well on our way to solving it.

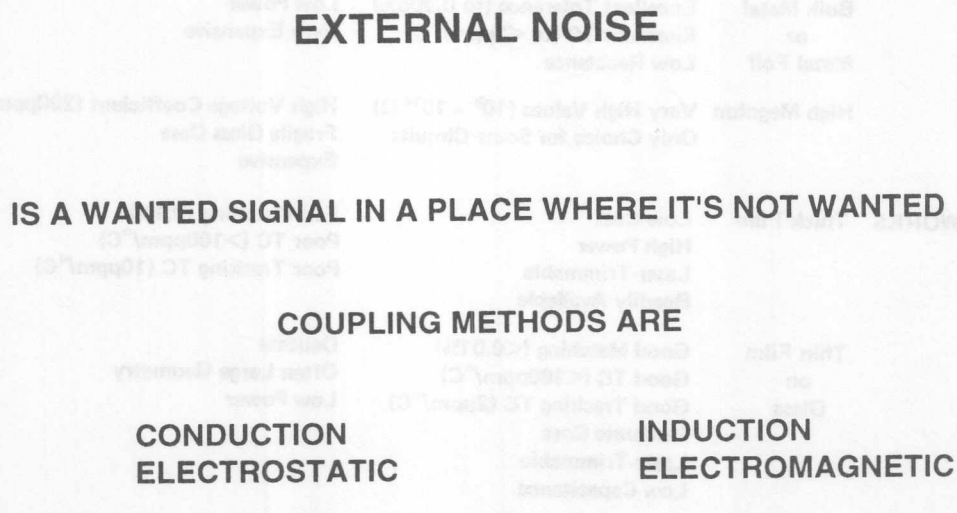


Figure 11.56

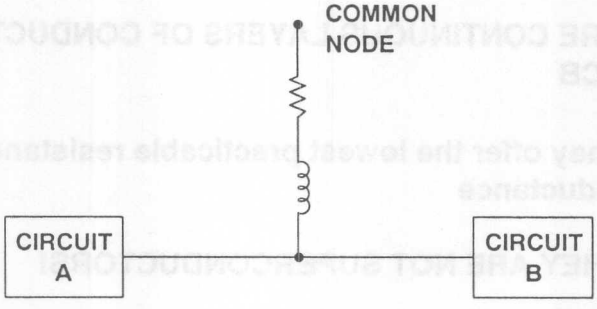
NOISE COUPLING - CONDUCTION

If two circuits share a common impedance, voltages caused by one will affect the other. This is a common mechanism for noise coupling.

If the common impedance is a power or ground conductor the problem may be cured by using separate conductors for the two circuits, or by using a shorter, fatter conductor with lower resistance and inductance. Properly decoupling of power supplies at both HF and LF is, of course, essential.

On a PCB power and ground tracks should never be minimized, but should be as wide as practicable. The ideal is to use ground planes and power planes wherever possible. These are whole layers of a PCB which are devoted to virtually continuous conductor, which is used for ground or power respectively. Ground planes offer the lowest possible ground impedance on a PCB.[5]

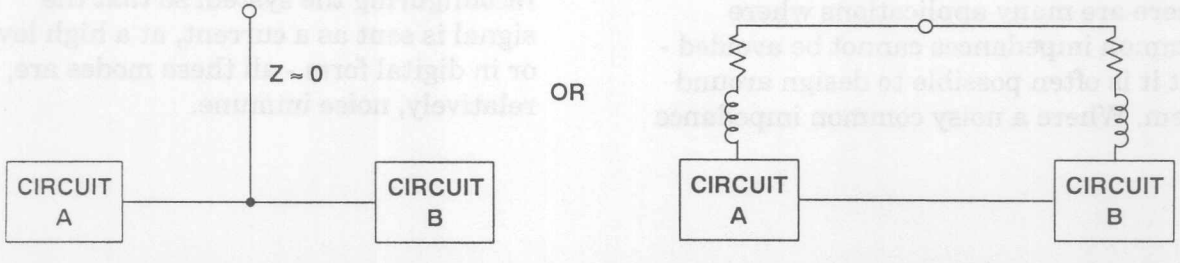
IF TWO CIRCUITS SHARE A COMMON IMPEDANCE, CURRENT FROM ONE WILL CAUSE A VOLTAGE DROP WHICH MAY AFFECT THE OTHER



Common impedances are most often ground or power lines.
Cures include removing common impedances or reducing them.

Figure 11.57

SOLUTIONS INCLUDE:



(1)
DECOUPLING POWER SUPPLIES AT HF & LF

(2)
REDUCING THE COMMON IMPEDANCE

(3)
ELIMINATING THE SHARED PATH

- Sometimes these are not possible or fully effective and more complex solutions are required.

Figure 11.58

GROUND PLANES AND POWER PLANES

- **ARE CONTINUOUS LAYERS OF CONDUCTOR IN A PCB**
- **They offer the lowest practicable resistance and inductance**
- **THEY ARE NOT SUPERCONDUCTORS!**
- **Room temperature superconductors have not yet been invented**

Figure 11.59

Room temperature superconductors have not yet (1-1-92) been invented, so even unbroken planes cannot offer zero resistance, let alone zero inductance. There are many applications where common impedances cannot be avoided - but it is often possible to design around them. Where a noisy common impedance causes signal transmission problems these may often be solved by sending the low-level signal differentially (so that common-mode noise is ignored) or reconfiguring the system so that the signal is sent as a current, at a high level, or in digital form - all these modes are, relatively, noise immune.

WHERE COMMON GROUND IMPEDANCES OR GROUND NOISE CANNOT BE REDUCED SEND SIGNALS AS CURRENTS, WORK AT HIGHER VOLTAGE LEVELS, CONVERT SIGNALS TO DIGITAL FORM BEFORE TRANSMISSION, OR SEND LOW-LEVEL SIGNALS DIFFERENTIALLY

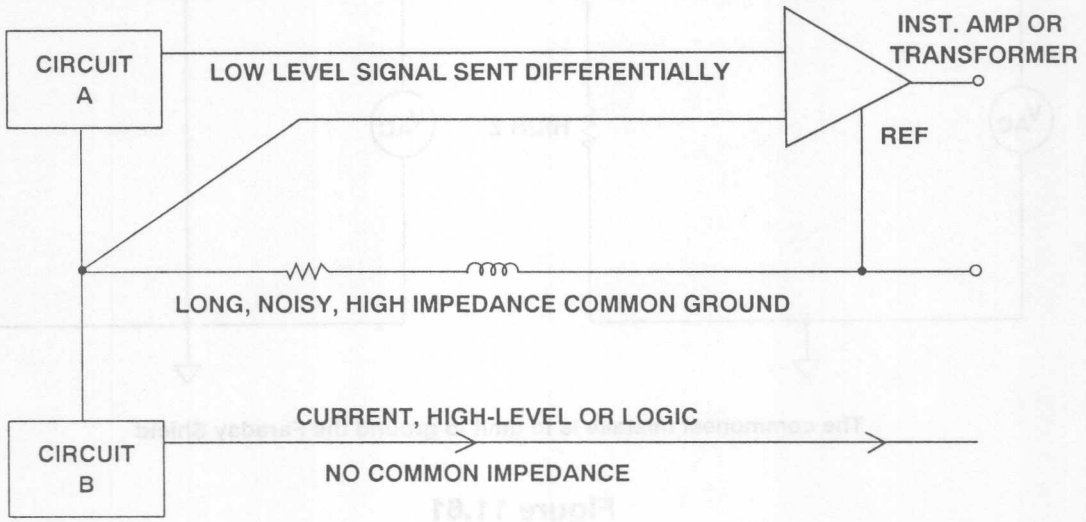


Figure 11.60

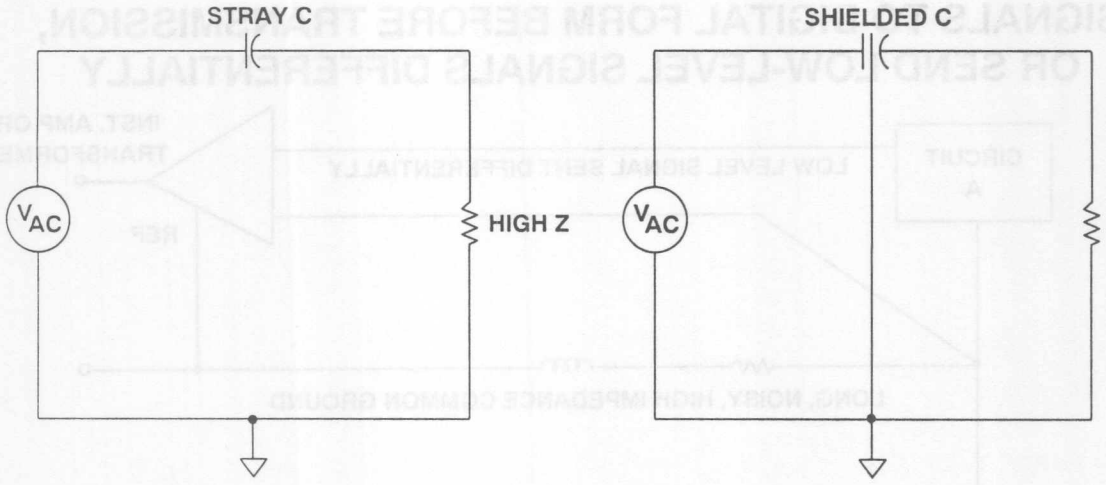
NOISE COUPLING - CAPACITIVE

In addition to the capacitors which are designed into the system, practical circuits are full of small stray capacitances. If a high impedance low-level point in a circuit is separated from a high voltage AC signal by a small distance it is probably that the stray capacitance will couple a noise signal into the low-level circuit.

Fortunately this particular source of noise is very easily cured. If a conductive shield is inserted between the plates of the stray capacitor, *and grounded*, the displacement current will flow to ground through the shield and not through the signal circuits. This conductive shield is known as a "Faraday Shield" and is easily constructed and used. It is generally very efficient, but a common fault is to fail to ground it - in which case the effective stray capacity is generally increased and the original problem is exacerbated.

Some integrated circuit packages have unconnected metal lids, which can act as ungrounded Faraday shields and thus pick up noise signals. These lids are generally made of gold-plated kovar and can be soldered carefully without risk to the chip in the package - they should generally be grounded, but it is sometimes better to connect them to other points in the circuit. They should never be left unconnected! [6]

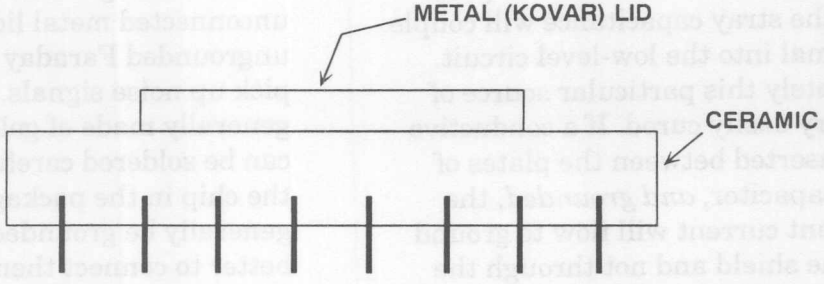
CAPACITIVE NOISE COUPLING IS EASILY MODELLED AND EASILY CURED



The commonest mistake is to omit to ground the Faraday Shield

Figure 11.61

SOME INTEGRATED CIRCUITS HAVE UNCONNECTED METAL LIDS WHICH BEHAVE AS UNGROUNDED FARADAY SHIELDS AND PICK UP NOISE



They should be grounded - they can be soldered without risk.

DO NOT GROUND LIDS WHICH ARE CONNECTED TO POWER!

Figure 11.62

NOISE COUPLING - MUTUAL INDUCTANCE

If a current flows in a conductor it produces a magnetic field. If the current changes the magnetic field strength changes. If the magnetic field around a conductor changes it produces an e.m.f. in that conductor. It therefore follows that if the current in a conductor changes voltages will be induced in nearby conductors. The phenomenon is known as mutual inductance. (A voltage is also induced in the original conductor by the related phenomenon of *self inductance* but we shall not consider that here.)

Mutual inductance is a powerful cause of noise. Consider a PCB where an AC current is flowing from a source to a load. If the outward and return signal paths are separated we can consider the total current path as a single-turn coil - the larger the loop area, the greater the inductance. If there is another such loop nearby we find that current changes in one loop produce voltages in the other - the two are coupled by mutual inductance.

Once the problem is stated in this way it is obvious that it may be attacked by reducing the areas of both loops and increasing their separation.[7]

Magnetic shielding is also possible. At high frequency a conductor will act as a magnetic shield provided that the conductor thickness is greater than the skin depth at that frequency - this tells us that standard PC foil acts as a magnetic screen above 12 MHz or so and that a room-temperature superconductor would be very useful! In the absence of room-temperature superconductors a high permeability material such as mu-metal will provide magnetic shielding at DC and LF but it is best avoided, where possible, because of its cost, weight, and fragile magnetic characteristics (a single blow will affect its grain-orientation and reduce its permeability).

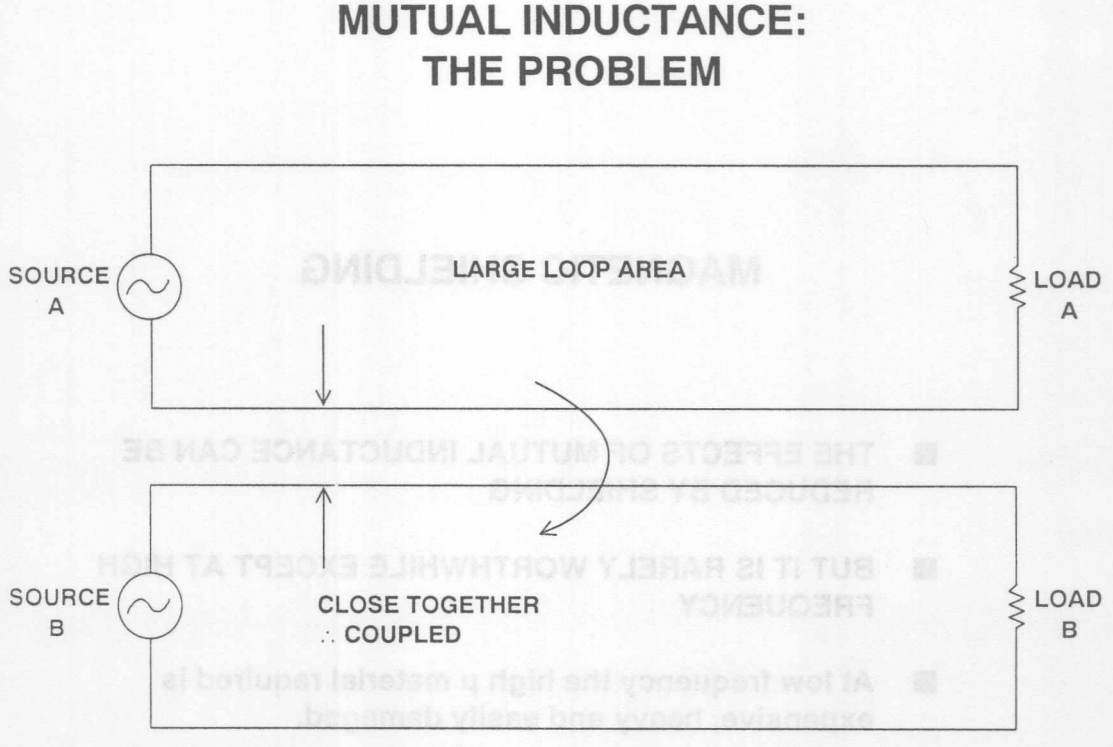


Figure 11.63

MUTUAL INDUCTANCE: THE CURE

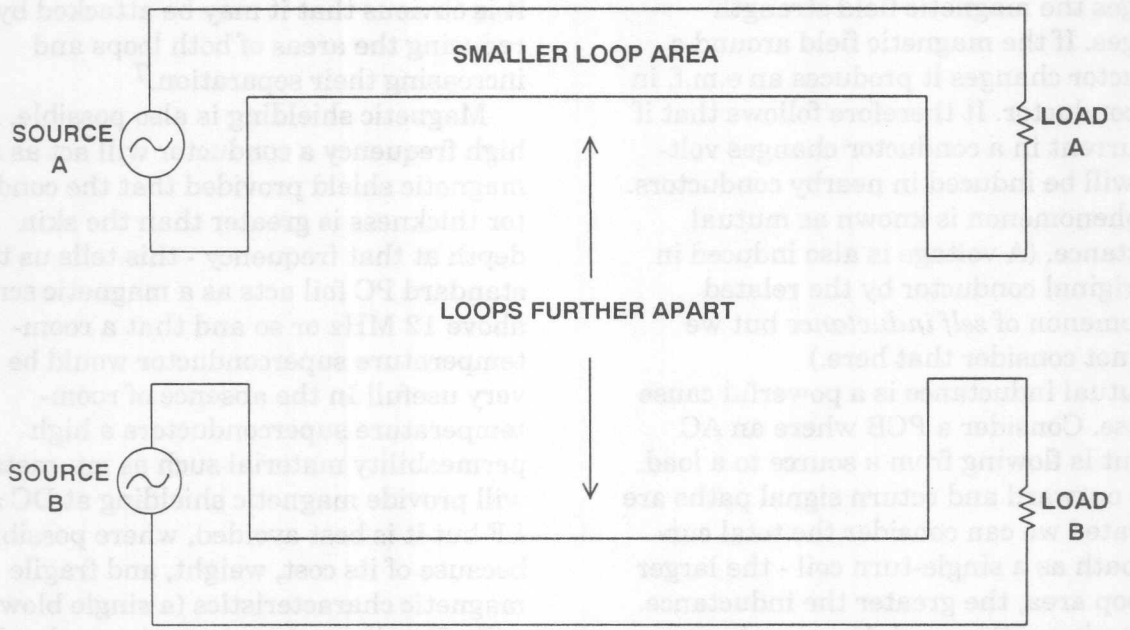


Figure 11.64

MAGNETIC SHIELDING

- THE EFFECTS OF MUTUAL INDUCTANCE CAN BE REDUCED BY SHIELDING
- BUT IT IS RARELY WORTHWHILE EXCEPT AT HIGH FREQUENCY
- At low frequency the high μ material required is expensive, heavy and easily damaged.

Figure 11.65

NOISE COUPLING - ELECTROMAGNETIC INTERFERENCE (EMI)

The World is full of radio transmitters. In addition to radio hams, CBers, policemen, security men, pizza delivery trucks, yuppies with portable telephones, radio and TV transmitters, garage door openers, microwave proximity detectors on supermarket doors and traffic lights, radars in ships, aeroplanes and speed traps, and the odd international terrorist - all of which deliberately produce and radiate electromagnetic radiation in the RF spectrum - there are also innumerable natural and non-deliberate sources of such radiation: lightning, the Sun, microwave ovens, medical diathermy, industrial heating and many more. It is folly to assume that your electronic equipment will never be required to perform in an environment where there is a field strength of a few volts per meter.

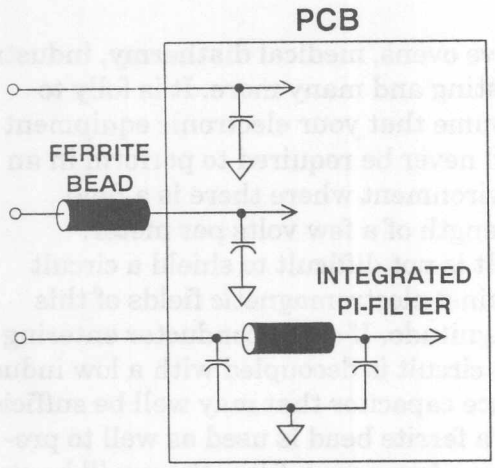
It is not difficult to shield a circuit against electromagnetic fields of this magnitude. If every conductor entering the circuit is decoupled with a low inductance capacitor that may well be sufficient - if a ferrite bead is used as well to produce a low-pass L filter there will be even more protection.

ELECTROMAGNETIC NOISE INTERFERENCE

- **The world is full of radio transmitters.**
- **Police, taxis, broadcast, amateur, CB, cellular and cordless telephones, telemetry and garage door openers.**
- **Do not imagine that your circuit will never encounter one.**

Figure 11.66

EMI PREVENTION



- SINGLE CERAMIC CAPACITOR
- FERRITE BEAD AND CAPACITOR
- INTEGRATED PI-FILTER

WHERE HIGH E-M FIELDS ARE ENCOUNTERED, CIRCUITRY SHOULD BE SCREENED BY A GROUNDED CONDUCTING ENCLOSURE

Figure 11.67

If any port turns out to be more vulnerable it is possible to buy, quite cheaply, an integrated π-filter, consisting of two ceramic capacitors and a ferrite bead in a single small "epoxy-blob" package.

If HF signals must enter or leave the board they should do so on a co-axial cable, which provides shielding. It may also be necessary to provide a bandpass filter to keep out of band signals from entering the board by this path.

If a circuit is particularly sensitive to EMI, or is to be used in an environment where high RF fields are likely to be encountered, it is good practice to enclose the entire circuit, or the sensitive parts of it, in a grounded conducting shield or can, which may be made of tin-plated steel or of copper foil.

PHOTOELECTRIC EFFECTS

Light is also an electromagnetic radiation, and it affects silicon junctions - all silicon diodes are photodiodes. Few amplifiers are not encapsulated in opaque packages[8] so it rarely necessary to worry about the effect of light on an IC, but diodes used in protective circuitry are often glass-encapsulated and may cause problems.

Figure 11.68 shows an example. A high voltage sensor with a low current output (a photocell or an ion detector or some similar transducer) is connected to a low-bias current op-amp configured as a current-voltage converter. To protect the op-amp against possible breakdown of the transducer there is a current-limiting resistor and a diode, which clamps the op-

PHOTOCURRENT IN GLASS DIODES CAN CAUSE HUM IN AMPLIFIERS

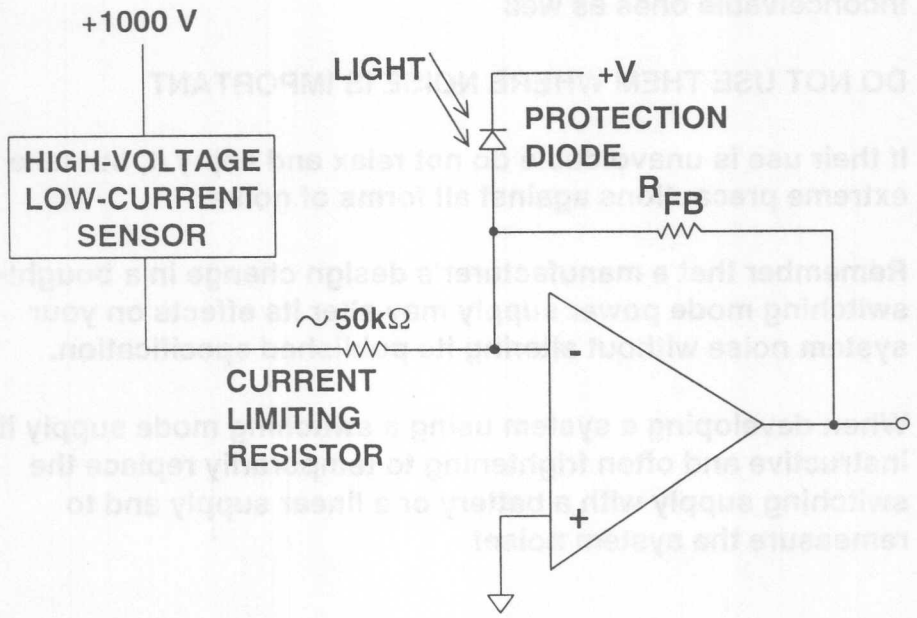


Figure 11.68

amp input to its positive supply. If the diode is a glass-encapsulated part it will be photosensitive. In most such diodes the sensitivity will be very low and may be disregarded, but occasionally a diode will be found which has higher photosensitivity. The DC photocurrent may be a problem, but much more commonly the 100 Hz (120 Hz in the USA) modulated light from fluorescent lamps modulates the photocurrent and causes hum in the amplifier. The solution is either to paint the diode black, or to use a plastic encapsulated diode.

NOISE FROM SWITCHING POWER SUPPLIES

The switching power supply offers low cost, small size, high efficiency, high reliability and the possibility of operating from a wide range of input voltages without adjustment. Unfortunately, it is very dangerous because it generates every form of noise known to mankind and several more which are not.

Switching power supplies work by chopping their input with varying mark/space ratios at frequencies which generally lie between 3 and 200 kHz and then using quite small inductors or transformers to transform to the final output voltage. The faster the switching can be accomplished, the higher the efficiency - but the more harmonics will be produced. Switching supplies produce noise over a broad band of frequencies - and it occurs as conducted noise, radiated noise, and electric and magnetic fields.

SWITCHING MODE POWER SUPPLIES

- **Generate every imaginable type of noise and some inconceivable ones as well**
- **DO NOT USE THEM WHERE NOISE IS IMPORTANT**
- **If their use is unavoidable do not relax and enjoy it, but take extreme precautions against all forms of noise**
- **Remember that a manufacturer's design change in a bought-in switching mode power supply may alter its effects on your system noise without altering its published specification.**
- **When developing a system using a switching mode supply it is instructive and often frightening to temporarily replace the switching supply with a battery or a linear supply and to remeasure the system noise!**

Figure 11.69

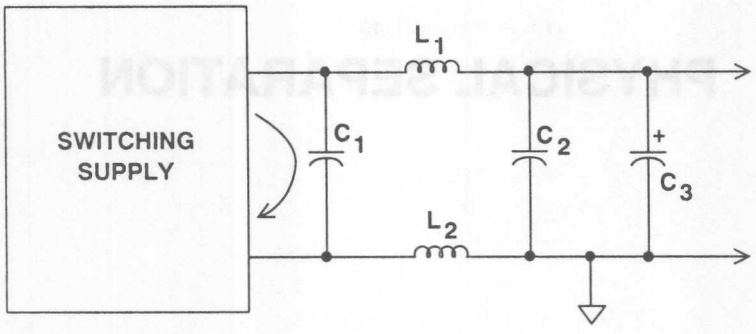
More practical, though, is to take extreme precautions when using a switching supply, and to recognize that in a very low noise system it may be better to use a less efficient linear supply. It is always wise, when designing a system using a switching supply, to measure the system noise, and then to remove the switching supply and, temporarily, replace it with a battery and measure the noise again. The results of such an experiment are always instructive and may be startling!

The conducted noise on a switching supply is dealt with by filtering. Remember that the capacitive reactance is only approximately true of an electrolytic capacitor at high frequencies because of the inductance of its structure, and that both electrolytic and ceramic capacitors and, probably, a choke (inductor) or two will be necessary to give an adequately low level of noise on the output of a switching supply.

The manufacturer will often include a filter which is adequate for supplies for digital systems, but for precision analog and, especially, for mixed signal sampled data systems further filtering should be taken for granted.

Switching supplies generate HF electric and magnetic fields (they generate electromagnetic fields as well, but these can generally be ignored). The electric fields are easily suppressed by a *grounded* Faraday shield (screen) , the HF magnetic fields, but not LF ones, will also be attenuated by such a shield (see comments earlier in this section on magnetic shielding), and both will cause fewer problems if the supply is physically located as far as possible from sensitive circuitry.

DECOUPLING A SWITCHING SUPPLY



- C_1 MUST HAVE LOW INDUCTANCE AND BE CLOSE TO THE SUPPLY TO MINIMIZE HF CURRENT LOOPS AND RESULTANT HF MAGNETIC FIELDS
- C_2 IS ALSO LOW INDUCTANCE, C_3 IS ELECTROLYTIC
- IF THE SWITCHING SUPPLY IS INTERNALLY GROUNDED, L_2 SHOULD BE OMITTED

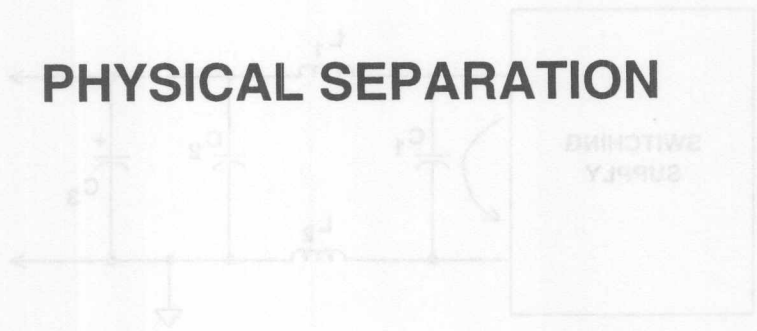
Figure 11.70

MINIMIZING THE EFFECTS OF SWITCHING POWER SUPPLY ELECTRIC AND MAGNETIC FIELDS

- SHIELD THEM AND LOCATE THEM WELL AWAY FROM SENSITIVE CIRCUITRY
- THIS IS A GENERAL PRINCIPLE
- Electromagnetic radiation is not usually too bad

Figure 11.71

PHYSICAL SEPARATION



MINIMIZES NOISE

Figure 11.72

This is really the global solution. It is bad practice to place switching supplies too close to sensitive circuitry - the design of the supply may change, without changing its data sheet specifications, and the external electric and magnetic fields may be completely altered. If the supply is located close to a sensitive circuitry its performance may be devastated - if it is further away problems will be minimized.

NOISE REDUCTION BY SEPARATION

The idea of minimizing external noise by physical separation does not apply only to switching supplies. Wherever noise from one circuit corrupts another, physical separation will reduce the effect. This separation can be by means of a shield, as discussed earlier, or it can be by sheer physical distance.

Modern electronic layout is costed to encourage minimal PCB area and components are placed as close together as possible. This may save money, but if it degrades the performance of circuits it is poor economy. It is often worthwhile to use separations of 4-10 mm of unpopulated board between potentially interfering parts of a system. This will allow a "moat" or "guard ring" of grounded copper to act as a shield between the parts. Production managers will howl about "wasted space" but the improvement in performance often justifies the cost.

MEASURING EXTERNAL NOISE

When a system is troubled with external noise it is often helpful to be able to measure the noise at various points in ground. It is rarely possible to do this with a simple oscilloscope probe but an instrumentation amplifier simplifies the job enormously.

If an instrumentation amplifier is set to a gain of 1000 and drives an oscilloscope with a sensitivity of 5 mV/cm then the sensitivity from its input to the oscilloscope will be 5 μV/cm. It will also have a common-mode rejection of over 100 dB and is thus ideal for measuring ground noise in PCBs and elsewhere.

There are two caveats: the external ground pin of the circuit board must be connected to the reference pin of the in-amp, the ground of the in-amp supply, and the ground of the oscilloscope in order to allow bias current to flow in the in-amp inputs, and, since if changing magnetic fields are present they can induce e.m.f.s in the loop formed by the input leads, giving spurious readings, their presence should be checked by shorting the probes to the board to provide bias current and moving their leads about and seeing if an AC signal, due to magnetic coupling, is detected.

This simple test system is extremely useful. Analog Devices once supplied their sales force with test boxes containing an instrumentation amplifier and batteries for performing this test. It was intended that they should lend them to customers who had ground noise problems. Within three months some 500 of these test boxes had been appropriated by customers who found them too useful to return![9]

GROUND NOISE DOWN TO 5μV FROM DC TO 50 kHz MAY BE MEASURED WITH AN OSCILLOSCOPE AND AN INSTRUMENTATION AMPLIFIER

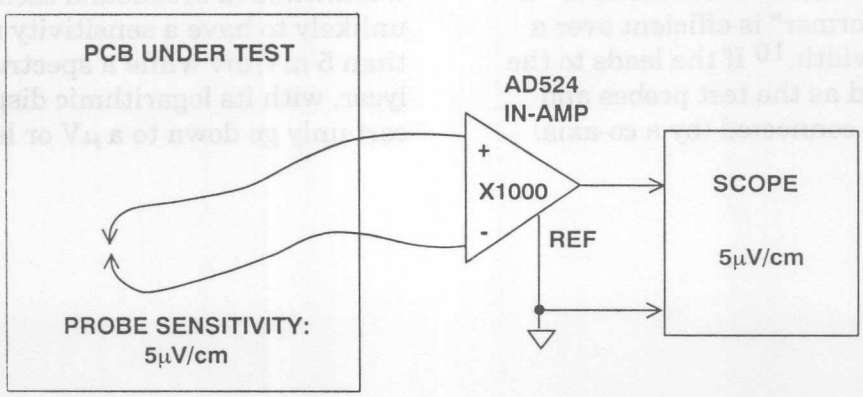


Figure 11.73

GROUND NOISE DOWN TO 0.5μV FROM 0.5 TO 500 MHz (OR MORE) MAY BE MEASURED WITH A BROADBAND TRANSFORMER AND A SPECTRUM ANALYZER

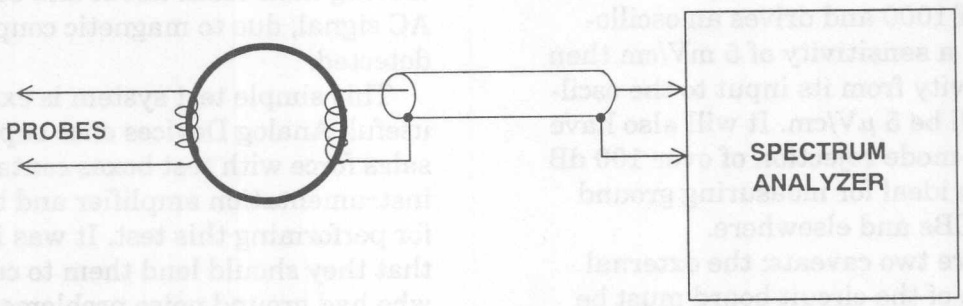


Figure 11.74

Many in-amps have a bandwidth of DC to 50 KHz. At higher frequencies there is another technique for ground noise measurement - a broadband transformer. Two lengths of enamelled copper wire are twisted together and the resulting twisted pair wound on a ferrite toroidal core, and one wire used as the primary and the other as the secondary of a transformer. Such a "transmission line transformer" or "Ruthroff transformer" is efficient over a very wide bandwidth.[10] If the leads to the primary are used as the test probes and the secondary is connected (by a co-axial cable) to the input of a broadband spectrum analyzer the system will measure ground noise down to a few microvolts from a few hundred KHz to over 1 GHz. The display, of course, will be in the frequency domain, rather than the time domain display of an oscilloscope, but this is quite easily interpreted and the additional 60-70 dB of dynamic range is worthwhile (a broadband oscilloscope is unlikely to have a sensitivity much better than 5 mV/div while a spectrum analyzer, with its logarithmic display, will certainly go down to a μV or less).

CONCLUSION

Noise has a reputation as a subject that is more black art than science. In fact the subject is quite simple - but extensive. Noise can come at you from all directions and it is important to consider all the possibilities, since Murphy's Law says that the one you don't consider is the cause of the problem.

This section of our seminar has attempted to lay the groundwork of noise in amplifier circuits, both the internal noise of the circuits and components and the external noise or interference. If all the sources are considered and suitable tests are performed it is usually comparatively easy to determine the source or sources of the noise and error in a system. If the source is understood the cure is much more easily accomplished.

If we must summarize the message of this section in a sentence, it is

THOUGHT BEFORE ACTION[11]

THOUGHT BEFORE ACTION

Figure 11.75

NOTES

1 All resistors have this noise, which is fundamental. It is possible to reduce it by reducing the temperature (but, being a square root law, quite low temperatures produce comparatively little improvement), the bandwidth or the resistance. It is not possible to reduce Boltzmann's Constant as he is dead, having committed suicide in Vienna in 1906.

2 For much more detail on this topic see "The Integrated Circuit Amplifier User's Guide to Grounding, Decoupling, and Making Things go Right for a Change" by A. Paul Brokaw (Analog Devices Application Note).

3For more detailed analysis of these two examples consult "Linear Design Seminar" Notes, Chapter 1. Available from Analog Devices.

4 For more detailed discussion of PCB layout issues see "Mixed Signal Seminar" Notes, Section XI. Available from Analog Devices.

5 But see the "Mixed Signal Seminar" Notes, pp XI-39 to XI-42 for more detailed discussion of problems with ground planes.

6 These lids are not ungrounded through the whim or malice of the analog IC manufacturer, but because the *package* manufacturer will only supply such packages with the lid connected to a corner pin, and analog ICs may not be able to use corner pins as ground.

7 See "Linear Design Seminar" Notes, Chapter 10, and "Mixed Signal Seminar" Notes, Section XI. Both available from Analog Devices.

8 Several manufacturers of optical remote control ICs manufacture transparent packages (sometimes packages transparent to infra-red only) containing a photocell and its associated amplifier on a single silicon chip. Such circuits are a special case.

9Although the boxes are no longer available (they've all been stolen) the data sheet on the box, which describes how it is made and used, is still available from Analog Devices Applications Department.

10 C. L. Ruthroff, "Some Broadband Transformers," **Proc. I.R.E.**, Vol 47, pp.1337-1342, August, 1959.

11 The full quotation comes from "The Edge" by Dick Francis and is "Thought before action - if there's time." In the analysis of noise in electronic circuits there is usually time.

ANALOG DEVICES

APPLICATION NOTE

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An I.C. Amplifier Users' Guide To Decoupling, Grounding, And Making Things Go Right For A Change

by Paul Brokaw

"There once was a breathy baboon
Who always breathed down a bassoon,
For he said "It appears
that in billions of years
I shall certainly hit on a tune"
(Sir Arthur Eddington)

This quotation seemed a proper note with which to begin on a subject which has made monkeys of most of us at one time or another. The struggle to find a suitable configuration for system power, ground, and signal returns too frequently degenerates into a frustrating glitch hunt. While a strictly experimental approach can be used to solve simple problems, a little forethought can often prevent serious problems and provide a plan of attack if some judicious tinkering is later required.

The subject is so fragmented that a completely general treatment is too difficult for me to tackle. Therefore, I'd like to state one general principle and then look a bit more narrowly at the subject of decoupling and grounding as it relates to integrated circuit amplifiers.

. . . Principle: Think—where the currents will flow.

I suppose this seems pretty obvious, but all of us tend to think of the currents we're interested in as flowing "out" of some place and "through" some other place but often neglect to worry how the current will find its way back to its source. One tends to act as if all "ground" or "supply voltage" points are equivalent and neglect (for as long as possible) the fact that they are parts of a network of conductors through which currents flow and develop finite voltages.

In order to do some advance planning it's important to consider where the currents originate and to where they will return and to determine the effects of the resulting voltage drops. This in turn requires some minimum amount of understanding of what goes on inside the circuits being decoupled and grounded. This information may be lacking or difficult to interpret when integrated circuits are part of the design.

Operational amplifiers are one of the most widely used linear I.C.'s, and fortunately most of them fall into a few classes, so far as the problems of power and grounding are concerned. Although the configuration of a system may pose formidable problems of decoupling and signal returns, some basic methods to handle many of these problems can be developed from a look at op-amps.

OP AMPS HAVE FOUR TERMINALS:

A casual look through almost any operational amplifier text might leave the reader with the impression that an ideal op-amp has three terminals: a pair of differential inputs and an output as shown in Figure 1. A quick review of fundamentals, however, shows that this can't be the case. If the amplifier has an output voltage it must be measured with respect to some point . . . a point to which the amplifier has a reference. Since the ideal op-amp has infinite common mode rejection, the inputs are ruled out as that reference so that there must be a fourth amplifier terminal. Another way of looking at it is that if the amplifier is to supply output current to a load, that current must get into the amplifier somewhere. Ideally, no input current flows, so again the conclusion is that a fourth terminal is required.

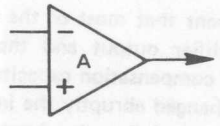


Figure 1. Conventional "Three Terminal" Op Amp

A common practice is to say, or indicate in a diagram, that this fourth terminal is "ground." Well, without getting into a discussion of what "ground" may be we can observe that most integrated circuit op-amps (and a lot of the modular ones as well) don't have a "ground" terminal. With these circuits the fourth terminal is one or both of the power supply terminals. There's a temptation here to lump together both supply voltages with the ubiquitous ground. And, to the extent that the supply lines really do present a low impedance at all frequencies within the amplifier bandwidth, this is probably reasonable. When the impedance requirement isn't satisfied, however, the door is left open to a variety of problems including noise, poor transient response, and oscillation.

DIFFERENTIAL TO SINGLE-ENDED CONVERSION:

One fundamental requirement of a simple op-amp is that an applied signal which is fully differential at the input must be converted to a single-ended output. Single ended, that is, with respect to the often neglected fourth terminal. To see how this can lead to difficulties, take a look at Figure 2.

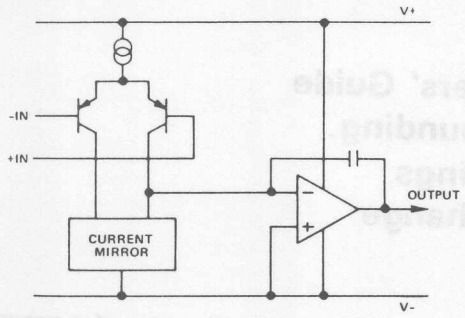


Figure 2. Simplifited "Real" Op Amp

The signal flow illustrated by Figure 2 is used in several popular integrated circuit families. Details vary, but, the basic signal path is the same as the 101, 741, TLO72, LF411,712, 515, and other integrated circuit amplifiers. The circuit first transforms a differential input voltage into a differential current. This input stage function is represented by PNP transistors in Figure 2. The current is then converted from differential to single-ended form by a current mirror which is connected to the negative supply rail. The output from the current mirror drives a voltage amplifier and power output stage which is connected as an integrator. The integrator controls the open-loop frequency response, and its capacitor may be added externally, as in the 101, or may be self-contained, as in the 741. Most descriptions of this simplified model don't emphasize that the integrator has, of course, a differential input. It's biased positive by a couple of base emitter voltages, but, the non-inverting integrator input is referred to the negative supply.

It should be apparent that most of the voltage difference between the amplifier output and the negative supply appears across the compensation capacitor. If the negative supply voltage is changed abruptly the integrator amplifier will *force* the output to follow the change. When the entire amplifier is in a closed loop configuration the resulting error signal at its input will tend to restore the output, but, the recovery will be limited by the slew rate of the amplifier. As a result, an amplifier of this type may have outstanding low frequency power supply rejection, but, the negative supply rejection is fundamentally limited at high frequencies. Since it is the feedback signal to the input that causes the output to be restored, the negative supply rejection will approach zero for signals at frequencies above the *closed loop* bandwidth. This means that high-speed, high-level circuits can "talk to" low-level circuits through the common impedance of the negative supply line.

Note that the problem with these amplifiers is associated with the negative supply terminal. Positive supply rejection may also deteriorate with increasing frequency, but, the effect is less severe. Typically, small transients on the positive supply have only a minor effect on the signal output. The difference between these sensitivities can result in an apparent asymmetry in the amplifier transient response. If the amplifier is driven to produce a positive voltage swing across its rated load it will draw a current pulse from the positive supply. The pulse may result in a supply voltage transient, but, the positive supply rejection will minimize the effect on the amplifier output signal. In the opposite case, a negative output signal will extract a current from the negative supply. If this pulse results in a "glitch" on the bus, the poor negative supply rejection will result in a similar "glitch" at the amplifier output. While a positive pulse test may give the amplifier transient response, a negative pulse test may actually give you a pretty good look at your negative supply line transient response, instead of the amplifier response!

Remember that the impulse response of the power supply itself is not what is likely to appear at the amplifier. Thirty or forty centimeters of wire can act like a high Q inductor to add a high-frequency component to the normally overdamped supply response. A decoupling capacitor near the amplifier won't always cure the problem either, since the supply must be decoupled *to* somewhere. If the decoupled current flows through a long path, it can still produce an undesirable glitch.

Figure 3 illustrates three possible configurations for negative supply decoupling. In 3a the dotted line shows the negative signal current path through the decoupling and along the ground line. If the load "ground" and decoupled "ground" actually join at the power supply the "glitch" on the ground lines is similar to the "glitch" on the negative supply bus. Depending upon how the feedback and signal sources are "grounded" the effective disturbance *caused* by the decoupling capacitor may be larger than the disturbance which it was intended to prevent. Figure 3b shows how the decoupling capacitor can be used to minimize disturbance of V– and ground busses. The high-frequency component of the load current is confined to a loop which doesn't include any part of the ground path. If the capacitor is of sufficient size and quality, it will minimize the glitch on the negative supply without disturbing input or output signal paths. When the load situation is more complex, as in 3c, a little more thought is required. If the amplifier is driving a load that goes to a virtual ground, the actual load current does not return to ground. Rather, it must be supplied by the amplifier creating the virtual ground as shown in the figure. In this case, decoupling the negative supply of the first amplifier to the positive supply of the second amplifier closes the fast signal current loop without disturbing ground or signal paths. Of course, it's still important to provide a low impedance path from "ground" to V– for the second amplifier to avoid disturbing the input reference.

The key to understanding decoupling circuits is to note where the actual load and signal currents will flow. The key to optimizing the circuit is to bypass these currents around ground and other signal paths. Note, that as in figure 3a, "single point grounding" may be an oversimplified solution to a complex problem.

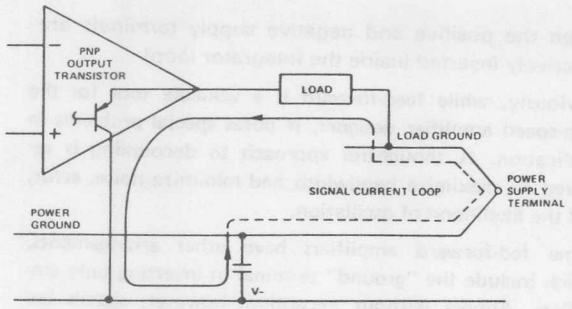


Figure 3a. Decoupling for Negative Supply Ineffective

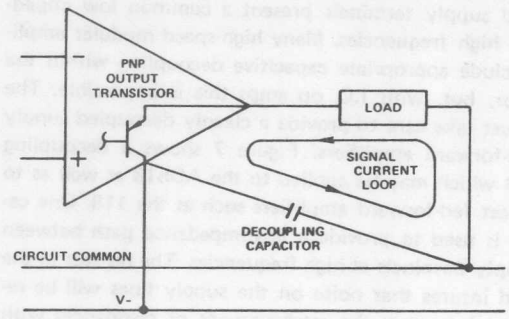


Figure 3b. Decoupling Negative Supply Optimized for "Grounded" Load

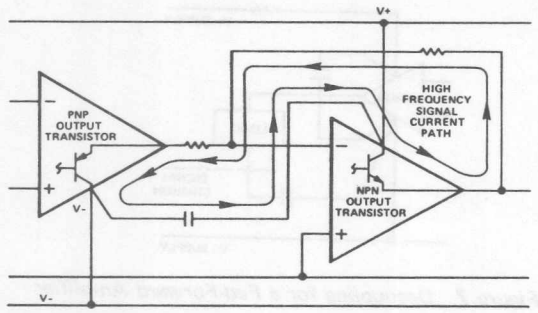


Figure 3c. Decoupling Negative Supply Optimized for "Virtual Ground" Load

Figure 3b and 3c have been simplified for illustrative purposes. When an entire circuit is considered conflicts frequently arise. For example, several amplifiers may be powered from the same supply, and an individual decoupling capacitor is required for each. In a gross sense the decoupling capacitors are all paralleled. In fact, however, the inductance of the interconnecting power and ground lines convert this harmless-looking arrangement into a complex L-C network that often rings like the "Avon Lady". In circuits handling fast signal wavefronts, decoupling networks paralleled by more than a few centimeters of wire generally mean trouble. Figure 4 shows how small resistors can be added to lower the Q of the undesired resonant circuits. The resistors can generally be tolerated since they convert a bad high-frequency jingle to a small damped signal at the op amp supply terminal. The residual has larger *low frequency* components, but, these can be handled by the op-amp supply rejection.

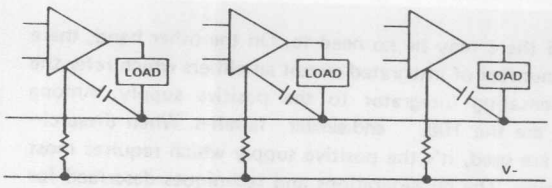


Figure 4. Damping Parallel Decoupling Resonances

FREQUENCY STABILITY:

There's a temptation to forget about decoupling the negative supply when the system is intended to handle only low-frequency signals. Granted that decoupling may not be required to handle low-frequency signals, but it may still be required for frequency stability of the op-amps.

Figure 5 is a more-detailed version of Figure 2 showing the output stage of the I.C. separated from the integrator (since this is the usual arrangement) and showing the negative power supply and wiring impedance lumped together as a single constant. The amplifier is connected as a unity gain follower. This makes a closed-loop path from the amplifier output through the differential input to the integrator input. There is a second feedback path from the collector of the output PNP transistor back to the other integrator input. The net input to the integrator is the difference of the signals through these two paths. At low frequencies this is a net, negative feedback. The high-frequency feedback depends upon both the load reactance and the reactance of the V– supply.

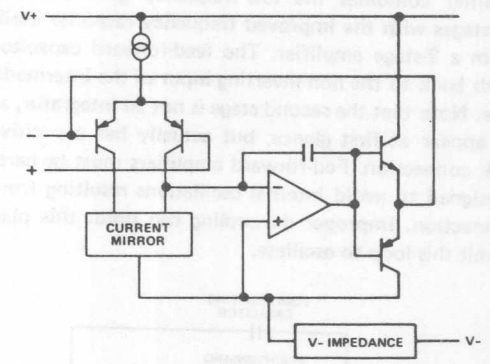


Figure 5. Instability Can Result from Neglecting Decoupling

When the supply lead reactance is inductive, it tends to destabilize the integrator. This situation is aggravated by a capacitive load on the amplifier. Although it's difficult to predict under exactly what circumstances the circuit will become unstable, it's generally wise to decouple the negative supply if there is any substantial lead inductance in the V– lead *or* in the common return to the load and amplifier input signal source. If the decoupling is to be effective, of course, it must be with respect to the *actual* signal returns, rather than to some vague "ground" connection.

POSITIVE SUPPLY DECOUPLING:

Up to this point we haven't considered decoupling the positive supply line, and with amplifiers typified by Figures 2

and 5 there may be no need to. On the other hand, there are a number of integrated circuit amplifiers which refer the compensating integrator to the positive supply. Among these are the 108, and similar families. When these circuits are used, it's the positive supply which requires most attention. The considerations and techniques described for the class of circuits shown in Figure 2 apply equally to this second class, but, should be applied to the positive supply rather than the negative.

FEED-FORWARD:

A technique which is most frequently used to improve bandwidth is called feed-forward. Generally, feed-forward is used to bypass an amplifier or level translator stage which has poor high frequency response. Figure 6 illustrates how this may be done. Each of the amplifiers shown is really a subcircuit, usually a single stage, in the overall amplifier. In the illustration, the input stage converts the differential input to a single-ended signal. The signal drives an intermediate stage (which in practice often includes level translator circuitry) which has low-frequency gain, but, limited bandwidth. The output of this stage drives an integrator-amplifier and output stage. The overall compensation capacitor feeds back to the input of the second stage and includes it in the integrator loop. The compromises necessary to obtain gain and level translation in the intermediate stage often limit its bandwidth and slow down the available integrator response. A feed-forward capacitor permits high-frequency signals to bypass this stage. As a result, the overall amplifier combines the low-frequency gain available from 3 stages with the improved frequency response available from a 2-stage amplifier. The feed-forward capacitor also feeds back to the non-inverting input of the intermediate stage. Note that the second stage is not an integrator, as it may appear at first glance, but actually has a positive feedback connection. Fed-forward amplifiers must be carefully designed to avoid internal oscillations resulting from this connection. Improper decoupling can upset this plan and permit this loop to oscillate.

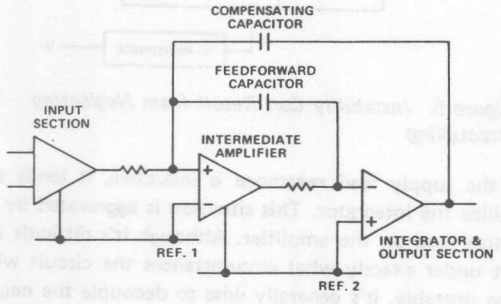


Figure 6. Fast Fed-Forward Amplifier

Note that the internal input stages are shown as being referred to separated reference points, Ideally, these will be the same reference so far as signals are concerned, although they may differ in bias level. In practice this may not be the case. Examples of fed-forward amplifiers are the AD518 and the AD707. In these amplifiers, signal Reference 1 is the positive supply, while signal Reference 2 is the negative supply. Signals appearing between the positive and negative supply terminals are effectively inserted inside the integrator loop!

Obviously, while feed-forward is a valuable tool for the high-speed amplifier designer, it poses special problems in application. A thoughtful approach to decoupling is required to maximize bandwidth and minimize noise, error, and the likelihood of oscillation.

Some fed-forward amplifiers have other arrangements, which include the "ground" terminal in inverting only amplifiers. Almost without exception, however, signals between some combination of the supply terminals get "inside" the amplifier. It is vital to proper operation that the involved supply terminals present a common low impedance at high frequencies. Many high-speed modular amplifiers include appropriate capacitive decoupling within the amplifier, but, with I.C. op amps this is impossible. The user must take care to provide a cleanly decoupled supply for fed-forward amplifiers. Figure 7 shows a decoupling method which may be applied to the AD518 as well as to other fast fed-forward amplifiers such as the 118. One capacitor is used to provide a low-impedance path between the supply terminals at high frequencies. The resistor in the V+ lead insures that noise on the supply lines will be rejected *and* prevents the establishment of resonances with other decoupling circuits. The second capacitor decouples the low side of the integrator to the load.

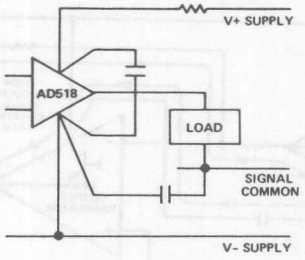


Figure 7. Decoupling for a Fed-Forward Amplifier

Alternatives include a resistor in both supply leads and/or decoupling from V+ to the load. In principle, the positive and negative supply should be tied in a "tight knot" with the signal return. To the extent that this cannot be done, there is a slight advantage to favoring the negative supply due to the high frequency limitations of PNP transistors used in junction-isolated I.C.'s.

OTHER COMPENSATION:

While most integrated circuit amplifiers use one of the three compensation schemes already described, a significant fraction use some other plan. The 725 type amplifiers combine a V– referred integrator with a network which the manufacturers recommend to be connected from signal ground to the integrator input. This makes the circuit extremely liable to pick up noise between V– and ground. In many circumstances it may be wiser to connect the external compensation to the negative supply, rather than to signal ground.

One more class of amplifiers is typified by the Analog Devices AD829 and AD847 . In these circuits, a single capaci-

tor may be used to induce a dominant pole of response without resorting to an integrator connection. The high-frequency response of the amplifier will appear with respect to the "ground" end of the compensation capacitor. In these amplifiers a small internal capacitance is connected between V+ and the compensation point. Unity gain compensation can be added in parallel and the pin-out is arranged to make this simple. The free end of the compensation capacitor can also be connected either to V– or signal common. It is extremely important that the signal common and the compensation connect directly or through a low-impedance decoupling.

Although the main signal path of these amplifiers can be compensated in a variety of ways, some care is required to insure the stability of internal structures. It's always wise to use extra care in decoupling wideband amplifiers to avoid problems with the output stage and other subcircuits which are similar to the main integrator problem illustrated by Figure 5. An effective compensation and decoupling circuit for the AD509 is shown in Figure 8. This arrangement is similar to Figure 7, and one of these two circuits is likely to be suitable for many types of wideband amplifier. Depending upon the power distribution, a small (10Ω to 50Ω) resistor may be appropriate in both of the supply leads to reduce power lead resonance and interference both to and from circuits sharing the power supply.

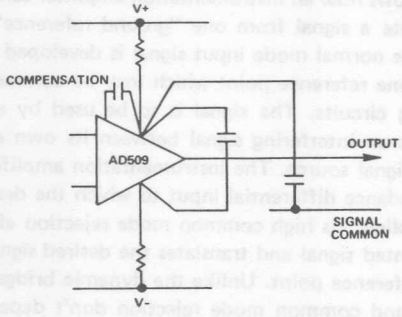


Figure 8. - Decoupling a Wideband Amplifier

GROUNDING ERRORS:

Ground in most electronic equipment is not an actual connection to earth ground, but a common connection to which signals and power are referred. It is frequently immaterial to the function of the equipment whether or not the point actually connects to earth ground. I myself prefer some distinguishing name or names for these common points to emphasize that they must be *made* common. The term "ground" too often seems to be associated with a sort of cure-all concept, like snake oil, money or motherhood. If you're one of those who regards ground with the same sort of irrational reverence that you hold for your mother, remember that while you can always trust your mother, you should *never* trust your "ground." Examine and think about it.

It's important to have a look at the currents which flow in the ground circuit. Allowing these currents to share a path with a low-level signal may result in trouble. Figure 9 illustrates how careless grounding can degrade the performance of a simple amplifier. The amplifier drives a load which is represented by the load resistor. The load current comes from the power supply and is controlled by the amplifier as it amplifies the input signal. This current must return to the supply by some path; suppose that points A and B are alternative power supply "ground" connections. Assuming that the figure represents the proper topology or ordering of connections along the "ground" bus, connecting the supply at A will cause the load current to share a segment of wire with the input signal connection. Fifteen centimeters of number 22 wire in this path will present about 8 milliohms of resistance to the load current. With a 2k load, a 10-volt output signal will result in about 40 microvolts between the points marked "ΔV." This signal acts in series with the non-inverting input and can result in significant errors. For example, the typical gain of an AD707 amplifier is 8 million so that only 1¼μV of input signal is required to produce a 10 volt output. The 40μV ground error signal will result in a 32 times increase in the circuit gain error! This degradation could easily be the most serious error in a high-gain precision application. Moreover, the error represents positive feedback so that the circuit will latch up or oscillate for large closed-loop gains with R_f/R_i greater than about 250k.

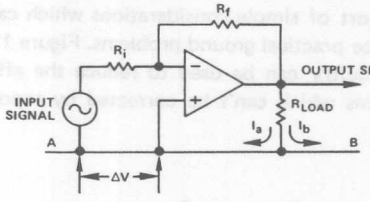


Figure 9. Proper Choice of Power Connections Minimizes Problems

Reconnecting the power supply to point B will correct the problem by eliminating the common impedance feedback connection. In a real system, the problem may be more complex. The input signal source, which is represented as floating in Figure 9, may also produce a current which must return to the power supply. With the supply at point B, any current which flows in additional loads (other than R_i) may interfere with the operation of the amplifier shown. Figure 10 illustrates how amplifiers can be cascaded and still drive auxiliary loads without common impedance coupling. The

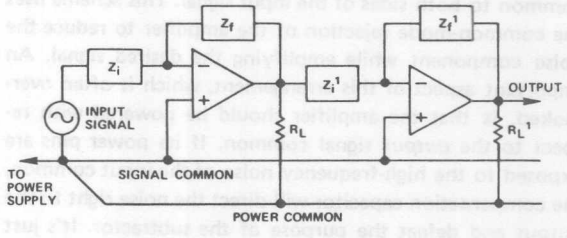


Figure 10. Minimizing Common Impedance Coupling

output currents flow through the auxiliary loads and back to the power supply through power common. The currents in the input and feedback resistors are supplied from

11

the power supply by way of the amplifiers as previously illustrated in Figure 3c. The only current flowing in signal common is the amplifier's input current, and its effect is generally negligibly small.

Having given an example of a simple "grounding error" and its solution, I will now get back on my soap box and say that grounding errors result from neglect based on the assumption that a ground, is a ground, is a ground. *Some* impedance will be present in any interconnection path, and its effect should be considered in the overall design of a system. Quantitative approaches are quite useful in specialized applications. In fast TTL and ECL logic circuitry the characteristic impedance of interconnections is controlled so that proper terminations can reduce problems. In RF circuitry the unavoidable impedances are taken into account and incorporated into the design of the circuit. With op-amp circuitry, however, impedance levels do not lend themselves to transmission line theory, and the power and ground impedances are difficult to control or analyze. The most expedient procedure, short of difficult and restrictive quantitative analysis, seems to be to arrange the unavoidable impedances so as to minimize their effects and arrange the circuitry to overcome the effects. Figures 9 and 10 illustrate the sort of simple considerations which can substantially reduce practical ground problems. Figure 11 illustrates how circuitry can be used to reduce the effect of ground problems which can't be corrected by topological tricks.

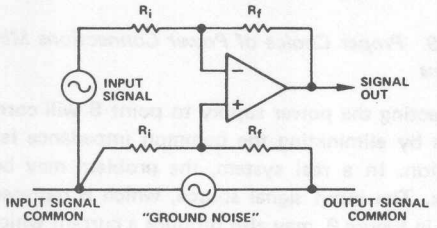


Figure 11. Subtractor Amplifier Rejects Common Mode Noise

GETTING AROUND THE PROBLEM:

In Figure 11 a subtractor circuit is used to amplify a normal mode input signal and reject a ground noise signal which is common to both sides of the input signal. This scheme uses the common-mode rejection of the amplifier to reduce the noise component while amplifying the desired signal. An important aspect of this arrangement, which is often overlooked, is that the amplifier should be powered with respect to the *output* signal common. If its power pins are exposed to the high-frequency noise of the input common, the compensation capacitor will direct the noise right to the output and defeat the purpose of the subtractor. It's just this kind of effect which makes it important to use care in grounding and decoupling. A subtractor or dynamic bridge, like Figure 11, will be ineffective in correcting a grounding problem if the amplifier itself is carelessly decoupled. In general, an op-amp should be decoupled to the point which is the reference for measuring or using its output signal. In "single-ended" systems it should also be decoupled to the input signal return as well. When it is impossible to satisfy both these requirements at once, there's a high probability of either a noise or oscillation problem or both. Frequently the difficulty can be resolved with a subtractor, like Figure 11, where a network like the single-ended feedback network (which needn't be all resistive) joins the input and output signal reference points and provides a "clean" reference point for the non-inverting input of the amplifier.

A problem with the subtractor is that it uses a balanced bridge to reject the common mode signal between the input and output reference points. The arms of the network must be carefully balanced, since to the extent they don't match, the unwanted signal will be amplified. Although even a poorly matched network will probably eliminate oscillation problems, noise rejection will suffer in direct proportion to any mismatches. An easier way to reject large "ground noise" signals is to use a true instrumentation amplifier.

INSTRUMENTATION AMPLIFIERS:

A true instrumentation amplifier has a very visible "fourth terminal." The output signal is developed with respect to a well defined reference point which is usually a "free" terminal that may be tied to the output signal common. The instrumentation amplifier also differs from an op amp in that the gain is fixed and well defined, but there is no feedback network coupling input and output circuits. Figure 12 shows how an instrumentation amplifier can be used to translate a signal from one "ground reference" to another. The normal mode input signal is developed with respect to one reference point which may be common to its generating circuits. The signal is to be used by a system which has an interfering signal between its own common and the signal source. The instrumentation amplifier has a high impedance differential input to which the desired signal is applied. Its high common mode rejection eliminates the unwanted signal and translates the desired signal to the output reference point. Unlike the dynamic bridge circuit, the gain and common mode rejection don't depend on a network connecting the input and output circuits. The gain is set, in Figure 12, by the ratio of a pair of resistors which are connected inside the amplifier. The amplifier has a very high input impedance, so that gain and common mode rejection are not greatly affected by variations or unbalance in source impedance.

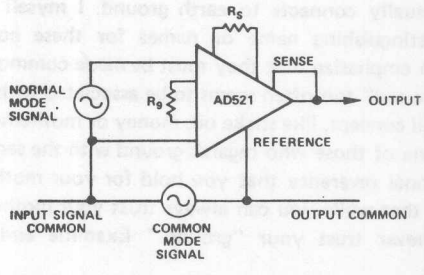


Figure 12. Applying an In-Amp

Since instrumentation amplifiers have a reference or "ground" terminal, they have the potential to be free of the power supply sensitivities of op amps. In practice, however, most instrumentation amplifiers have internal frequency

compensation which is referred to the power supply. In the case of the AD521, the compensation integrator is referred to the negative supply terminal. The decoupling of this terminal is particularly important, and it should be decoupled with respect to the output reference terminal, or actually to the point to which this terminal refers.

THE "OTHER" INPUT:

Most I.C. op-amps and in-amps include offset voltage nulling terminals. These terminals generally have a small voltage on them and by loading the terminals with a potentiometer the amplifier offset voltage can be adjusted. While their impedance level is much lower than the normal input, the null terminals can act as another differential input to the amplifier. Although the null terminals aren't generally looked at as inputs, most amplifiers are quite sensitive to signals applied here. For example, in 741 family amplifiers the output voltage gain from the null terminals is greater than the gain from the normal input!

An illustration of the type of problems that can arise with the "other" input is shown in Figure 13. The figure is an op-amp circuit with some of the offset null detail shown.

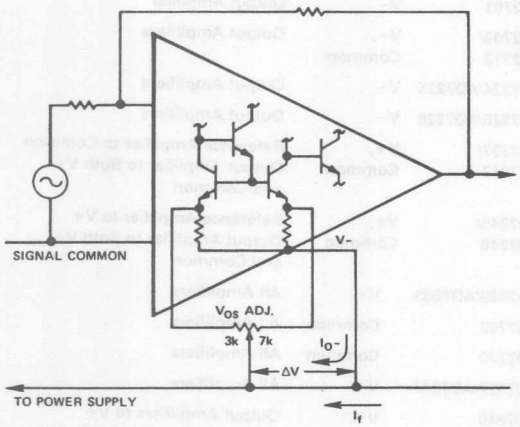


Figure 13. Details of V_{OS} Nulling – the "Other" Input

As it's drawn, the V_{OS} null pot wiper connects to a point along a V– "clothesline" which carries both the return current from the amplifier and currents from other circuits back to the power supply. These currents will develop a small voltage, ΔV, along the conductor between the amplifier V– terminal and the null pot wiper. If the null pot is set on center, the equal halves will form a balanced bridge with the resistors inside the amplifier. The effect of the voltage generated along the wire is balanced at the V_{OS} terminals and will have little effect on the amplifier output. On the other hand, if the null pot is unbalanced, to correct an amplifier offset, the bridge will no longer balance. In this case voltages developed along the "clothesline" will result in a difference voltage at the V_{OS} terminals. For instance, suppose that a 10k null pot balances out the op amp offset when it is set with 3k and 7k branches as shown in the figure. In a 741 the internal resistors are about 1k so that the difference signal at the V_{OS} terminals will be about 1/8 ΔV. The gain from these terminals is about twice the gain from the normal input, so that the disturbance acts as if it were an input signal of about 1/4 ΔV. Using the same assumptions as in the discussion of Figure 9. the current I_{O-} will result in a 10 microvolt input error signal. In this case, however, the error will appear *only* when the amplifier load current comes from the negative supply. When the load is driven positive the error will disappear. As a result, the V_{OS} input signal will result in distortion rather than a simple gain error!

An additional problem is created by I_f, a current returning to the power supply from other circuits. The current from other circuits is not generally related to the op amp signal, and the voltage developed by it will manifest itself as noise. This signal at the null terminals can easily be the dominant noise in the system. A few milliamps of V– current through a few centimeters of wire can result in interference which is orders of magnitude larger than the inherent input noise of the amplifier. The remedy is to make the connection from the null pot wiper direct to the V– pin of the amplifier, as shown in Figure 14. Some amplifiers such as the AD707 and AD840 refer to the null offset terminals to V+. Obviously, the pot wiper should go to the V+ terminal of this type of amplifier. It's important to connect the line directly to the op amp terminal so as to minimize the common impedance shared by the op amp current and the null pot connection.

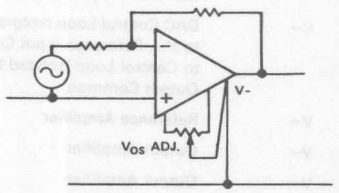


Figure 14. Connecting the Null Pot for Trouble Free Operation

The considerations for op-amp null pots also apply to the similar trimmers on almost all types of integrated circuits. For example, the AD521 In-Amp null terminals exhibit a gain of about 30 to the output. Although this is much less than in the case of most op-amps, it still warrants care in controlling the null pot wiper return. Table I lists the integrated circuits manufactured by Analog Devices, including some popular second-source families, and indicates how internal conversions from differential to single ended are referred. That is, the signals are made to appear with respect to the terminal(s) listed.

11

	Internal Integrator Referred to:	Comment
AD OP 07/ 27/37	V+, V−	Internal Feedforward Cap V+ to V− and Integrator V− to Output
AD380	V+	
AD390	V−	Output and Reference Amplifier
AD394/AD395	V−	Output Amplifiers
AD396	V−	Output Amplifiers
AD507	–	External Cap to Signal Common or V+
AD508	–	External Cap to Signal Common or V+
AD510	V+	
AD517	V+	
AD518	V+, V−	Internal Feedforward Cap V+ to V− and Integrator V− to Output
AD521	V−	Output Amplifier Integrator
AD524	V−	Output Amplifier Integrator
AD526	V−	Output Amplifier Integrator
AD532/AD533	V+	Multiplier Output Amplifier Integrator
AD534/AD535	V−	Output Amplifier
AD536A	V−, V+ Common	External Integrator to V+, Internal Feedforward V− to Common
AD538	V−	Internal Amplifiers
AD542/AD642	V−	
AD544/AD644	V−	
AD545A	V−	
AD546	V−	
AD547/AD647	V−	
AD548/AD648	V−	
AD549	V−	
AD557/AD558	Common	Output Amplifier and DAC Control Loop Integrator Referred to Common
AD561	V−, Common	DAC Control Loop Integrator and Ref. Amp Referred to Common and Ref. Bias Amplifier Referred to V−
AD565A/ AD566A	V−	DAC Control Loop Integrator Referred to V−. Reference Input Common to Control Loop Isolated from DAC Output Common
AD568	V+	Reference Amplifier
AD580	V−	Output Amplifier
AD581	V−	Output Amplifier
AD582	V−	Output Amplifier
AD584	V−	Output Amplifier
AD586/AD587	V−	Output Amplifier
AD588	V−	Output Amplifier
AD624/AD625	V−	Output Amplifier Integrator
AD636	V−, V+, Common	External Integrator to V+, Internal Feedforward V− to Common
AD637	V−, Common	Internal Feedforward V− to Common
AD645	V−	
AD650/AD652	V+	Internal Amplifier
AD662	Common	DAC Control Loop Integrator and Reference Amplifier Referred to Common
AD664	V−	Output Amplifiers
AD667	V−, Common	Output Amplifier Referred to V− and Reference Amplifier Referred to Common
AD668	V+	Reference Amplifier
AD688	V−	Output Amplifier
AD689	V−	Output Amplifier
AD704/AD705/ AD706	V+	
AD707/AD708	V+, V−	Internal Feedforward Cap V+ to V− and Integrator V− to Output
AD711/AD712/ AD713	V−	
AD736/ AD737	V−, Common	External Integrator to V− Internal Feedforward V− to Common
AD741	V−	
AD744/AD746	V−	
AD766	V−	Output and Reference Amplifier
AD767	V−, Common	Output Amplifier Referred to V− and Reference Amp Referred to Common
AD840/AD841/ AD842	V+, V−	
AD843	V+, V−	
AD844/AD846	V+, V−	
AD845	V+	
AD847/AD848/ AD849	V+, V−	
AD1856/AD1860	V−	Output and Reference Amplifier
AD1864	V−	Output and Reference Amplifier
AD2700/AD2710	Common	Output Amplifier
AD2701	V−	Output Amplifier
AD2702/ AD2712	V−, Common	Output Amplifiers
AD7224/AD7225	V−	Output Amplifiers
AD7226/AD7228	V−	Output Amplifiers
AD7237/ AD7247	V+, Common	Reference Amplifier to Common Output Amplifier to Both V+ and Common
AD7245/ AD7248	V+, Common	Reference Amplifier to V+ Output Amplifier to Both V+ and Common
AD7569/AD7669	V−	All Amplifiers
AD7769	Common	All Amplifiers
AD7770	Common	All Amplifiers
AD7837/AD7847	V+	All Amplifiers
AD7840	V+, Common	Output Amplifiers to V+ Reference Amplifier to Common
AD7845	V+	All Amplifiers
AD7846	V+	All Amplifiers
AD7848	V+, Common	Output Amplifier to V+ Reference Amplifier to Common

Table I.

This collection of examples won't solve all your potential grounding problems. I hope that it will give you some good ideas how to prevent some of them, and it should also give you some of the "inside story" on I.C.'s which you can put to work in very practical ways. There is no general grounding method which will prevent all possible problems. The only generally applicable rule is attention to detail, and remember that you can always trust your mother, but . . . .

SECTION XII
HARDWARE TECHNIQUES

- Leakage In Insulators:
  Guard Rings, Electrostatic Damage (ESD)

- Grounding and Signal Routing:
  Signal Return Currents, Ground Noise and Ground Loops, Star Grounds, Separate Analog and Digital Grounds, Ground Planes, Transmission Lines, System Grounds, Signal Routing

- Problem Areas:
  Limitations of Spice Modelling, Sockets, Prototyping

SECTION XII

HARDWARE TECHNIQUES

JAMES M. BRYANT

LEAKAGE IN INSULATORS

Just as conductors are improperly viewed as superconductors, so are insulators often mistakenly treated as perfect insulators, rather than very high resistances, which is the more accurate model.

Most printed circuit board materials are very good insulators, but they are not perfect, and inadequately cleaned PCB material may be quite a poor insulator. Furthermore, PCBs are anisotropic - even on a clean PCB different parts of the surface may have different resistivities, and the bulk resistance (between two plated through holes, for instance) is generally lower than the surface resistance between two tracks.

Since the insulation resistance is so variable (and it will vary further with temperature and humidity) it is hard to predict in any particular circumstances but it is safe to assume that it is unlikely that the resistance between two conductors on a clean PCB will drop below 10^{10} - 10^{11} ohms, and with teflon PCB material (which is very expensive) will usually be over 10^{12} ohms.

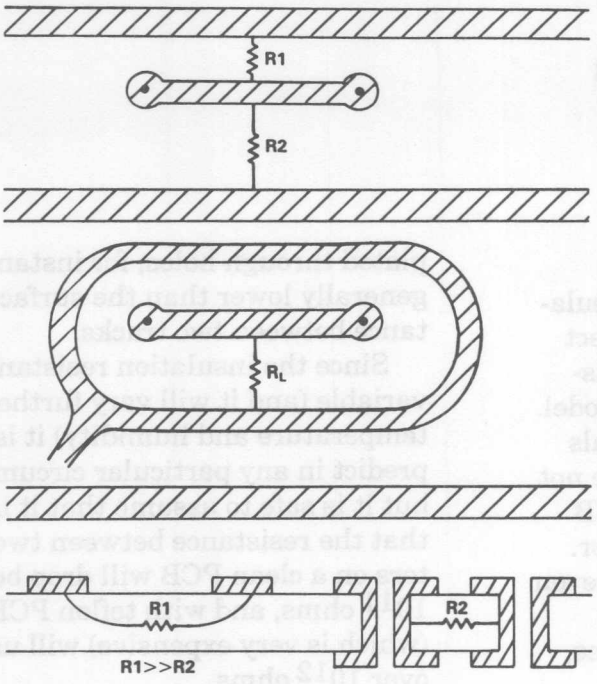
GUARD RINGS

In applications where high impedances and very low currents are involved a guard ring may be used to minimize the effects of low insulation resistance. If critical high impedance nodes are surrounded by a ring of conductor which is at (or very close to) the potential of the node itself then the leakage current at the node will be minimized. If the node is at, or near to, ground then a grounded guard ring will be appropriate, if it is at some other potential it may be necessary to use a high input impedance buffer amplifier, with its input connected to the node, to force the guard ring to the node potential. It is obvious that, in general, guard rings should be on both sides of the PCB with plated-through holes.

Nodes which are sufficiently sensitive to require guard rings should not contain plated through holes (unless the PCB is made of teflon) because, as mentioned above, the bulk resistivity of PCB material is less than the surface resistivity.

An alternative to the use of a guard ring is to use teflon stand-off insulator(s) to support the high impedance point(s). If virgin teflon is used insulation resistance of around 10^{15} ohms is possible ("Virgin teflon" is a solid piece of new teflon material which has been machined to shape and has not been welded together from powder or grains). The material of the rest of the circuit board need not have particularly high insulation resistance.

LEAKAGE RESISTANCE ON PCBs



SURFACE LEAKAGE ON A PCB IS UNPREDICTABLE. R1 IS NOT NECESSARILY LESS THAN R2

IF A VULNERABLE CONDUCTOR IS SURROUNDED BY A GUARD RING (ON BOTH SIDES OF THE BOARD) WHICH IS AT THE SAME POTENTIAL AS THE CONDUCTOR IT IS GUARDING THE EFFECTS OF LEAKAGE RESISTANCE WILL BE MINIMIZED

LEAKAGE RESISTANCE BETWEEN SURFACE TRACKS ON A PCB IS GENERALLY MUCH LARGER THAN BETWEEN PLATED HOLES

Figure 12.1

A VIRGIN TEFLON STANDOFF INSULATOR HAS MUCH LOWER LEAKAGE THAN A PCB TRACK

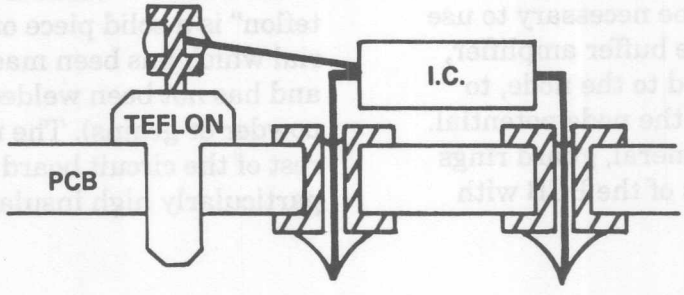


Figure 12.2

ELECTROSTATIC DAMAGE (ESD)

Where resistances are very high, especially in conditions of low humidity, there is always the possibility of electrostatic charge and electrostatic damage. A full discussion of electrostatic damage (ESD) and its prevention will be found in Analog Devices' Application Note on the subject, which is available free of charge from Analog Devices.[1]

This application note describes procedures to minimize the risk of electrostatic damage to sensitive devices. The basic principle of all ESD protection is to prevent a vulnerable item from being in the path of a discharge. Many of the precautions used in factories are designed to minimize the possibility of any damaging discharge, even in the event of carelessness. When experienced engineers handle ICs they may dispense with most of the ESD protection apparatus and merely ensure that the IC is never in any potential discharge path: when taking a circuit from conductive foam touch the foam to equalize charge before touching the circuit, similarly touch the foam with the hand before inserting the circuit in it, and hold your colleague's hand BEFORE passing the IC.

All integrated circuit structures are vulnerable to damage from the high voltages and high peak currents involved in even small electrostatic discharges but precision analog circuits suffer from a special disadvantage - the circuitry used to protect integrated circuit structures from ESD can often degrade the analog accuracy of the circuit where it is employed. Thus we have the choice between high performance and a high degree of protection. Which we choose will depend upon individual circumstances but it is essential to realize that the choice must be made - and if it is made in favour of accuracy then the circuit involved must not be exposed to electrostatic discharge.

A precision analog circuit exposed to ESD may not fail totally, but merely suffer degradation of its analog performance, and possible reduction of life expectancy. When an IC is returned to Analog Devices for failure analysis of inadequate performance the first check that is made when the package is opened is a visual inspection for evidence of electrostatic damage - and this is found in a large percentage of cases.

An interesting example of an unobvious effect of ESD occurred in Finland, where very cold winters produce very low humidity and particularly severe electrostatic problems. A customer complained that the AD549 low bias current BIFET op-amp had poor long-term reliability and that its noise performance deteriorated over a few years of use.

The amplifier was being used as a unity gain buffer with an electrochemical cell and the non-inverting input was connected to a platinum electrode and to nothing else. In use this electrode was immersed in electrolyte but after use it was washed (automatically) in deionized water and air dried. It was then left unconnected until the machine was next used.

Although there was no possibility of the electrode being touched at this time (it was in the very center of the machine) it could encounter random particles of electrostatically charged dust - and the pulse currents as these dust particles discharged were sufficient to cause gradual deterioration of the noise figure. As soon as arrangements were made to ground the electrode when it was not in use (with an NC reed relay for minimum leakage) the problem disappeared.

ELECTROSTATIC DISCHARGE (ESD)

ESD
PREVENTION MANUAL

ANALOG DEVICES

Figure 12.3

ELECTROSTATIC DISCHARGE PROTECTION

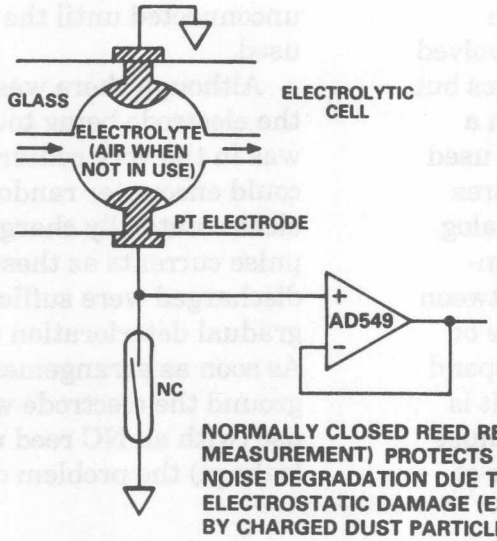


Figure 12.4

GROUNDING AND SIGNAL ROUTING

SIGNAL RETURN CURRENTS

Kirchoff's Law tells us that at any point in a circuit the algebraic sum of the currents is zero. This tells us that all currents flow in circles and, particularly, that the return current must always be considered when analyzing a circuit.

Most people consider the return current when considering a fully differential circuit, but when considering the more usual circuit where a signal is referred to "ground" it is common to assume that all the points on the circuit diagram where the ground symbol is to be found are at the same potential. This is unwise.

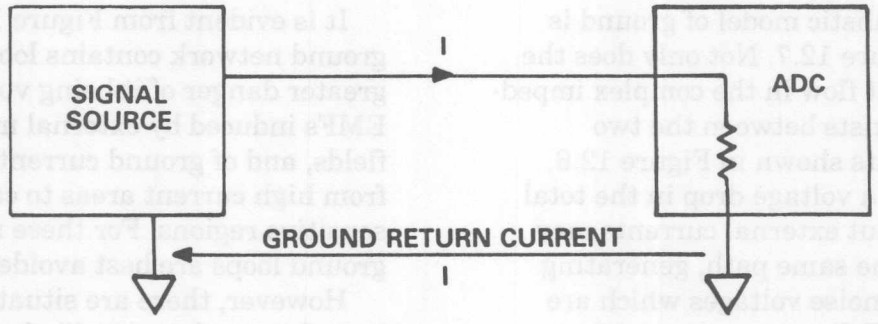


Figure 12.5

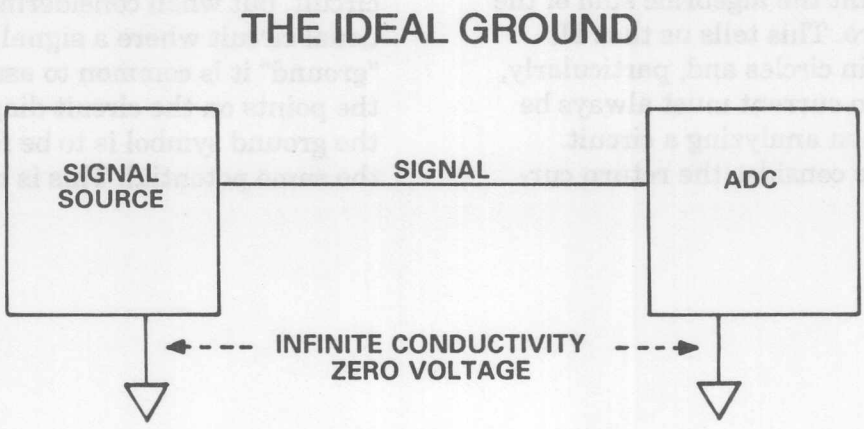


Figure 12.6

GROUND NOISE & GROUND LOOPS

A more realistic model of ground is shown in Figure 12.7. Not only does the return current flow in the complex impedance which exists between the two "ground" points shown in Figure 12.6, giving rise to a voltage drop in the total signal path, but external currents may also flow in the same path, generating uncorrelated noise voltages which are seen by the ADC.

It is evident, of course, that other currents can only flow in the ground impedance if there is a current path for them. Figure 12.7 shows such a path at "ground" potential, which is the notorious "Ground Loop", but equally severe problems could be caused by a circuit sharing an unlooped ground return with the signal source but drawing a large and varying current from its supply and ground return.

It is evident from Figure 12.9 that if a ground network contains loops there is a greater danger of it being vulnerable to EMFs induced by external magnetic fields, and of ground current "escaping" from high current areas to cause noise in sensitive regions. For these reasons ground loops are best avoided.

However, there are situations where looped grounds are unlikely to cause unacceptable noise and the configuration may actually offer benefits in the form of safety or reduced impedance. In such circumstances the optimum ground arrangement may contain loops. Sensible engineers should not allow the almost superstitious dread inspired by the term "ground loop" to prevent the adoption of such designs, if careful analysis and experiment has shown that they actually are optimum.

A MORE REALISTIC GROUND

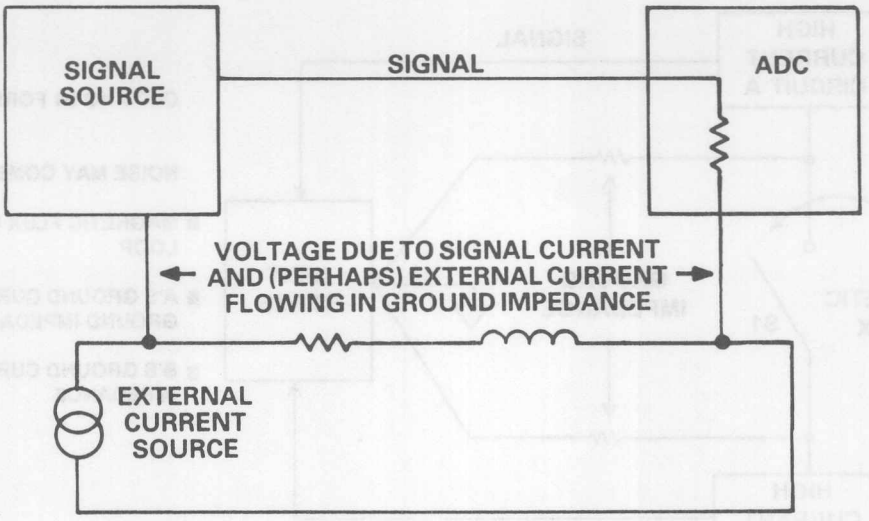


Figure 12.7

ANY CURRENT FLOWING IN A COMMON GROUND MAKES NOISE; A GROUND LOOP IS NOT NECESSARY

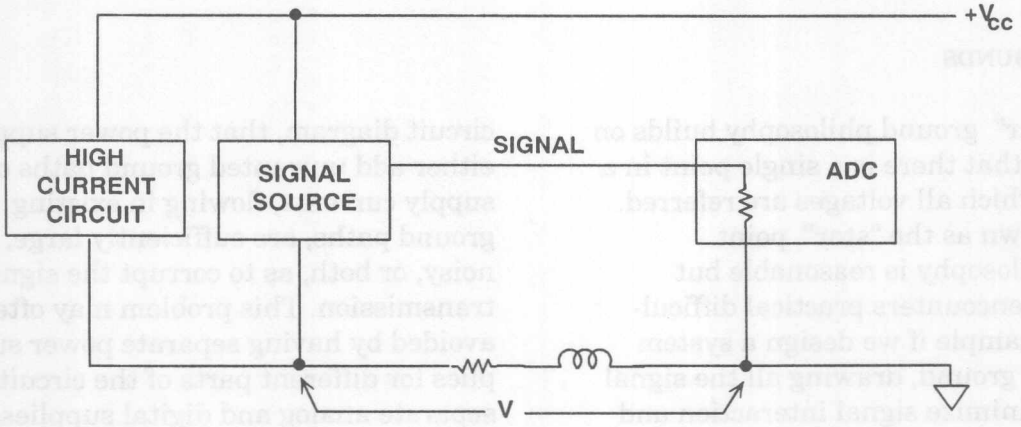


Figure 12.8

GROUND LOOP

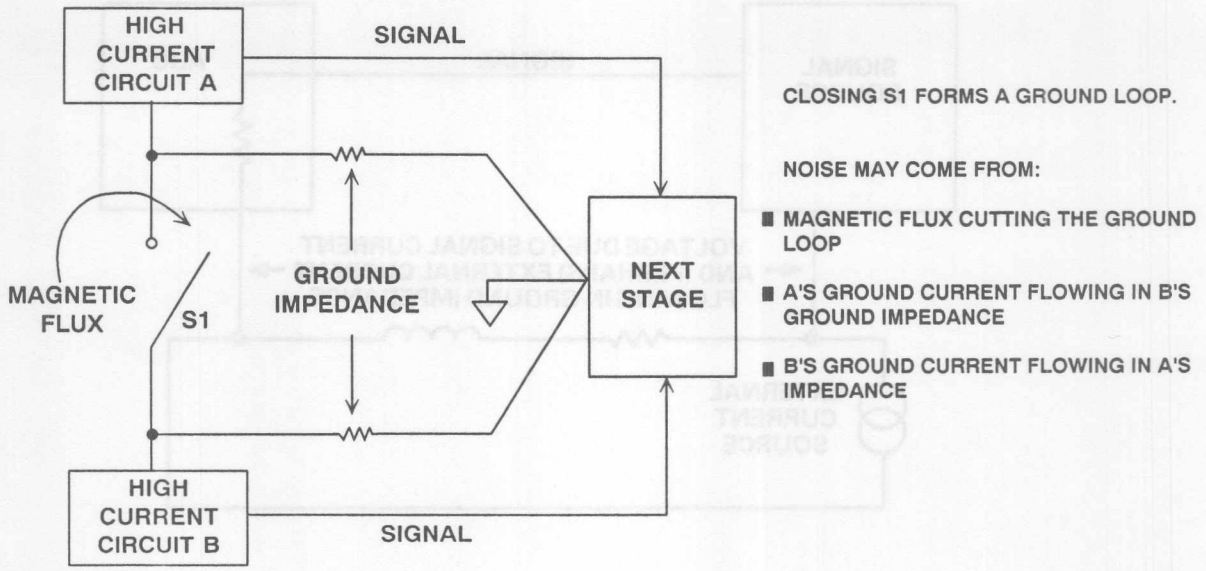


Figure 12.9

There are a number of possible ways of attacking the problem of ground noise, apart from the (presently) impracticable one of using superconducting grounds. It is rare for a single method to be used to the exclusion of all others, and systems generally contain a mixture of approaches. For the purposes of description, however, it is better to describe each approach separately.

STAR GROUNDS

The "star" ground philosophy builds on the theory that there is a single point in a circuit to which all voltages are referred. This is known as the "star" point.

This philosophy is reasonable but frequently encounters practical difficulties. For example if we design a system with a star ground, drawing all the signal paths to minimize signal interaction and the effects of high impedance signal or ground paths, we frequently find, when the power supplies are added to the circuit diagram, that the power supplies either add unwanted ground paths or that supply currents, flowing in existing ground paths, are sufficiently large, or noisy, or both, as to corrupt the signal transmission. This problem may often be avoided by having separate power supplies for different parts of the circuit - separate analog and digital supplies, and separate analog and digital grounds joined at the star point, are common in mixed signal applications.

STAR GROUNDS

■ **If all signal voltages in a system are measured with respect to a single point that point is said to be the *star* ground of the system.**

Figure 12.10

SEPARATE ANALOG AND DIGITAL GROUNDS

Digital circuitry is noisy. Saturating logic draws large fast current spikes from its supply during switching and, having noise immunity of hundreds of millivolts or more, has little need of high levels of supply decoupling.

Analog circuitry, on the other hand, is very vulnerable to noise in supplies or grounds. It is therefore sensible to separate analog and digital circuitry to prevent digital noise from corrupting analog performance. Such separation will involve separation of both grounds and power supplies, which may be inconvenient in a mixed signal system. Nevertheless, if a system is to give the full performance of which it is capable it is often essential to have separate analog and digital grounds and power supplies. The fact that some analog circuitry will operate from a single +5 V supply does NOT mean that it may safely be operated from the same noisy +5V supply as the microprocessor and dynamic RAM, the electric fan, and the solenoid jackhammer!

However, analog and digital ground in a system must be joined at some point to allow signals to be referred to a common potential. This star point, or analog/digital common point, is chosen so that it does not introduce digital currents into the ground of the analog part of the system - it is often convenient to make the connection at the power supplies.

Many ADCs and DACs have separate "analog ground" and "digital ground" pins, and users are advised, on the data sheets, to connect these pins together at the device package. This seems to conflict with the advice to connect analog and digital ground at the power supplies, and, in systems with more than one converter, with the advice to join the analog and digital ground at a single point.

SUPPLY & GROUND NOISE

- Digital circuitry is noisy
- Analog circuitry is quiet
- Circuit noise from digital circuitry carried by power and ground leads can corrupt precision analog circuitry
- It is advisable to separate the power and ground of the digital and analog parts of a system
- Analog and digital grounds must be joined at ONE point

Figure 12.11

ANALOG AND DIGITAL GROUND

- Monolithic and hybrid ADCs and DACs frequently have separate AGnd & DGnd pins which must be joined together at the device.
- This is not done from a desire to be difficult, but because the voltage drop in the bondwire is too large to allow the connection to be made internally.
- The best solution to the grounding problem arising from this requirement is to connect both pins to system "analog ground."
- It is likely that neither the digital noise so introduced in the system AGnd, nor the loss of digital noise immunity, will seriously affect the system performance.

Figure 12.12

There is, in fact, no conflict. The labels "analog ground" and "digital ground" on these pins refer to the parts of the converter to which the pins are connected, and not to the system grounds to which they must go. In general these two pins should be joined together and to the analog ground of the system. It is not possible to join the two pins within the IC package because the analog part of the converter cannot tolerate the voltage resulting from the digital current flowing in the bond wire to the chip.

If these pins are connected in this way the digital noise immunity of the converter is diminished by the amount of common- mode noise between the digital and analog system grounds. Since digital noise immunity is of the order of hundreds or thousands of millivolts this is unlikely to be important.

The analog noise immunity is diminished only by the external digital currents of the converter itself flowing in the analog ground. These currents should be quite small, and can be minimized by ensuring that the converter outputs do not drive large fanouts. If the logic supply to the converter is isolated with a small resistance and decoupled to analog ground with a 0.1 μF capacitor sited as close to the converter as possible all the internal digital currents of the converter will return to ground through the capacitor and will not appear in the external ground circuit. If the analog ground impedance is as low as it should be for adequate analog performance the additional noise due to the external digital ground current should rarely present a problem.

ANALOG GROUND (AGND) AND DIGITAL GROUND (DGND) OF ADCs/DACs SHOULD BE RETURNED TO SYSTEM ANALOG GROUND

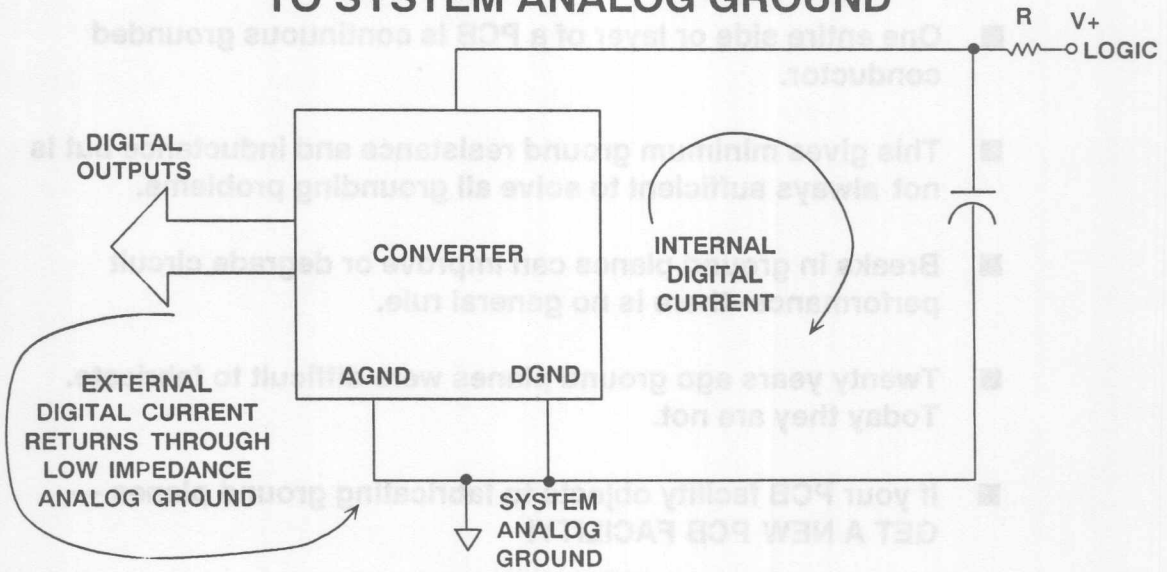


Figure 12.13

GROUND PLANES

Related to the star ground system is the use of a ground plane. One side of a double-sided PCB, or one layer of a multilayer one, is made of continuous metal, which is used as ground. The theory behind this is that the large amount of metal will have low resistance and as low inductance as is possible.

It is sometimes argued that ground planes should not be used because they are liable to introduce problems in manufacture and assembly. Such an argument may have had a limited validity twenty years ago when PCB adhesives were less well developed, wave-soldering less reliable, and solder resist techniques less well understood, but today it should not be tolerated.

Ground planes solve many ground impedance problems, but not all. Even a continuous sheet of copper foil has residual resistance and inductance and in some circumstances they can be enough to prevent proper circuit function. Figure 12.15 shows such a problem - and a possible solution.

GROUND PLANES

- **One entire side or layer of a PCB is continuous grounded conductor.**
- **This gives minimum ground resistance and inductance but is not always sufficient to solve all grounding problems.**
- **Breaks in ground planes can improve or degrade circuit performance--there is no general rule.**
- **Twenty years ago ground planes were difficult to fabricate. Today they are not.**
- **If your PCB facility objects to fabricating ground planes --- GET A NEW PCB FACILITY!**

Figure 12.14

A SLIT IN A GROUND PLANE CAN RECONFIGURE CURRENT FLOW FOR BETTER ACCURACY

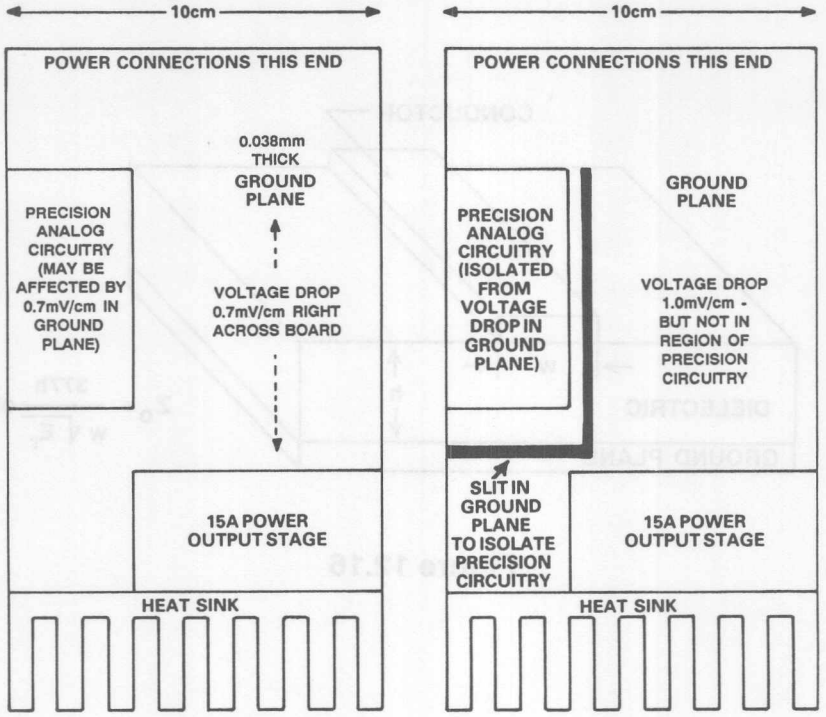


Figure 12.15

Consider a ground-plane PCB 100 mm wide with a ground connection at one end and a power amplifier at the other drawing 15A. If the ground plane is 0.038 mm thick and 15 A flows in it there will be a voltage drop of 68 μV/mm. This voltage drop would cause quite serious problems to any ground-referenced precision circuitry sharing the PCB. However, if we slit the ground plane so that high current does not flow in the region of the precision circuitry we can possibly solve the problem - even though the voltage gradient will increase in those parts of the ground plane where the current does flow.

TRANSMISSION LINES

A break in a ground plane is not always a good thing. We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. As we saw in Figure 11.7, when an HF signal flows in a PC track running over a ground plane the arrangement functions as a microstrip transmission line and the majority of the return current flows in the ground plane underneath the line.

The characteristic impedance of the line will depend upon the width of the track and the thickness and dielectric constant of the PCB material. For most lower frequency applications the characteristic impedance will be unimportant, as the line will not be correctly terminated, but at UHF and higher it is possible to use PCB tracks as microstrip transmission lines in properly terminated systems. If losses in such systems are to be minimized the PCB material must be chosen for low high frequency loss. This usually means the use of expensive teflon PCB material.

MICROSTRIP TRANSMISSION LINE

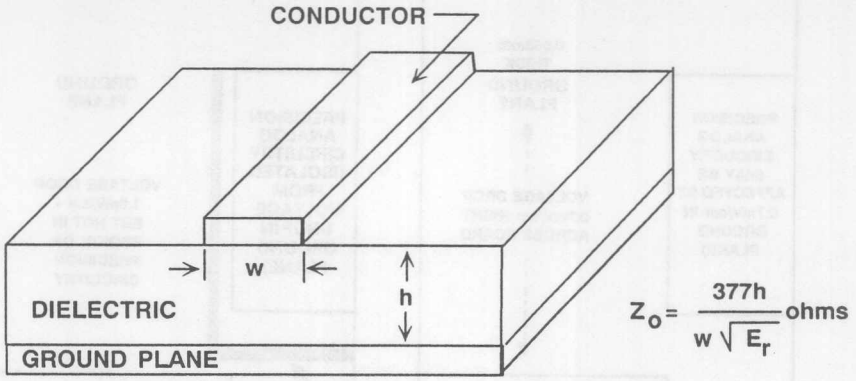


Figure 12.16

BREAKS IN GROUND PLANE RAISE INDUCTANCE

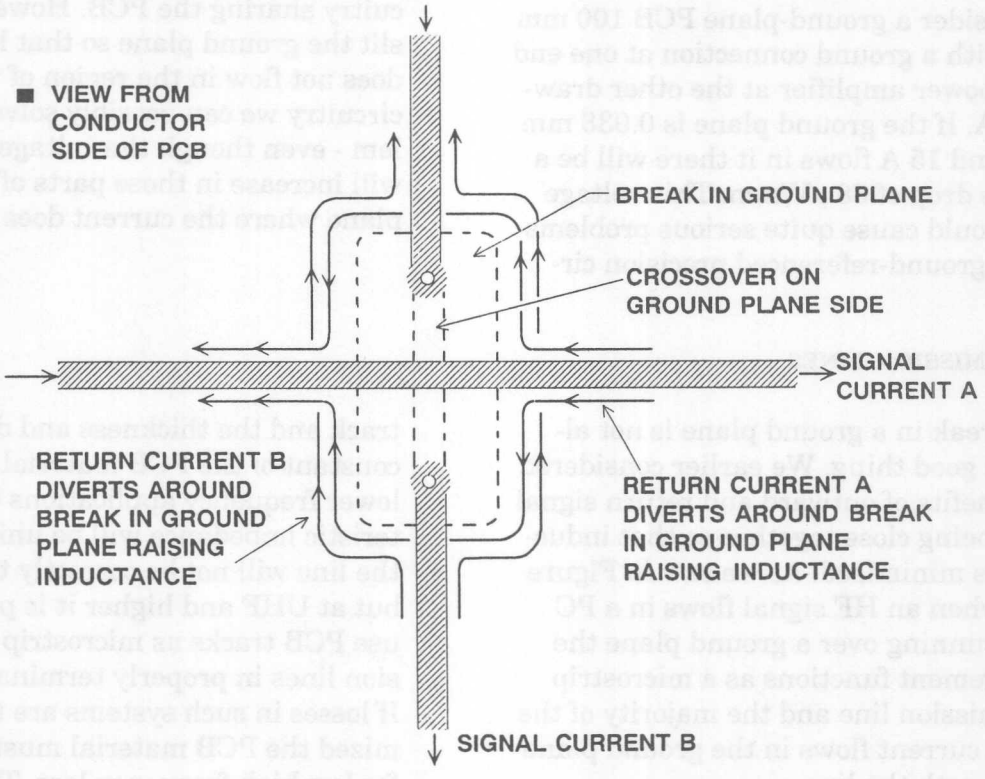


Figure 12.17

Where there is a break in the ground plane under a conductor the return current must flow around the break and both the inductance and the vulnerability of the circuit to external fields are increased.

Where such a break is made to allow a crossover of two perpendicular conductors it would be far better if the second signal were carried across both the first and the ground plane by means of a piece of wire. The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multi-layer board both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multi-layer PCBs are expensive and harder to trouble-shoot than simple double-sided boards but do offer even better shielding and signal routing. The principles involved remain unchanged but the range of layout options is increased.

Use of double-sided or multi-layer board with at least one continuous ground plane is undoubtedly one of the most successful approaches to the design of high performance mixed signal circuitry. Often the impedance of the ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system, but this does depend upon the resolution and bandwidth required and the amount of digital noise in the system.

SYSTEM GROUNDS

In systems where there are several PCBs grounding may be more of a problem. At first sight it would appear that the problem is similar to that of a single PCB where particular subsystems must be positioned so that large ground currents do not flow where ground noise must be minimized - in a multicard system the grounds of individual PCBs must be interconnected so that such harmful interactions are minimized.

There are three problems with this. First of all there is far less opportunity for rearranging the physical layout of a system consisting of a few cards connected to a common backplane. Secondly many multicard systems are designed to be reconfigured in a "mix 'n' match" arrangement to allow large numbers of system options - it can be impossible to predict what systems are going to be required and to ensure that all of them are noise free. Finally, multicard systems are likely to have higher ground currents than occur on single, relatively simple, PCBs - but these currents must flow in the higher impedances which are associated with the intercard connectors even when multiple ground pins are used.

The basic principles still apply: ground impedance must be as low as possible, high level and low level signals must be separated so that they do not interfere with each other, and capacitance and mutual inductance coupling must be avoided. Nevertheless, it must be accepted that situations can arise where it is not possible to transfer a high speed, high accuracy signal from one PCB to another without unacceptable signal degradation.

MULTIPLE CARD SYSTEMS

- **Multiple card systems are likely to have higher ground currents and higher ground impedances than are found on a single PCB.**
- **It is therefore more difficult to transfer ground-referenced signals accurately between cards than across a PCB.**
- **In some cases it will be IMPOSSIBLE to transfer ground-referenced signals between PCBs without unacceptable loss of quality.**

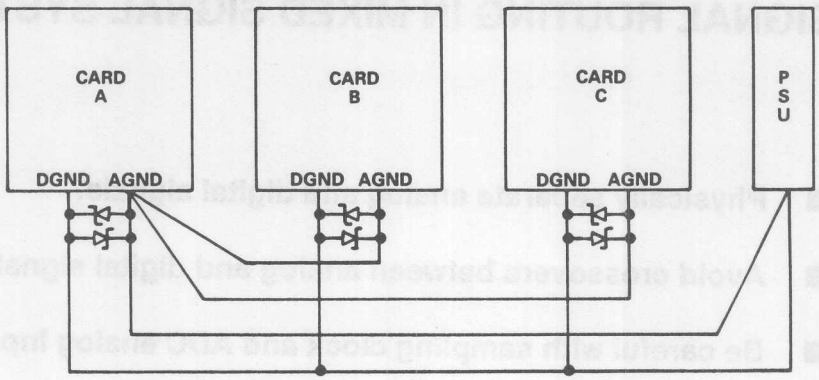
Figure 12.18

The best way of minimizing ground impedance in a multicard system is to use another PCB as a backplane and have a ground plane (or even two - one analog, one digital) on that mother card. If the earlier advice about multiple ground pins has been observed this arrangement is capable of excellent performance. Where there are several card cages (racks for PCBs) the ground planes of the several mother boards must be tied together and, probably, to the metal chassis holding the card cages - the exact layout of the interconnections will depend on the overall system architecture.

If a mother board with a ground plane is not possible then the ground pins of the PCB sockets must be wired together, with due attention to probable current flows and common ground impedances, with heavy, multi-strand wire, having as low resistance as possible. In many cases the resulting ground screen will be tied to chassis ground at a number of points but it will sometimes be better to join them at a single star point.

It is not just the ground layout that is important in high performance mixed signal systems, the siting of different subsystems and the routing of signals is most important in determining overall system performance.

STAR ANALOG GROUND IN A MULTICARD SYSTEM



- Schottky diodes protect cards in the event of loss of analog ground
- This grounding system may be inadequate at high resolution or where large ground currents flow
- This MAY permit accurate intercard transmission of ground referenced signals

Figure 12.19

SIGNAL ROUTING

It is evident that we can minimize noise by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

If a ground plane is used, as it should in be most cases, it can act as a shield where sensitive signals cross. Figure 12.21 shows a good layout for a data acquisition system where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this the principle remains a valid one.

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mOhms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 20-30% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection,

SIGNAL ROUTING IN MIXED SIGNAL SYSTEMS

- Physically separate analog and digital signals.
- Avoid crossovers between analog and digital signals.
- Be careful with sampling clock and ADC analog input runs.
- Be careful with high impedance points.
- Use lots of ground plane.
- Use microstrip techniques for controlled impedances.

Figure 12.20

PCB FLOWCHART

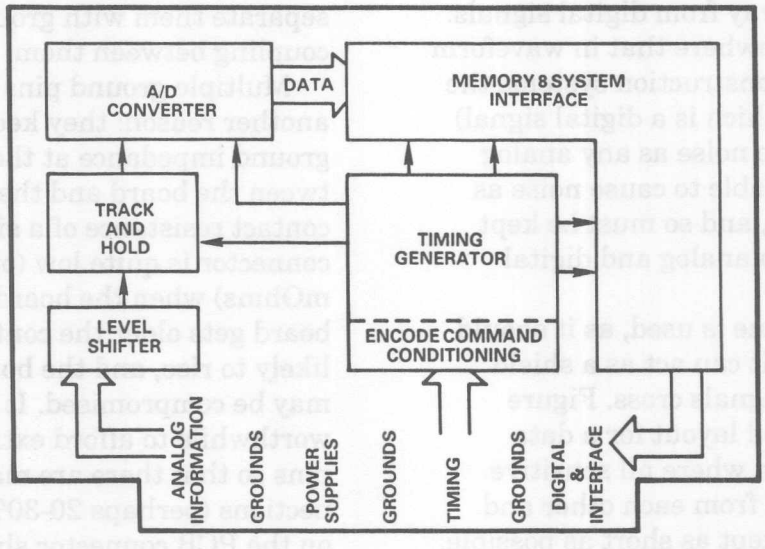


Figure 12.21

EDGE CONNECTIONS

- **Separate sensitive signals by ground pins.**
- **Keep down ground impedance with multiple (20-30% of total) ground pins.**
- **Have several pins for each power line.**
- **Critical signals may require a separate connector (possibly coax).**

Figure 12.22

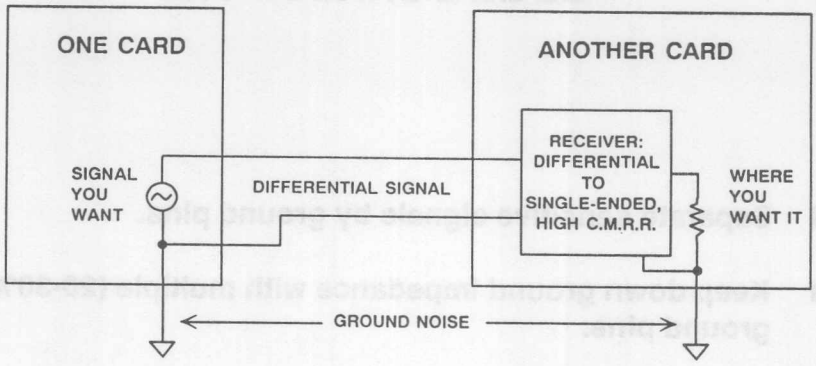
although there is no need to have as many as there are ground pins.

Modern high performance mixed signal systems handle signals with resolutions of 8 bits at sampling rates of over 500 MHz and resolutions of 14 bits sampled at more than 10 MHz. Preserving signal integrity between cards in a multi-card system is extremely difficult at such performance levels and may be impossible.

The use of balanced transmission lines can help but if the signal bandwidth extends to DC there will be a need for a very high performance instrumentation amplifier at the receiving end to restore a ground referenced signal.

The best, and in many cases the only, solution to problems of this sort, is to partition the system so that the highest quality signals are not transferred between boards.

DIFFERENTIAL TRANSMISSION MINIMIZES GROUND ERRORS



- At DC and LF the receiver will be an instrumentation amplifier
- At HF the receiver will be a transformer
- There is no ideal receiver for video signals which have components from DC to HF

Figure 12.23

VIDEO SIGNAL TRANSMISSION

- It is often IMPOSSIBLE to transmit very broadband high accuracy signals between the PCBs of a multicard system without unacceptable loss of quality.
- In such cases the system must be reconfigured to allow all the analog processing to take place on a single PCB.
- It may be inconvenient, but it's the only way you'll get it to work!

Figure 12.24

PROBLEM AREAS

LIMITATIONS OF SPICE MODELLING

As we have seen, real electronic circuits contain many "components" which were not present in the circuit diagram but which are there because of the physical properties of conductors, circuit boards, IC packages, etc. These components are difficult, if not impossible, to incorporate into computer modelling software and yet they have substantial effects on circuit performance at high resolutions, or high frequencies, or both.

It is therefore inadvisable to use SPICE modelling or similar software to predict the ultimate performance of such high performance analog circuits. After modelling is complete the performance must be verified by experiment.

This is not to say that SPICE modelling is valueless - far from it. Most modern high performance analog circuits could never have been developed without the aid of SPICE and similar programs, but it must be remembered that such simulations are only as good as the models used and these models are not perfect. We have seen the effects of parasitic components arising from the conductors, insulators and components on the PCB, but it is also necessary to appreciate that the models used within SPICE simulations are not perfect models.

Consider an operational amplifier. It contains some 20-40 transistors, almost as many resistors, and a few capacitors. A

SPICE MODELLING

- **SPICE modelling is a powerful tool for predicting the performance of analog circuits.**

HOWEVER

- **Models omit real-life effects**
- **No model can simulate all the parasitic effects of discrete components and a PCB layout.**

THEREFORE

- **Prototypes must be built and proven before production.**

Figure 12.25

complete SPICE model will contain all these components and probably a few of the more important parasitic capacitances and spurious diodes formed by the diffusions in the op-amp chip. This is the model that the designer will have used to evaluate the device during his design. In simulations such a model will behave very like the actual op-amp, but not exactly.

However, this model is not published, as it contains too much information which would be of use to other semiconductor companies who might wish to copy or improve on the design. It would also take far too long for a simulation of a system containing such models of a number of op-amps to reach a useful result. For these, and other, reasons the SPICE models of analog circuits published by manufacturers or software companies are "macro" models, which simulate the major features of the component but lack some of the fine detail. Consequently SPICE modelling does not always reproduce the exact performance of a circuit and should always be verified experimentally.

SOCKETS

It is tempting to mount expensive ICs in sockets rather than soldering them in circuit - especially during circuit development. Engineers would do well not to succumb to this temptation.

USE OF SOCKETS WITH HIGH PERFORMANCE ANALOG CIRCUITS

- **DON'T! (If at all possible)**
- **Use "Pin sockets" or "Cage jacks" such as Amp Part No: 5-330808-3 or 5-330808-6 (Capped & uncapped respectively).**
- **Always test the effect of sockets by comparing system performance with and without the use of sockets.**
- **Do not change the type of socket used without evaluating the effects of the change on performance.**

Figure 12.26

Sockets add resistance, inductance and capacitance to the circuit and may degrade performance to quite unacceptable levels. When this occurs, though, it is always the IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon not to degrade the performance of high performance (high speed or high precision or, worst of all, both) devices, and as the socket ages and the board suffers vibration the contact resistance of low insertion force sockets is very likely to rise. Where a socket must be used the least loss of performance is achieved by using individual pin sockets (sometimes called "cage jacks") to make up a multi-pin socket in the PCB itself.

It really is best not to use IC sockets with high performance analog and mixed signal circuits. If their use can be avoided it should be. However at medium speeds and medium resolutions the trade-off between performance and convenience may fall on the side of convenience. It is very important, when sockets are used, to evaluate circuit performance with and without the socket chosen to ensure that the type of socket chosen really does have minimal effect on the way that the circuit behaves. The effects of a change of socket on the circuit should be evaluated as carefully as a change of IC would be and the drawings should be prepared so that the change procedures for a socket are as rigorous as for an IC - in order to prevent a purchase clerk who knows nothing of electronics from devastating the system performance in order to save five cents on a socket.

PROTOTYPING HIGH PERFORMANCE ANALOG CIRCUITRY

As we have seen, circuit board layout is part of the circuit design of all high performance analog circuits. Prototyping techniques derived from the "node" theory, while ideal for logic breadboarding at low and medium speeds, are quite unsuitable for any analog circuits, or even for very fast digital ones. Vector board and wire wrap prototyping will tell an engineer nothing about the behavior of a properly laid out version of the analog circuit.

The best technique for analog prototyping is to use a prototype of the final PCB - certainly no design is complete until the final PCB layout has been proved to give the required performance. Nevertheless this approach may be a little limiting where a number of different possibilities are to be evaluated, or for a multicard system.

In this case components should be mounted on a board having a continuous copper ground plane (ideally on both sides of the board, though while convenient this is not essential), with ground connections made to the plane and short point to point wiring made above and below it. The overall component placing and signal routing should be as close as possible to the planned final layout.

As we have already indicated, IC sockets can degrade the performance of analog ICs. While directly soldered components are ideal for prototyping, an IC socket made of pin sockets mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5 mm around each ungrounded pin socket - solder the grounded ones to ground on both sides of the board).

Allowing wiring to float in the air can be a little tricky. There is a breadboarding system which is conceptually very similar to that described above but which provides adhesive PC pads which stick to the ground plane and allow more rigid component mounting and wiring. This system is manufactured by Wainwright Instru-

PROTOTYPING MIXED SIGNAL CIRCUITRY

- **NEVER use vector boards or wire-wrap for the analog parts of the system (they can be invaluable for data buses and address lines in the digital part).**
- **Wherever possible avoid the use of sockets for analog ICs.**
- **Use a prototype of your final PCB layout as early as possible.**

Figure 12.27

ments and is known as "Minimount" in Europe and "Solder Mounts" in the USA. The manufacturer's and distributors' addresses are given in the references at the end of this section.[2]

Manufacturer's evaluation boards are also useful in system prototyping since they have already been optimized for best performance. Analog Devices offers many evaluation boards for a wide array of products. They offer the designer an excellent starting point for the layout.

When the prototype layout is transferred to a CAD system for PCB layout it is important to disable, or at any rate override where necessary, any automatic routing or component placing software. The criteria used by such software are more closely related to "node" theory and aesthetically pleasing rows of components (which, admittedly, are also easier on automatic component placing machinery) than to optimizing stray inductance and capacitance and minimizing common ground impedances.

ADDITIONAL PROTOTYPING HINTS

- Pay *equal* attention to signal routing, component placing and supply decoupling in *both* the prototype and the final design.
- Verify performance as well as functionality at each stage of the design.
- For "freehand" prototyping use a copper-clad board, mount components to it by their ground pins and wire the remaining connections point-to-point (use Wainwright Instruments' Minimount/Solder Mountadhesive PC pads if aerial point-to-point wiring seems too fraught with peril).

Figure 12.28

NOTES

1 "E.S.D. Prevention Manual"
Available free from Analog Devices.

2 Wainwright Instruments Inc. P.O.Box 2203, Capistrano Beach, CA 92624. Tel: 714-248-2490 Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-2245

SECTION XIII
ANALOG CIRCUIT SIMULATION

- Macromodel Versus Micromodel
- The ADSpice Model
- The Noise Model
- Current Feedback Amplifier Model
- Voltage Reference Model
- Analog Multiplier Model
- Simulation and Breadboarding
- Using Simulation Wisely

SECTION XIII

ANALOG CIRCUIT SIMULATION

JOE BUXTON

In the past few years, circuit simulation has been taking on an increasingly important role in the design of analog circuits, and SPICE, in its multiple forms, continues to be the most popular simulation tool. However, to achieve accurate and meaningful results, designers need accurate models of the many devices and components in their systems. In answer to this need, Analog Devices developed an advanced SPICE model for operational amplifiers. By utilizing an innovative open architecture, the gain and phase response can be fully modelled, enabling designers to accurately predict their circuits' AC and transient behavior as well as DC performance. Since then, this modelling methodology has been extended to such varied devices as instrumentation amplifiers, references, and analog multipliers.

The popularity of SPICE simulation has led to the release of op amp macromodels from many different sources, such as device manufacturers and SPICE software vendors. With the many versions comes confusion as to what is modelled, what is not modelled, and how accurate the model is. All of which are important to understand in order to know whether or not the simulation results are believable. Thus, it is important to verify each model before using it. This involves checking the model and comparing it to the actual device under various conditions such as a transient response.

SIMULATION IS A POWERFUL TOOL WHEN USED WISELY

- **Understand the Goals of the Simulation**
- **Evaluate the Models Accordingly**
- **Know the Capabilities for Each Op Amp Model From Different Sources**
- **Breadboarding is Necessary in Addition to Simulation**

13

Figure 13.1

An accurate model alone does not guarantee accurate simulations. Instead, each circuit needs to be verified in the lab by breadboarding. A breadboard of the circuit can often reveal behavior that was not predicted by SPICE either because of an incomplete model, external circuit parasitics, or numerous other reasons. By using SPICE and breadboarding together, a circuit can be efficiently and quickly designed with good assurance of working properly on the final PC board.

MACROMODEL VS. MICROMODEL

The distinction between macromodel and micromodel is often unclear. A micromodel is the actual transistor level model of the device with all the active devices fully characterized according to the process the device is built on. Typically, a micromodel is used in the actual design of an IC. In contrast, a macromodel looks at a finished device and uses ideal elements to model its observed behavior. In other words, in developing a macromodel a device is measured in the lab, and then the model is adjusted to match this behavior.

There are advantages and disadvantages to both approaches. A micromodel can give a complete and accurate model of the circuits behavior under almost all conditions. However, because of the large number of transistors with their multiple internal nodes, the simulation time is very long. Also, manufacturers are reasonably reluctant to release these models because they contain proprietary information about the process and design of the IC. Lastly, even though all the transistors are included, this is not a guarantee that the model will be accurate. The transistor models themselves do not cover all regions of operation or may have inaccuracies in their characterization. Any small errors in the transistor models can translate into larger errors in the complete device model. Futhermore, because the number of nodes is high, SPICE has more difficulty in DC and transient convergence calculations, which may cause the simulation to fail.

On the other hand, if carefully developed, a macromodel can produce accurate results while saving considerable simulation time. With an advanced model such as the ADSpice model (described in the next section), the transient and AC performance of the device can be closely replicated. Furthermore, much of an op amp's non-linear behavior can also be included, such as short circuit current limits and output voltage swing. However, because the macromodel is a simplified version of the device, not all non-linearities are modelled. For example, the ADSpice model does not include the common mode input voltage range, which would most likely be part of a micromodel. This is not to say that such effects could not be included, but a choice was made to concentrate on more critical parameters such as AC and transient response. Adding every possible op amp characteristic would lead to a macromodel that was overly large, slow, and could possibly have convergence problems. Thus, the ADSpice macromodel includes an op amp's behavior that is critical to a circuit's performance under normal operating conditions, but does not necessarily model some of the non-linear behavior.

MACROMODEL OR MICROMODEL??

	METHODOLOGY	ADVANTAGES	DISADVANTAGES
MACROMODEL	Ideal Elements Model the Device Behavior	Fast Simulation Time, Easy to Modify	May Not Model All Characteristics
MICROMODEL	Fully Characterized Transistor Level	Most Complete Model	Slow Simulation, Difficulty in Convergence

Figure 13.2

THE ADSPICE MODEL

The ADSpice model was developed to advance the state-of-the-art in op amp macromodelling and provide a tool for designers to accurately simulate their circuits. Previously, the dominant model architecture was the Boyle model.[1] However, this model was developed over 15 years ago and does not accurately model many of today's higher speed amplifiers. The primary reason for this is that the Boyle model has only two frequency shaping poles and no zeroes. In contrast, the ADSpice model has an open architecture that allows for unlimited poles and zeroes, leading to much more accurate AC and transient responses.

The ADSpice model is comprised of three main portions, the input and gain stage, the pole / zero stages, and the output stage. The input stage shown in Figure 13.3 uses the only two transistors in the entire model. These are needed to properly model an op amp's differential input stage characteristics. Although the example here uses NPN transistors, the input stage can easily be modified to include PNP, JFET, or CMOS devices. The rest of the input stage uses simple SPICE elements such as resistors, capacitors, and controlled sources. An example of a controlled source is Gm1 in the gain stage, which is a voltage controlled current source. It senses the differential collector voltage from the input stage and converts that to a current. When the current flows through R_7, a single ended voltage is produced. By making the product of gm_1 and R_7 equal to the open loop gain, the entire open-loop gain is produced in the gain stage, which means that all other stages are unity gain. This leads to significant flexibility in adding and deleting stages.

INPUT AND GAIN STAGES

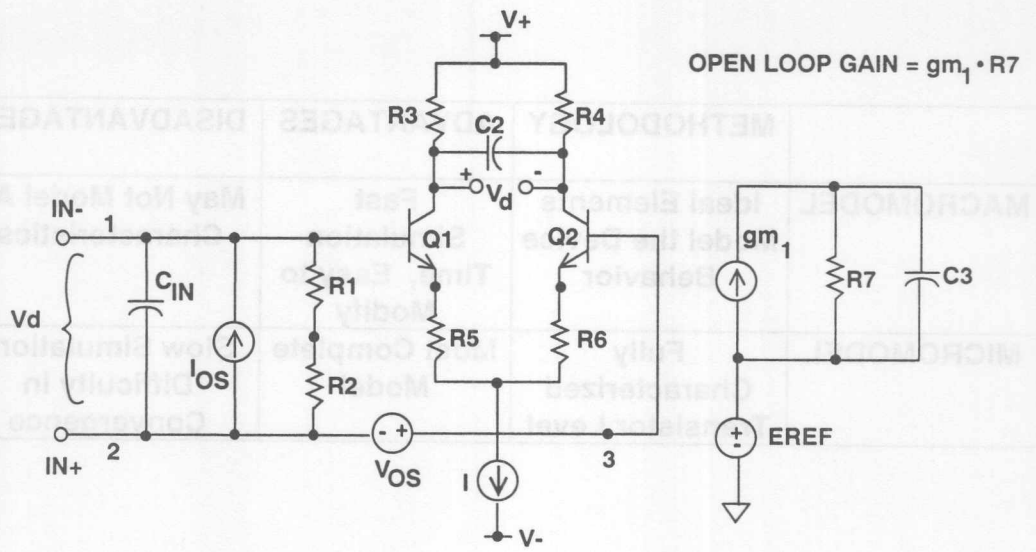


Figure 13.3

POLE AND ZERO STAGE

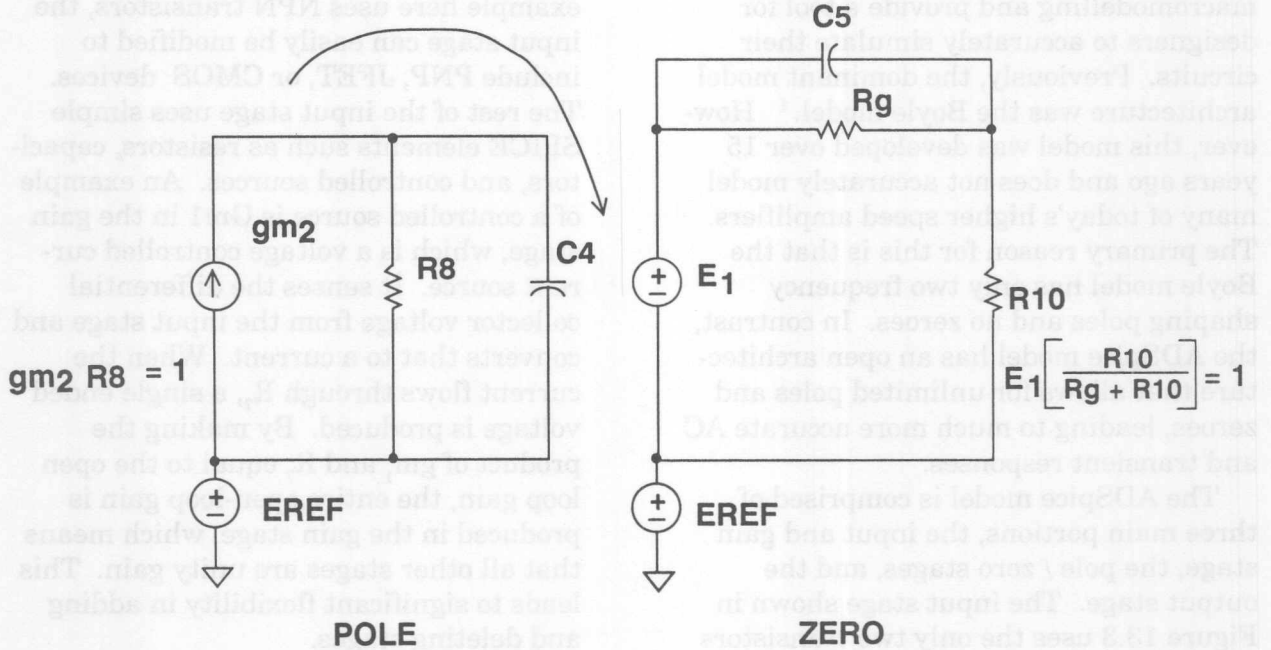


Figure 13.4

Following the gain stage are an unlimited number of pole / zero stages. The typical topology of these stages is shown in Figure 13.4, which is similar to the gain stage. The main difference is that now the product of gm_2 times R_8 is equal to unity. The pole or zero frequency is set by the parallel combination of the resistor and capacitor, R_8 C_4 for the pole and R_9 C_5 for the zero. Because these stages are unity gain, any number of them can be added or deleted without affecting the low frequency response of the model. Instead, the high frequency gain and phase response can be tailored to accurately match the actual amplifier's response. The benefits are especially apparent in closed loop pulse response and stability analysis.

The output stage in Figure 13.5 not only models the open loop output impedance at DC but with the inclusion of an inductor also models the rise in impedance at high frequencies. Additionally, the output current is correctly reflected in the supply currents. This is a significant improvement over the Boyle model because now the power consumption of the circuit under load can be analyzed accurately. Furthermore, circuits that use the supply currents for feedback can also be simulated.

All of these improvements satisfied our goal of providing an accurate state-of-the-art macromodel that can predict a circuit's behavior under many different conditions including the difficult AC and transient analysis. A comparison in Figure 13.6 of the ADSpice model, the Boyle model, and an actual op amp reveals the improved performance from the unlimited number of poles and zeros. The difference is easily apparent from a transient analysis plot for a simple unity gain follower circuit. In this case an OP-249 amplifier is used with the output connected to the inverting input and a 260pF capacitive load to produce the ringing seen in the response. The ADSpice model accurately predicts the amount of overshoot and frequency of the damped ringing in contrast to the Boyle model, which predicts about half the overshoot and significantly less ringing.

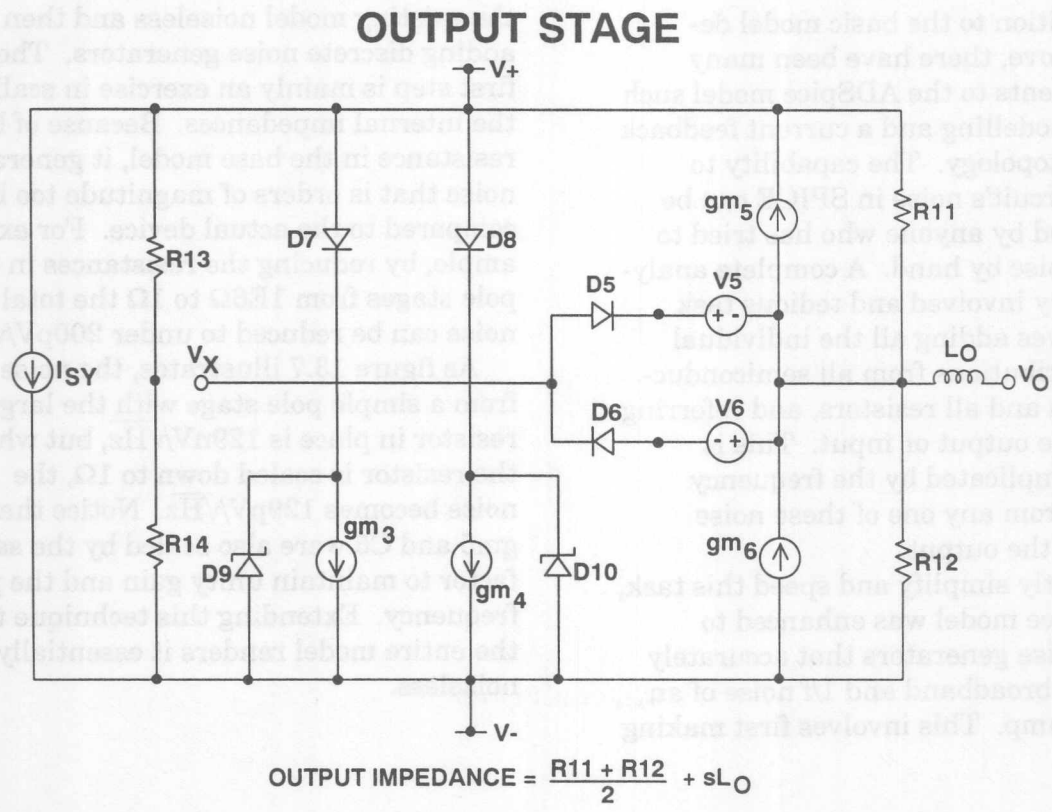
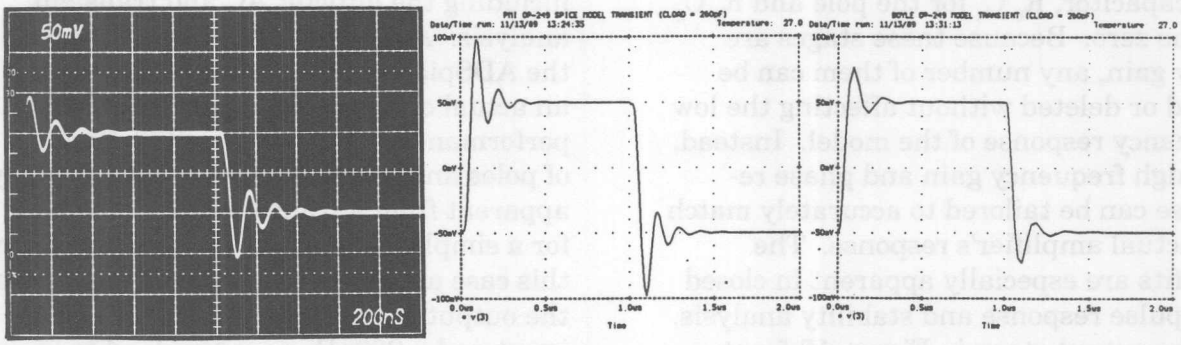


Figure 13.5

OP-249 TRANSIENT RESPONSE TEST

ACTUAL **ADSpice MODEL** **BOYLE MODEL**



VERTICAL SCALE: 50mV / div.
HORIZONTAL SCALE: 200ns / div.

LOAD = 260pF

Figure 13.6

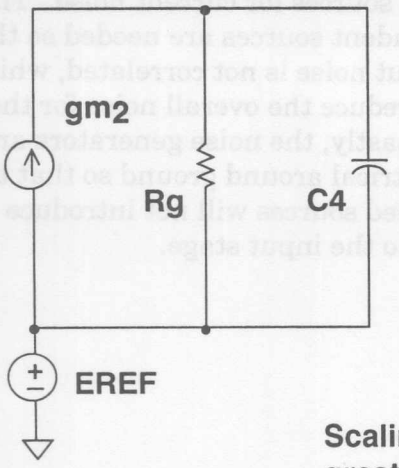
THE NOISE MODEL

In addition to the basic model described above, there have been many enhancements to the ADSpice model such as noise modelling and a current feedback amplifier topology. The capability to model a circuit's noise in SPICE can be appreciated by anyone who has tried to analyze noise by hand. A complete analysis is a very involved and tedious task that involves adding all the individual noise contributions from all semiconductor devices and all resistors, and referring them to the output or input. This is further complicated by the frequency response from any one of these noise sources to the output.

To greatly simplify and speed this task, the ADSpice model was enhanced to include noise generators that accurately mimic the broadband and 1/f noise of an actual op amp. This involves first making the existing model noiseless and then adding discrete noise generators. The first step is mainly an exercise in scaling the internal impedances. Because of high resistance in the base model, it generates noise that is orders of magnitude too large compared to the actual device. For example, by reducing the resistances in the pole stages from 1E6Ω to 1Ω the total noise can be reduced to under $200pV/\sqrt{Hz}$.

As figure 13.7 illustrates, the noise from a simple pole stage with the large resistor in place is $129nV/\sqrt{Hz}$, but when the resistor is scaled down to 1Ω, the noise becomes $129pV/\sqrt{Hz}$. Notice that gm5 and C5 were also scaled by the same factor to maintain unity gain and the pole frequency. Extending this technique to the entire model renders it essentially noiseless.

NOISE FROM A POLE STAGE

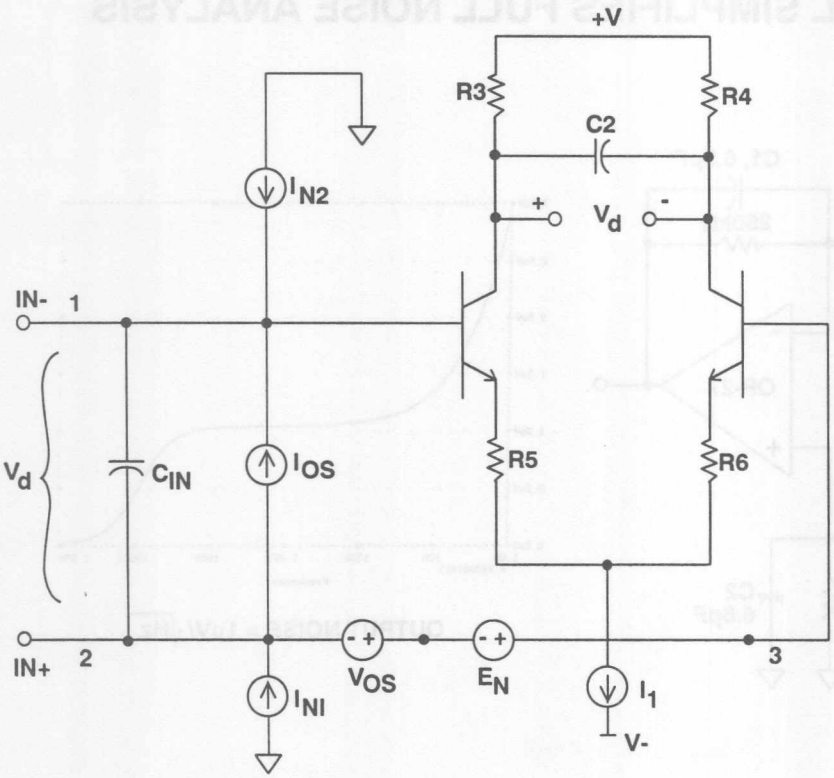


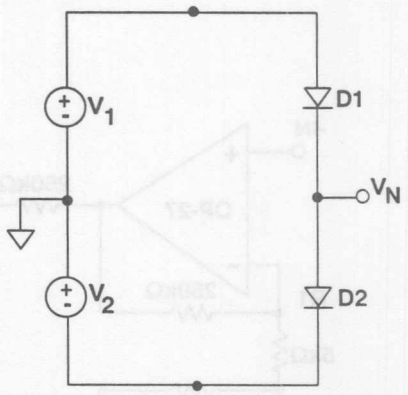
	CASE	
	"NOISY"	"NOISELESS"
Rg	$1x10^{6}\ \Omega$	1Ω
gm2	$1x10^{-6}$	1.0
C4	$159x10^{-15}$F	$159x10^{-15}$F
Noise	$129nV/\sqrt{Hz}$	$129pV/\sqrt{Hz}$

Scaling the resistors down greatly reduces noise

Figure 13.7

ADDING NOISE TO THE INPUT STAGE





- The noise source is symmetrical to prevent DC offsets.
- Voltage-controlled sources introduce the noise in the input.

Figure 13.8

13

Once this is achieved, three independent noise sources are added, one for voltage noise and two for current noise. All three noise sources have the same topology shown in Figure 13.8. In SPICE, semiconductor models have the built in ability to generate both broadband (thermal) noise and 1/f (flicker) noise. The noise generators use diodes mainly because they are the simplest to work with. By properly specifying the series impedance (RS) to get the broadband noise and the flicker coefficients (KF and AF) for the 1/f noise, this topology can achieve any amount of input noise. The noise is then introduced into the input stage using a voltage controlled voltage source for voltage noise and two voltage controlled current sources for current noise. Three independent sources are needed so that the input noise is not correlated, which would reduce the overall noise for the op amp. Lastly, the noise generators are symmetrical around ground so that the controlled sources will not introduce a DC bias into the input stage.

NOISE MODEL SIMPLIFIES FULL NOISE ANALYSIS

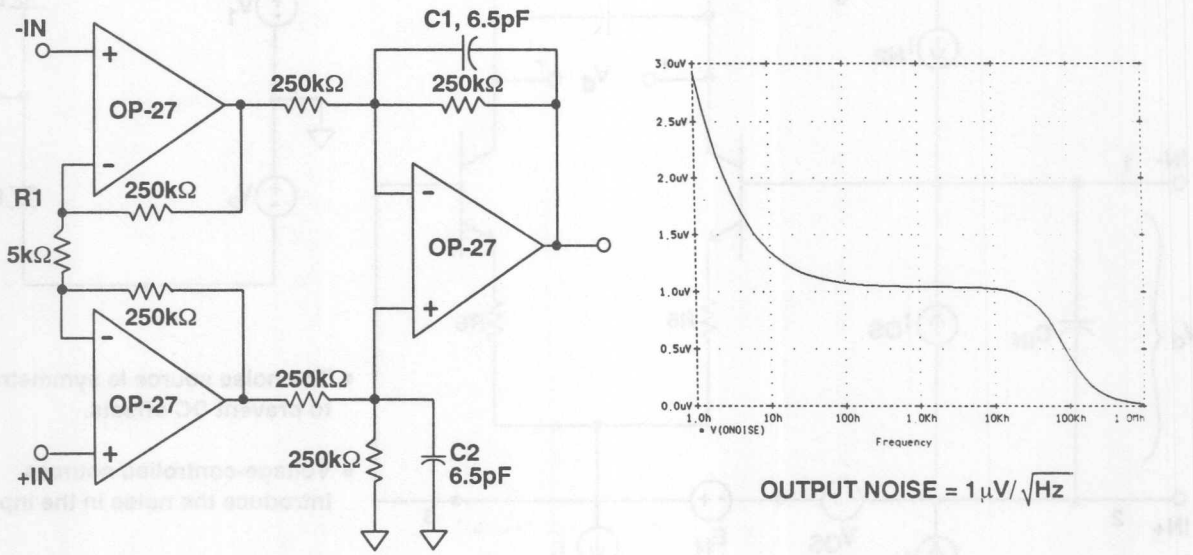


Figure 13.9

Running a noise analysis in SPICE can reveal substantial information about a circuit's noise performance. The broadband and 1/f noise referred to output or input can be plotted, as well as the total RMS noise. SPICE can also print out the noise contribution due to each element to determine the dominant sources. A simple three op amp instrumentation amplifier with a gain of 100 is a good example of how the ADSpice noise model can predict the total noise of a system. Figure 13.9 shows the topology, which in this case uses OP-27 op amps because of their low noise performance of $3nV/\sqrt{Hz}$. Running a SPICE analysis results in a broadband noise of $1\mu V/\sqrt{Hz}$ and a 1/f corner at 10Hz.

An even more useful number is the total RMS noise. This can be plotted in such programs as MicroSim's Probe by integrating the noise over the circuit's entire bandwidth. Figure 13.10 shows the total output noise as $270\mu V_{RMS}$. As can be seen from this graph, noise is being collected all the way up to 55kHz; however, if the circuit only needs a bandwidth of 1kHz, then much of the noise can be filtered out by increasing the value of C1 and C2 to 640pF. Doing so results in a total noise figure of $40\mu V_{RMS}$, which is also plotted in Figure 13.10. Already the noise has been improved by a factor of 7, but there may still be room for improvement. Looking at the SPICE output file for each component's contribution to total noise reveals that the input resistor, R1, dominates. Reducing it to 500Ω, and all the other resistors by the same factor of 10, further lowers the total noise to $20\mu V_{RMS}$ as shown on the bottom trace of the graph. As this example illustrates, the ADSpice noise model greatly simplifies a complete noise analysis, which further speeds the design of a circuit.

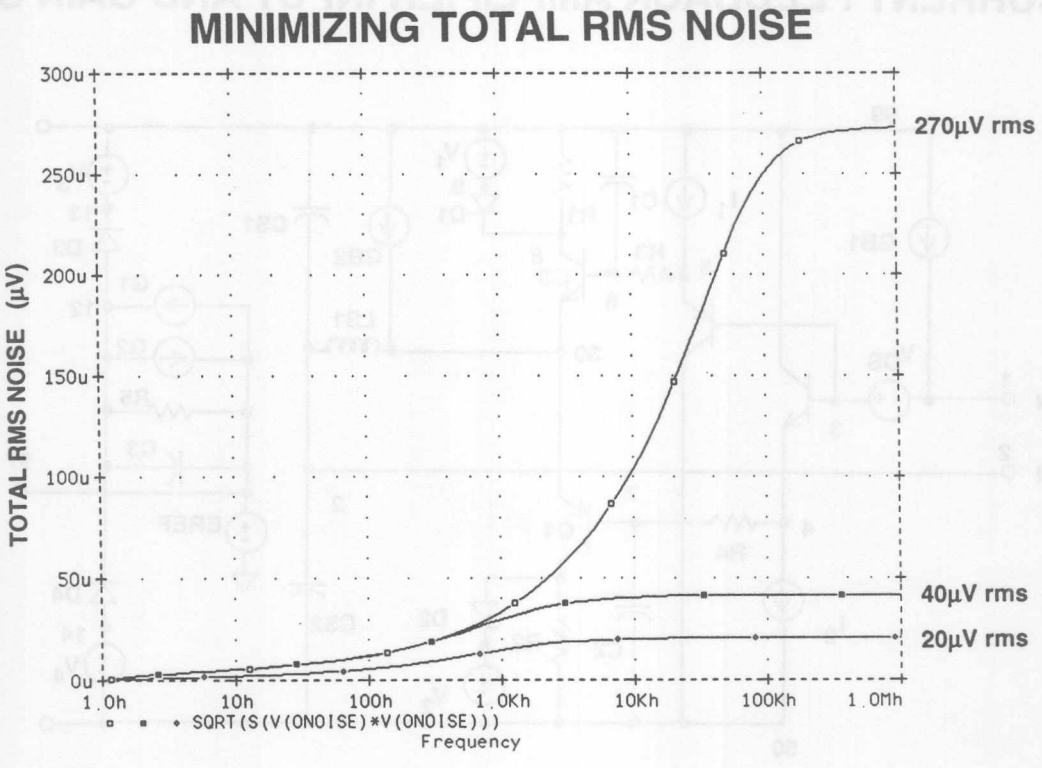


Figure 13.10

CURRENT FEEDBACK AMPLIFIER MODEL

A new model topology had to be developed for current feedback amplifiers to accommodate their unique input stage structure. The model uses the topology shown in Figure 13.11 for the input stage, and the rest of the model containing the gain stage, pole / zero stages, and output stage are essentially the same as for voltage feedback amplifiers. The input stage resembles that of most actual current feedback amplifiers with a high impedance non-inverting input and a low impedance inverting input. The slew rate is very high in current feedback amplifiers because large amounts of current can flow in the inverting input, which is then available to charge the compensation capacitor by using current mirrors. The current mirrors in the ADSpice model is actually the voltage controlled current sources in the gain stage. These sense the voltage drops across the input stage resistors (R1 and R2) and translates this into a current to charge C3. By making the value of G1 and G2 equal to the reciprocal of R1 and R2, the currents will be identical. Clamping the voltage drops across R1 and R2 limits the total current and thus the amplifier's slew rate.

One of the unique properties of current feedback amplifiers is that the bandwidth is a function of the feedback resistor and the internal compensation capacitor C3. The lower the feedback resistor, the higher the bandwidth. The lower limit of the resistor is the value at which the part oscillates. By the model also includes the low impedance inverting input, it will accurately mimic the actual parts behavior as the resistor is altered. Figure 13.12

CURRENT FEEDBACK AMPLIFIER INPUT AND GAIN STAGE

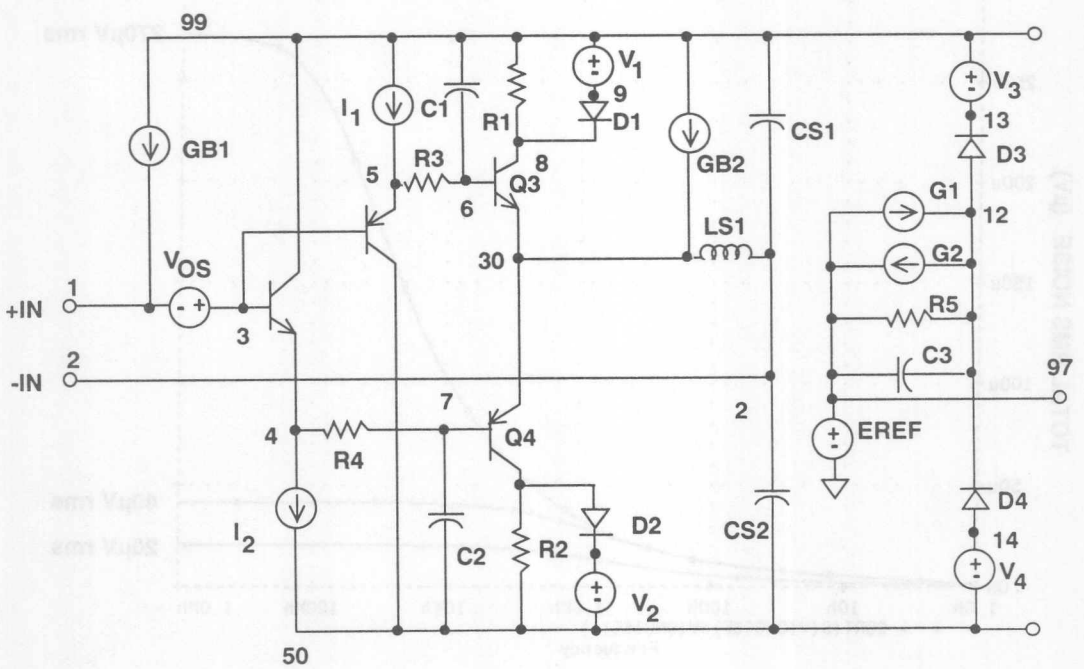


Figure 13.11

compares the ADSpice model to the actual device for an AD811 video amplifier. As the graphs show,the ADSpice model accurately predicts the gain roll off at the much lower frequency for the 1kΩ feedback resistor than for the 500Ω resistor.

The current feedback amplifier input stage is yet another enhancement to the ADSpice model that further increases its flexibility in modelling different types of devices to increase a design cycle's speed.

VOLTAGE REFERENCE MODEL

ADI is committed to continually expanding the library into new device types to make complete system analysis possible. One recent addition is a voltage reference model. This model was designed to accurately simulate most reference parameters such as DC accuracy, output noise, temperature drift, turn on time, and transient load settling time. The topology is actually very simple, consisting of an ideal 1.23V bandgap reference voltage, a gain stage, and an output stage as labelled in Figure 13.13. Again the macromodel approach is used to simplify the development and speed the simulation time. For example, the bandgap reference is simply a current source and a resistor to develop the required 1.23V. The additional controlled sources accurately predict line and load regulation. This is a great simplification of the actual device, without sacrificing accuracy.

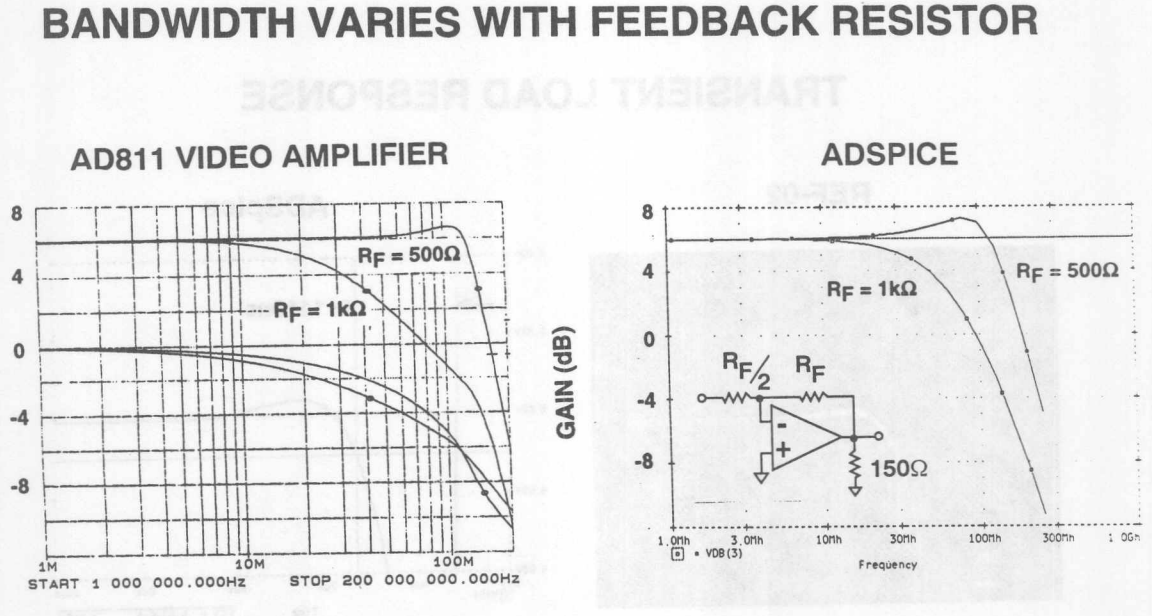


Figure 13.12

ADSPICE VOLTAGE REFERENCE MODEL

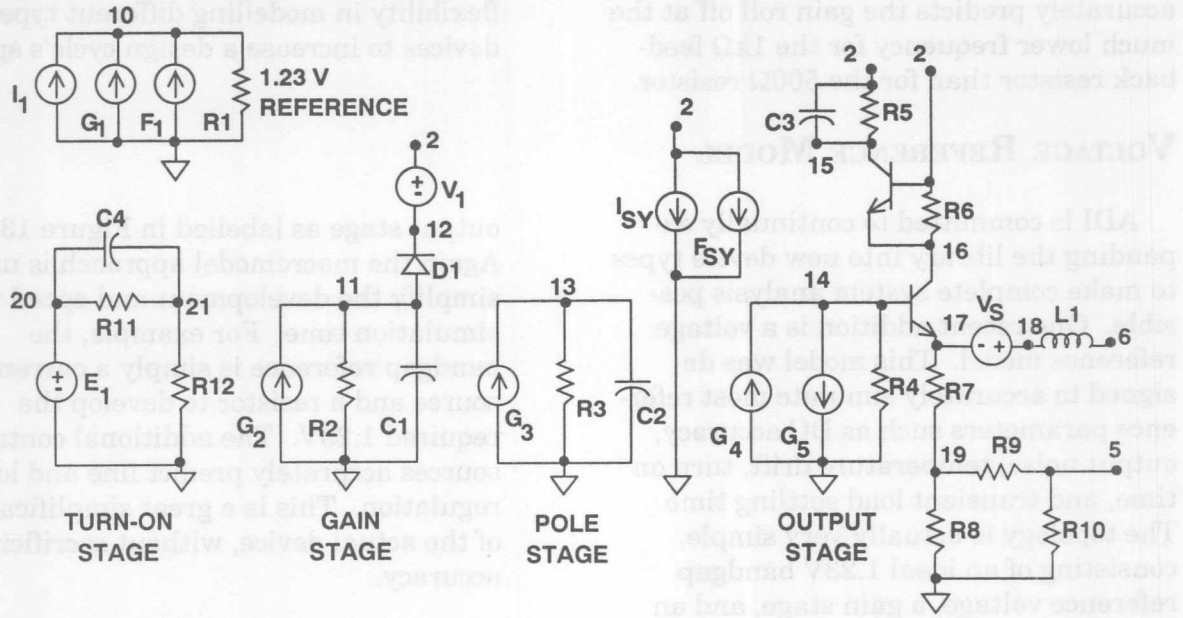
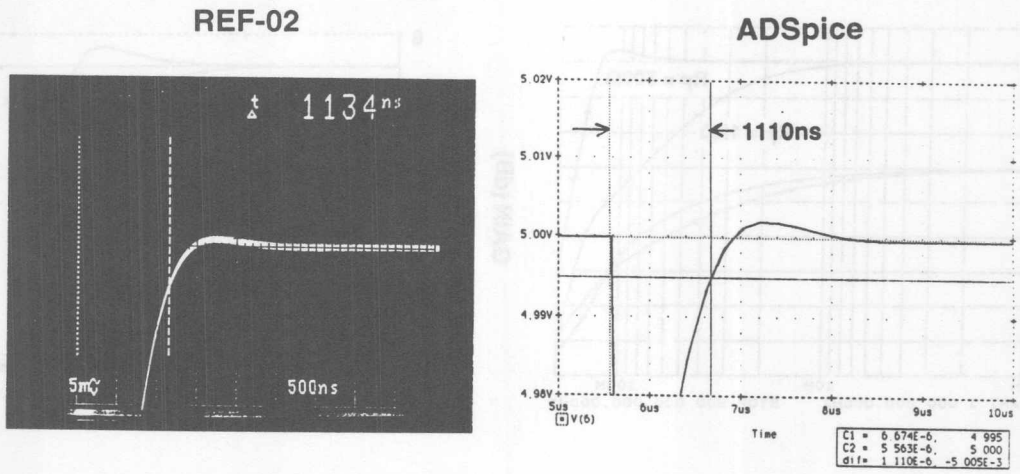


Figure 13.13

TRANSIENT LOAD RESPONSE



SETTLING TIME TO 0.1% FOR A 1mA STEP IN LOAD CURRENT

Figure 13.14

An important characteristic for voltage references is their ability to recover from transient load current pulses on their outputs. For example, some analog to digital converters produce a step change in load current on the reference during conversion. In such a case the reference needs to settle to its correct output voltage before the next conversion decision. This can affect the accuracy of the system making it important for the reference model to predict this. Figure 13.14 compares the response to a 1mA step change in the output current of the REF-02 to the SPICE model of the part. The two results show excellent agreement.

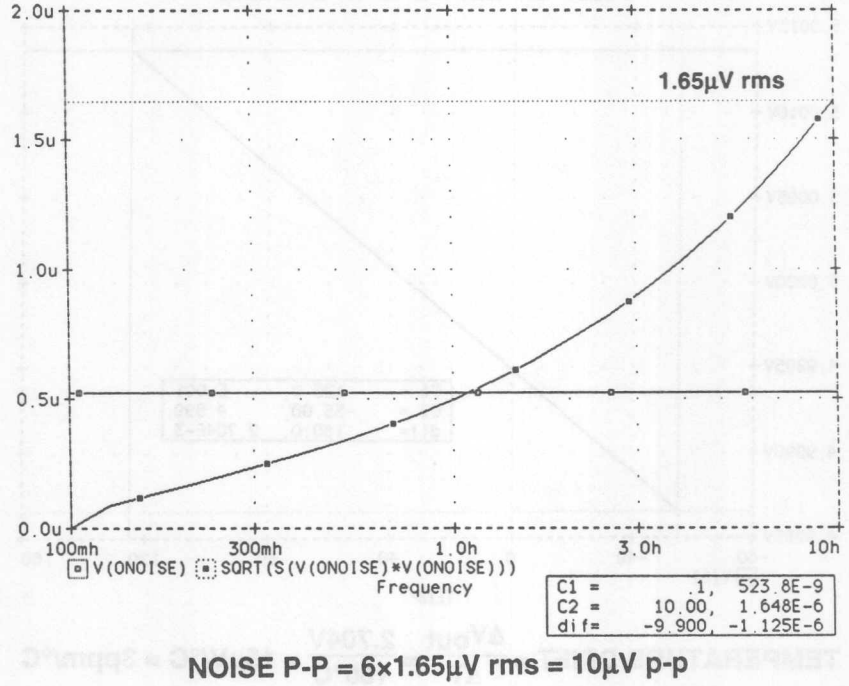
Another key parameter that can affect the accuracy of a system, especially as the resolution increases, is the output voltage noise. By properly setting the internal impedance of the 1.23V reference stage, the model can accurately simulate output noise. Figure 13.15 shows the broadband noise as well as the total noise for a 0.1 to 10Hz bandwidth. This correlates to the typical data sheet specification for the REF-02 noise of 10μVp-p, by using the standard multiplication factor of 6 to convert RMS to peak-to-peak noise.

Voltage references are required to maintain their accuracy over the full operating temperature range of the system. Thus, the drift needs to be very low, and any SPICE model needs to be able to predict this critical parameter. This is easily done by adding temperature dependance to the resistor in the bandgap reference stage. Temperature dependency in resistor models is a standard feature for all versions of SPICE and is set as follows:

R1 10 4 1000E3 [TC = 3E-6]

where the TC coefficient is the change in resistor value per degree Celsius. This

TOTAL RMS NOISE OF THE REF-02 ADSpice MODEL



NOISE P-P = 6x1.65μV rms = 10μV p-p

Figure 13.15

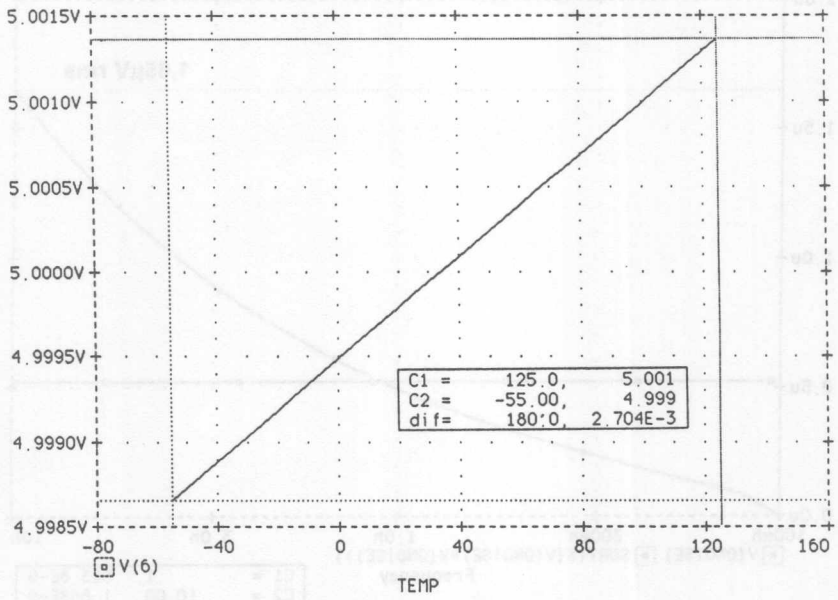
produces a linear variation of the output voltage with temperature. The actual device does have a somewhat non-linear temperature variation, but simplifying this to a linear coefficient still gives a good indication of the overall variation. The output plot in Figure 13.16 shows the typical temperature drift, which matches the data sheet parameter of 3ppm/°C. This new model is a complete reference model that yields accurate results under many real world input and loading conditions. Furthermore, it is one more significant piece in a system level analysis.

ANALOG MULTIPLIER MODEL

Like the voltage reference model, ADI has also developed the world's first analog multiplier macro model based on the AD734, a wideband, 4-quadrant analog multiplier. The development of the model offers significant benefits to system designers. Predicating the behavior of analog functions such as modulation/demodulation, frequency doubling, and high-speed RMS-to-DC conversion is a complex task by analytical means. However, with the new model, designers can, by computer simulation, quickly evaluate complex circuit responses under real world transient and small-signal conditions, thus saving time during the design cycle.

The topology of the macro model follows very closely to the block diagram of the AD734 which is shown in Figure 13.17. Each subsection of the model, including the denominator control and an internal voltage reference, was designed using techniques developed for the

TEMPERATURE DRIFT OF THE ADSpice REFERENCE MODEL



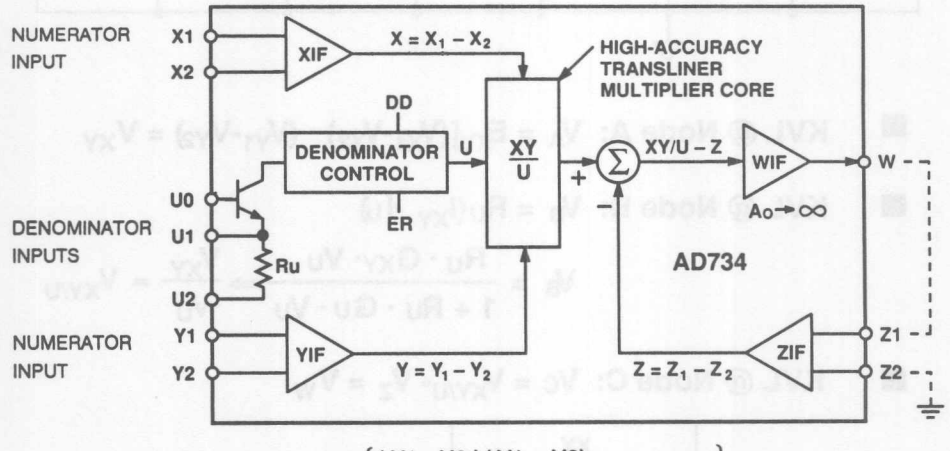
$$\text{TEMPERATURE DRIFT} = \frac{\Delta V_{out}}{\Delta T} = \frac{2.704V}{180°C} = 15\mu V/°C = 3ppm/°C$$

Figure 13.16

ADSpice op amp model. Only controlled sources and as few active devices as possible are used throughout the model to speed simulation time. For example, the macro model's input X-, Y-, and Z-interfaces were designed using only resistors, capacitors, and controlled sources to model the AD734's input offset voltages, input bias currents, common-mode rejection, and 40-MHz input bandwidth. Similarly, the design of macro model's output amplifier (the AD734's W-interface) was based on the op amp macro model's gain and output stage topology and accurately predicts the AD734's output voltage swing, open-loop voltage gain, short circuit current, 10 MHz 3-dB bandwidth, and 450-V/μs slew rate.

At the heart of the AD734 is a translinear multiplier core which exhibits a 250 MHz gain-bandwidth product and is based on the Gilbert multiplier cell. In its monolithic form, the AD734's core requires approximately 50 active and passive components to derive the transfer function, W = XY/U. Using a transistor level model for the translinear core would slow simulation time down so much as to make computer analysis of complex analog functions (for example, a frequency doubler) very CPU intensive and time consuming. As shown in Figure 13.18, the macro model's multiplier core was synthesized using only 8 ideal components to derive the same transfer function and gain-bandwidth product.

AD734 MULTIPLIER BLOCK DIAGRAM



$$W = \left[\frac{(X1 - X2)(Y1 - Y2)}{U1 - U2} - (Z1 - Z2)\right] A_0$$

Figure 13.17

To understand how the multiplier core works, KVL equations will be used. The voltage at node A is given by:

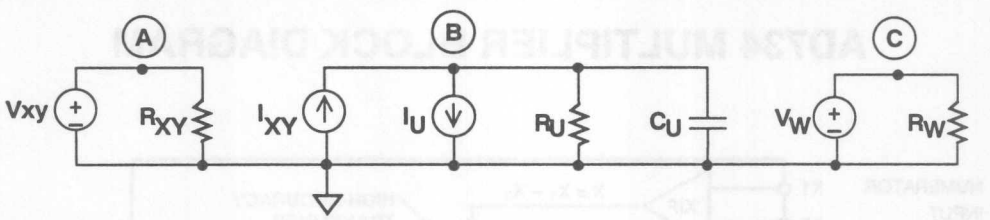
$$V_A = E_{XY} \cdot (V_{X1} - V_{X2}) \cdot (V_{Y1} - V_{Y2}) = V_{XY}$$

where the coefficient of E_{XY} is set to 1.

To arrive at the KVL equation for node B, V_A is first converted to a current by G_{XY}, such that $I_{XY} = G_{XY} \cdot V_A$. Then, a second controlled source, G_U (a second order polynomial), is used to generate a current such that $I_U = G_U \cdot (V_U \cdot V_B)$. The KVL equation at Node B is given by:

$$V_B = R_U \cdot (I_{XY} - I_U)$$

AD734 SPICE MACRO MODEL MULTIPLIER CORE WITH 250 MHz GAIN-BANDWIDTH PRODUCT



- KVL @ Node A: $V_A = E_{XY}[(V_{X1}-V_{X2}) \cdot (V_{Y1}-V_{Y2}) = V_{XY}$
- KVL @ Node B: $V_B = R_U(I_{XY} - I_U)$

$$V_B = \frac{R_U \cdot G_{XY} \cdot V_U}{1 + R_U \cdot G_U \cdot V_U} \Rightarrow \frac{V_{XY}}{V_U} = V_{XY/U}$$

- KVL @ Node C: $V_C = V_{XY/U} - V_Z = V_W$

$$\boxed{W = \frac{XY}{U} - Z}$$

Figure 13.18

Substituting $G_{XY} \cdot V_A$ for I_{XY} and $G_U \cdot (V_U \cdot V_B)$ for I_U yields:

$$V_B = R_U \cdot (G_{XY} \cdot V_A - G_U \cdot V_U \cdot V_B)$$

Simplifying the equation by solving for V_B yields:

$$V_B = \frac{R_U G_{XY} V_U}{1 + R_U G_U V_U}$$

Setting G_{XY} and G_U to 1 and R_U to 1E12 simplifies the expression for the voltage at node B to:

$$V_B = = V_{XY/U}$$

Lastly, the AD734 high-gain output op amp nulls the difference between XY/U and an additional input, Z = Z1 - Z2, to generate the final output, W. This is done in the macro model by subtracting the Z input signal from XY/U using another controlled source, E_W. Hence, the voltage at node C is given by:

$$V_C = E_W \cdot (V_{XY/U} - V_Z)$$

and, as was done for E_{XY}, the coefficient of E_W is set to 1.

To complete the multiplier core, a capacitor, C_U, was added across R_U to model the 250 MHz gain-bandwidth product of the AD734. The versatility of the AD734 to be configured as a three-variable analog multiplier/divider (shown in Figure 13.19) by using direct denominator control permitted evaluation of the macro model's small-signal response. The model's performance (Figure 13.20b) shows excellent agreement to the actual measured data (Figure 13.20a) for four denominator settings.

THREE VARIABLE MULTIPLIER/DIVIDER USING DIRECT DENOMINATOR CONTROL

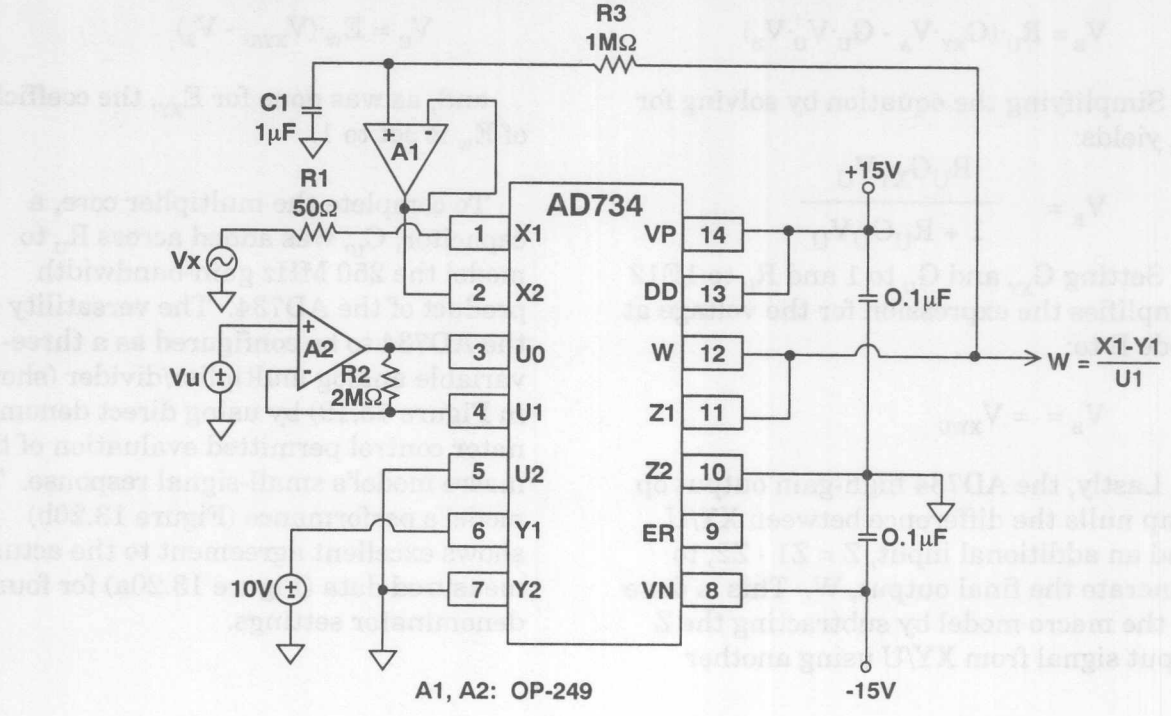


Figure 13.19

SMALL SIGNAL AC RESPONSE COMPARISON FOR AD734 THREE-VARIABLE MULTIPLIER

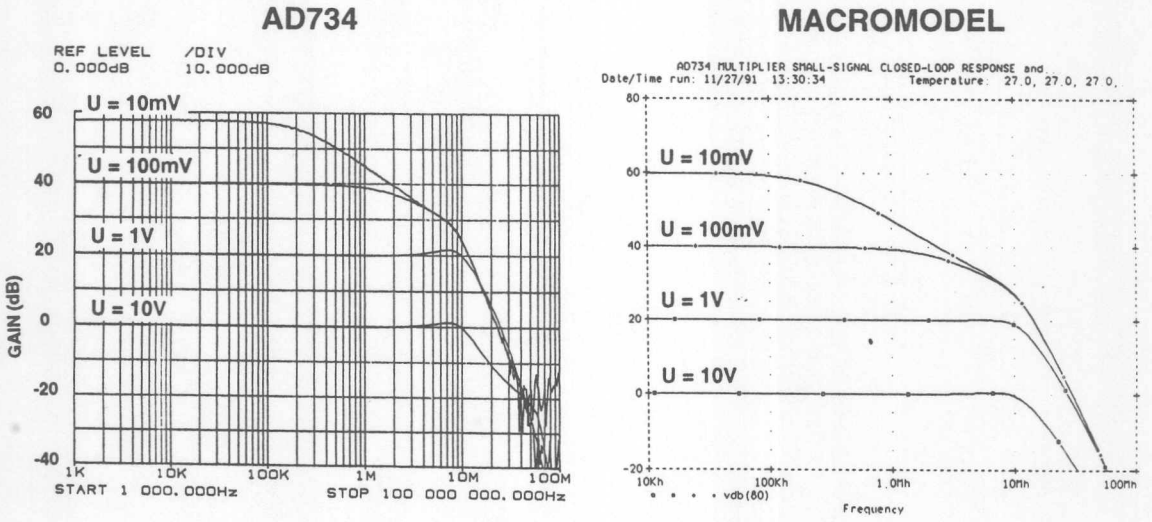


Figure 13.20

In avionics and communications, one of the most important characteristics of an analog multiplier is its transient response. It is important in these applications that an analog multiplier exhibit high slew rates to maintain high full-power bandwidths with low distortion. The AD734 is the ideal device for these applications and the macro model accurately simulates the AD734's transient response. The comparisons were done using the circuit in Figure 13.21 where the load circuit consisted of 500 ohms in parallel with 20 pF. The use of frequency shaping stages in the macro model permitted custom tailoring of the AD734's small-signal and transient response with a high degree of accuracy, as Figure 13.22 shows.

It is the accurate modeling of AD734's small-signal and transient response, as well as incorporating its DC parameters, that makes the macro model a very powerful tool in evaluating and analyzing complex analog circuits and systems. Accurately predicting real circuit behavior under small-signal and transient conditions provides a high level of confidence in the design of an analog system. To this end, Analog Devices is committed to developing new macro models for other non-linear analog building block circuits.

CIRCUIT DIAGRAM OF THE AD734 USED TO EVALUATE TRANSIENT RESPONSE

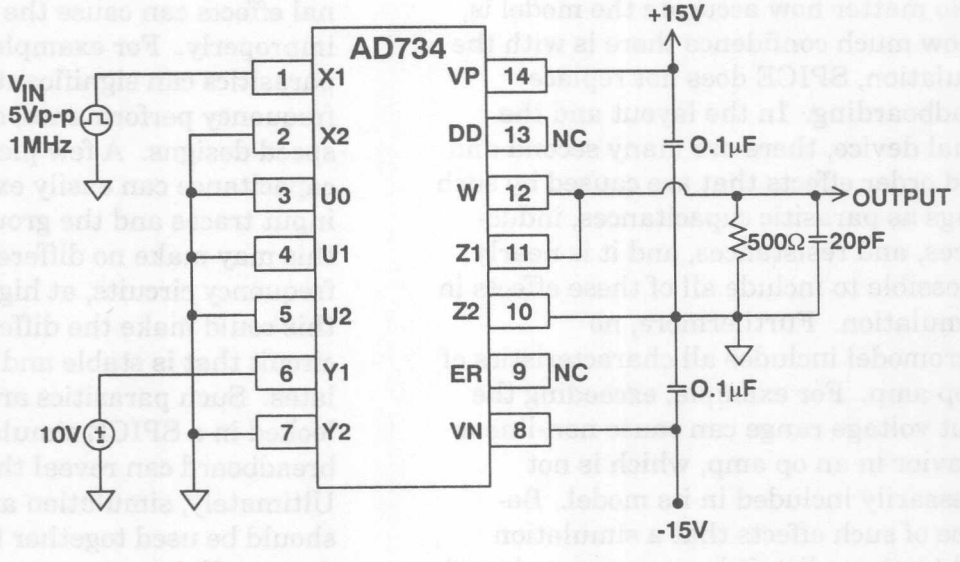
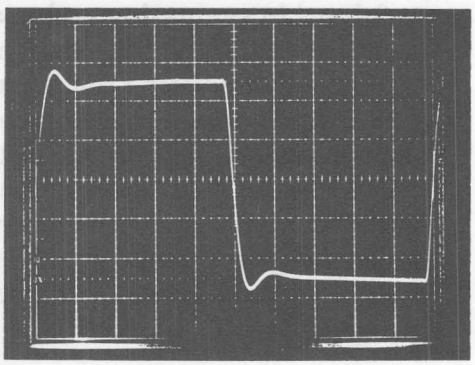


Figure 13.21

AD734 ACTUAL VERSUS SIMULATED TRANSIENT RESPONSE COMPARISON

AD734



VERTICAL = 1V/div.
HORIZONTAL = 100ns/div.

MACROMODEL

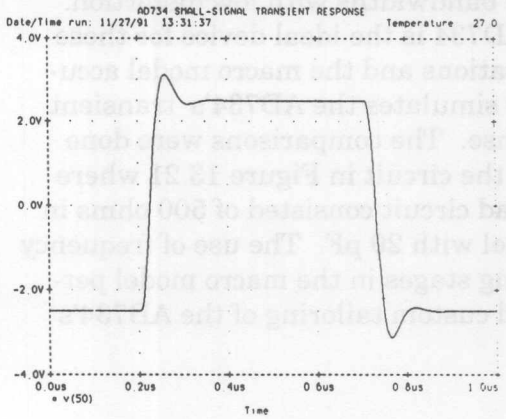


Figure 13.22

SIMULATION DOES NOT REPLACE BREADBOARDING

No matter how accurate the model is, or how much confidence there is with the simulation, SPICE does not replace breadboarding. In the layout and the actual device, there are many second and third order effects that are caused by such things as parasitic capacitances, inductances, and resistances, and it is nearly impossible to include all of these effects in a simulation. Furthermore, no macromodel includes all characteristics of an op amp. For example, exceeding the input voltage range can cause non-linear behavior in an op amp, which is not necessarily included in its model. Because of such effects that a simulation might not predict, it is necessary to breadboard the circuit.

Even with a model as comprehensive as the ADSpice macromodel, other external effects can cause the circuit to work improperly. For example, PC board parasitics can significantly alter the frequency performance, especially for high speed designs. A few picofarads of stray capacitance can easily exist between the input traces and the ground plane. While this may make no difference in lower frequency circuits, at high frequencies this could make the difference between a circuit that is stable and one that oscillates. Such parasitics are easily overlooked in a SPICE simulation, but a breadboard can reveal the instability. Ultimately, simulation and breadboarding should be used together to maximize the design efficiency.

BREADBOARDING AND SPICE

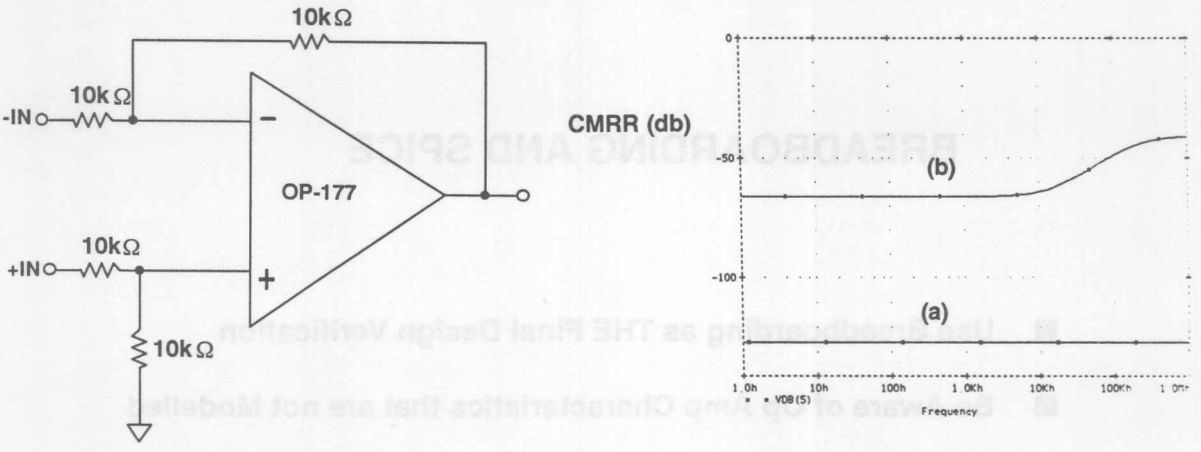
- **Use Breadboarding as THE Final Design Verification**
- **Be Aware of Op Amp Characteristics that are not Modelled**
- **Pay Attention to PC Board Parasitics that could Impact the Circuit's Behavior**

Figure 13.23

USE SIMULATION WISELY

Simulation is an extremely powerful tool, but it must be used wisely to realize all its benefits. This includes knowing the models well, understanding PC board effects, and anticipating the results. For example, consider a simple differential instrumentation amplifier (Figure 13.24a) comprised of an op amp and four resistors that needs to be analyzed for common mode rejection ratio(CMRR) performance. The CMRR at low frequencies will be dominated by resistor mismatch and at higher frequencies by the op amp's CMRR performance. However, the simulation will only show this if the external resistors are mismatched and the op amp properly models not only CMRR at DC but also the reduction in CMRR at higher frequencies. If these two important points are overlooked then the bottom plot in Figure 13.24b results. This shows excellent CMRR performance over the entire bandwidth of the circuit. Unfortunately, it is not correct. In contrast, substituting an ADSpice model, which has CMRR modelled as a function frequency, and substituting mismatched resistors results in the top plot in Figure 13.20b Now the picture is very different, showing realistic CMRR performance including the expected rise at higher frequencies.

KNOW WHAT IS AND IS NOT MODELLED



CMRR Test Circuit

(a) Resistors not mismatched and SPICE model not complete.

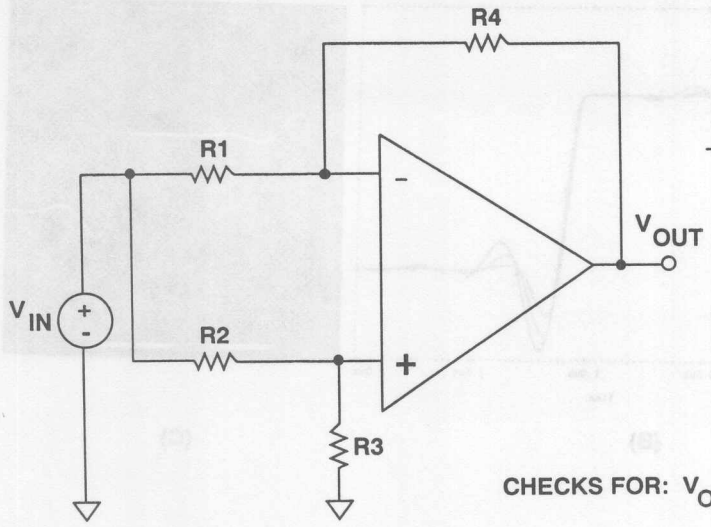
(b) Resistor with 0.1% tolerance and OP-177 ADSpice model includes CMRR vs. Frequency.

Figure 13.24

KNOW THE MODELS

The above example illustrates the importance of knowing the goals of a simulation and evaluating the models accordingly. In fact, one of the first steps in doing a simulation should be to check each model for its accuracy and what is included. Perhaps even more important is to understand what is not modelled in order to anticipate situations where the simulation may not yield the correct results. The best way to check a model is to actually perform simulations and check the results. Figure 13.25 shows a simple configuration to check DC parameters such as offset voltage and input currents. The accompanying table shows the values for the resistors and the resulting output. For the first three tests no input voltage source is needed, and the input resistors are tied to ground. A value of 0Ω in the table indicates a short, and infinity Ω indicates an open. The DC bias solution for the output voltage gives the result listed for the first three tests. The CMRR test is the only one that requires an AC sweep over the frequency range of the amplifier. This test reveals both the DC value and the high frequency roll off if it is included, as in the ADSpice models. Similar simple tests can be devised to check many other DC and AC parameters.

A SIMPLE TEST CIRCUIT FOR DC PARAMETERS



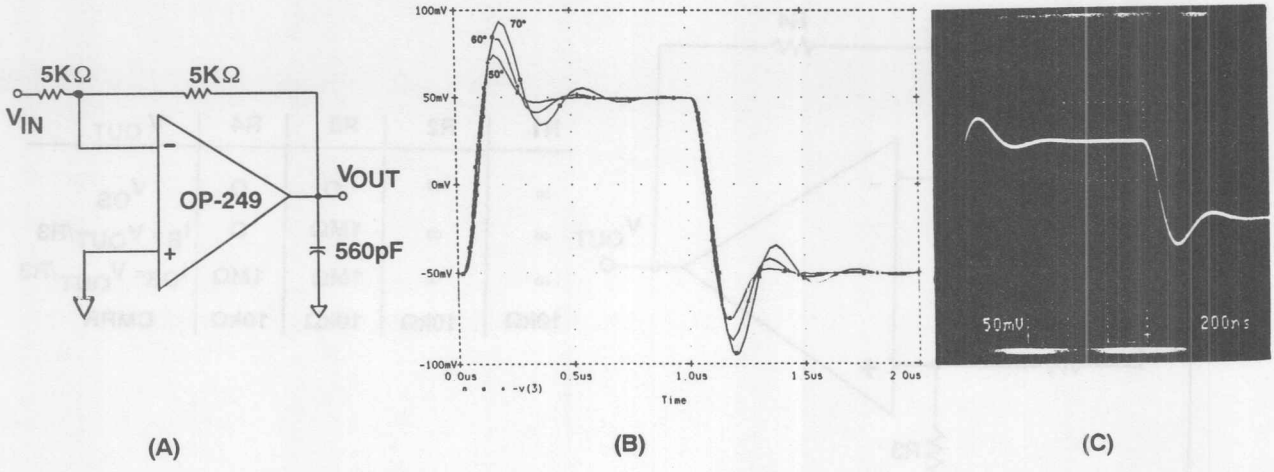
R1	R2	R3	R4	V_{OUT}
∞	∞	0	0	V_{OS}
∞	∞	1MΩ	0	$I_B = V_{OUT}/R3$
∞	∞	1MΩ	1MΩ	$I_{OS} = V_{OUT}/R3$
10kΩ	10kΩ	10kΩ	10kΩ	CMRR

Figure 13.25

The gain and phase margin of a circuit determines many important performance characteristics such as overshoot, settling time, and oscillation. For the simulation to accurately predict these parameters, the model must have an accurate open-loop gain and phase response. Having an accurate AC SPICE model increases the confidence level that the desired response of the actual circuit will behave close to the simulation results.

Using a simple inverting amplifier configuration, the open-loop gain and phase can be determined by dividing the output voltage by the error voltage on the inverting input. The simulation output can then be compared to data sheet graphs. Unfortunately, many data sheets only show the amplifier's dominant pole. This leaves many questions about the actual characteristics of the gain and phase, especially near the op amp's unity gain crossover. The same test can be performed on the actual device using a network analyzer; however, this may not be a feasible option. Fortunately, a transient response test reveals much of the same information in the amount of overshoot, frequency of ringing, and the damping characteristics.

TRANSIENT RESPONSE REVEALS PHASE MARGIN



(A) (B) (C)

• 60° phase curve agrees with actual device

Figure 13.26

Figure 13.26 shows the transient response of the OP-249 SPICE model with a capacitive load to induce ringing. The phase margin is adjusted for the different simulations as labelled next to each curve. As can be seen, a 10° decrease in phase margin leads to a significant change in the amount of overshoot and frequency of ringing on the output. A photo of the actual device's performance is also shown for comparison, which shows good agreement with the 60° curve. This result correlates with comparisons of the frequency response of the OP-249 to its SPICE model, which both show a phase margin of 60°. Thus, checking the transient response can reveal the accuracy of a model's phase response.

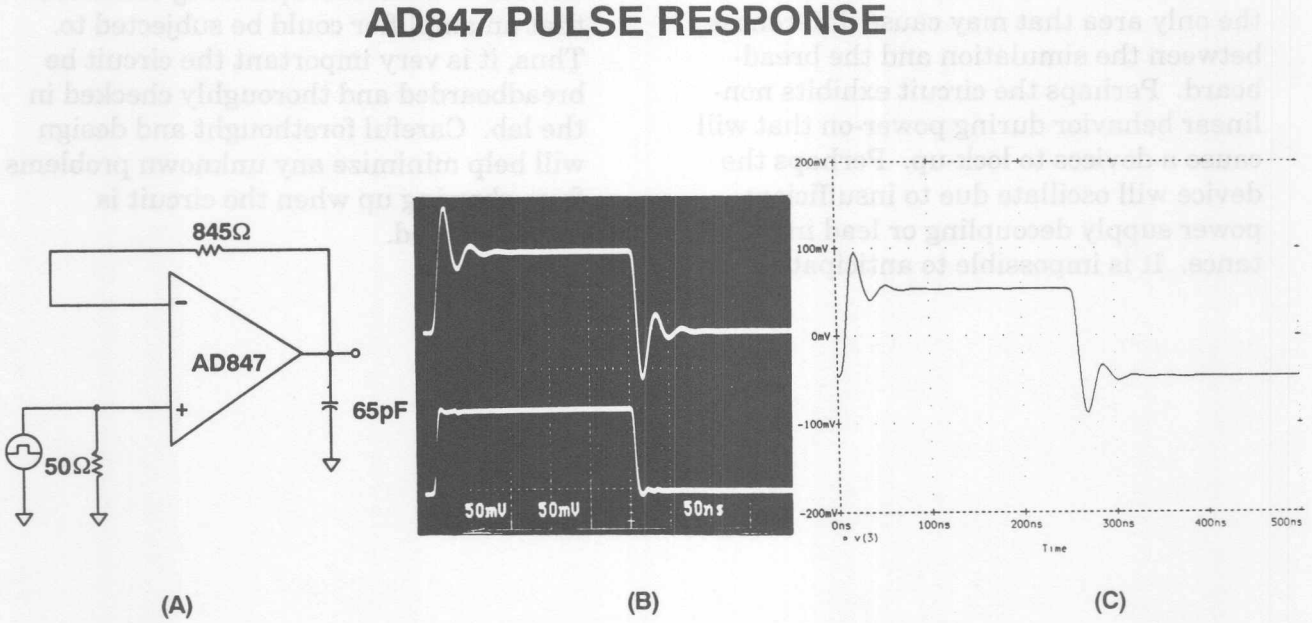
The small signal transient response is one of the most important of all the tests in determining a model's AC accuracy. Even if a network analyzer is available to check the frequency response, the small signal pulse response should still be compared. It is also informative to check how the model behaves with a capacitive load. Placing varying capacitances on the output and looking at the change in overshoot and ringing further verifies the model.

Using the above tests, an op amp macromodel, regardless of source, can be checked for accuracy. Further tests can be devised for other op amp parameters that may be important for a particular simulation. All of which is important because knowing the model's capabilities ahead of time can help prevent many headaches later.

UNDERSTAND PC BOARD PARASITICS

Even if the model passes all the above tests, caution still needs to be exercised. As discussed above, PC board parasitics can have significant impact on a circuit's performance. This is especially true for high speed circuits. A few picofarads of capacitance on the input node can make the difference between a stable circuit and one that oscillates. Thus, these effects need to be carefully considered when simulating the circuit to achieve meaningful results.

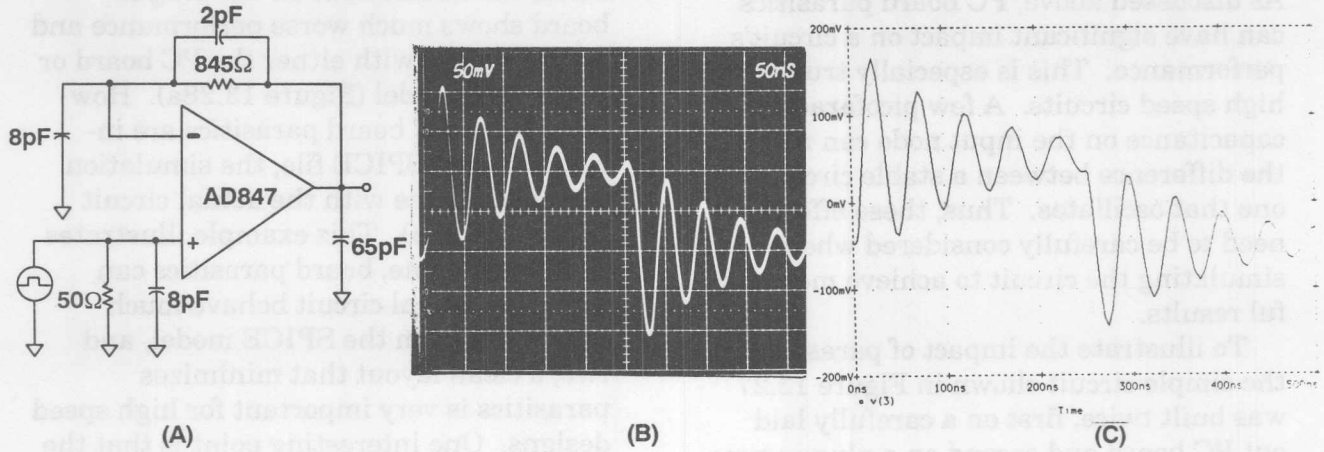
To illustrate the impact of parasitics, the simple circuit shown in Figure 13.27 was built twice, first on a carefully laid out PC board and second on a plug-in type of protoboard. The AD847 is used because of its wide bandwidth of 50 MHz, which makes any parasitics much more critical. The properly laid out PC board has a clean response with less overshoot and ringing (Figure 13.27b). The SPICE model results are in close agreement with the actual circuit showing an accurate simulation (Figure 13.27c). On the other hand, the circuit built on the plug-in board shows much worse performance and no agreement with either the PC board or the SPICE model (Figure 13.28a). However, when PC board parasitics are included in the SPICE file, the simulation results do agree with the actual circuit (Figure 13.28b). This example illustrates two points. One, board parasitics can make the actual circuit behave much differently from the SPICE model, and two, a clean layout that minimizes parasitics is very important for high speed designs. One interesting point is that the simulation can be used as a rough measure of the PCB layout design. If the simulation, without any parasitics, agrees with the PC board, then there is a reasonable assurance that PC board is well laid out.



Properly laid out PC board and simulation agree closely

Figure 13.27

PC BOARD PARASITICS WILL ALTER THE RESULTS



(A) (B) (C)

- **Parasitic capacitances worsen the circuit's response**
- **Properly modelling the parasitics in SPICE yields good results**

Figure 13.28

Parasitic PC board elements are not the only area that may cause differences between the simulation and the breadboard. Perhaps the circuit exhibits non-linear behavior during power-on that will cause a devices to lock-up. Perhaps the device will oscillate due to insufficient power supply decoupling or lead inductance. It is impossible to anticipate all normal or abnormal operating conditions that an amplifier could be subjected to. Thus, it is very important the circuit be breadboarded and thoroughly checked in the lab. Careful forethought and design will help minimize any unknown problems from showing up when the circuit is manufactured.

SIMULATION SPEEDS THE DESIGN CYCLE

While simulation cannot replace breadboarding, the two can be used together to increase the efficiency of a design cycle. Simulation is very effective in the initial design phase to try out different ideas and circuit configurations. When a circuit topology has been decided upon and tested in SPICE, then a breadboard can be built. If the simulation was done carefully, the breadboard has good likelihood of working correctly without significant modifications. When the simulation and the actual results correlate, then the circuit can be easily altered in SPICE to perform many different types of analysis. For example, it is much easier to try to optimize the circuit in SPICE then it is to repeatedly modify the breadboard. Quick substitutions of the op amps and components can be made in SPICE and the results immediately viewed. Worst-case and sensitivity analysis can also be done in SPICE easier then on paper or on a breadboard. Using multiple SPICE runs, the sensitivity to a certain parameter can be determined.

SPICE SAVES DESIGN TIME

- **Quickly Checks Circuit Ideas**
- **Eases Circuit Optimization**
- **Alter Component and Model Parameters for Worst Case Sensitivity Analysis**
- **Quickly Check Different Op Amps**

13

Figure 13.29

There are many ways in which SPICE and the ADSpice macromodel make the design task easier. SPICE is a very effective design tool if it is used with forethought, understanding, and caution. The complete ADSpice library is available on a 1.2Mbit, 5-1/4" IBM PC compatible diskette. Contact your local sales office or the Analog Devices Literature Center for your free copy. The complete list of all 264 models on the "Release E, 10/91" version of the diskette is shown in Figure 13.30.

ADSpice Release E, 10/91

AD624 *	AD744	OP160A	OP27B	OP43B
AD624A *	AD744A	OP160F	OP27C	OP43E
AD624B *	AD744B	OP160G	OP27E	OP43F
AD624C *	AD744C	OP177	OP27F	OP43G
AD624S *	AD744J	OP177A	OP27G	OP44
AD645	AD744K	OP177B	OP290	OP470
AD645A	AD744S	OP177E	OP290A	OP490
AD645B	AD744T	OP177F	OP290E	OP490A
AD645J	AD746	OP177G	OP290F	OP490E
AD645K	AD746A	OP20 *	OP290G	OP490F
AD645S	AD746B	OP20B *	OP297	OP490G
AD704 *	AD746J	OP20C *	OP297A	OP497 *
AD704A *	AD746S	OP20F *	OP297E	OP497A *
AD704B *	AD811 *	OP20G *	OP297F	OP497B *
AD704J *	AD829	OP20H *	OP297G	OP497C *
AD704K *	AD829A	OP200	OP37	OP497F *
AD704T *	AD829J	OP200A	OP37A	OP497G *
AD705 *	AD829S	OP200E	OP37B	OP61
AD705A *	AD840	OP200F	OP37C	OP64
AD705B *	AD840J	OP200G	OP37E	OP77
AD705J *	AD840K	OP21 *	OP37F	OP77A
AD705K *	AD840S	OP21A *	OP37G	OP77B
AD705T *	AD844 *	OP21E *	OP400	OP77E
AD706 *	AD844A *	OP21F *	OP400A	OP77F
AD706A *	AD844B *	OP21G *	OP400E	OP77G
AD706B *	AD844S *	OP21H *	OP400F	OP90
AD706J *	AD845	OP215	OP400G	OP90A
AD706K *	AD845A	OP215A	OP400H	OP90E
AD706T *	AD845B	OP215B	OP41	OP90F
AD711	AD845J	OP215C	OP41A	OP90G
AD711A	AD845K	OP215E	OP41B	OP97
AD711B	AD845S	OP215F	OP41E	PM1012
AD711C	AD846	OP215G	OP41F	REF01 *
AD711J	AD846A	OP220 *	OP41G	REF01A *
AD711K	AD846B	OP220A *	OP42	REF01C *
AD711S	AD846S	OP220C *	OP42A	REF01E *
AD711T	AD847	OP220E *	OP42E	REF01H *
AD712	AD847A	OP220F *	OP42F	REF02 *
AD712A	AD847J	OP220G *	OP42G	REF02A *
AD712B	AD847S	OP221 *	OP420 *	REF02C *
AD712C	AD848	OP221A *	OP420B *	REF02D *
AD712J	AD848A	OP221B *	OP420C *	REF02E *
AD712K	AD848J	OP221C *	OP420F *	REF02H *
AD712S	AD848S	OP221E *	OP420G *	REF05 *
AD712T	AD9617	OP221G *	OP420H *	REF05A *
AD713	AD9618	OP249	OP421 *	REF05B *
AD713A	AD9630	OP249A	OP421B *	REF10 *
AD713B	AMP01	OP249E	OP421C *	REF10A *
AD713J	AMP02	OP249F	OP421F *	REF10B *
AD713K	MAT02	OP249G	OP421G *	SSM2131
AD713S	MAT03	OP260	OP421H *	SSM2210
AD713T	MAT04	OP27	OP43	SSM2220
AD734 *	OP160	OP27A	OP43A	

Figure 13.30

NOTES

[1] Boyle, Graeme et al, "Macromodelling of Integrated Circuit Operational Amplifiers," IEEE Journal of Solid State Circuits, Vol. sc-9, no. 6, December 1974

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